



LPC3152/3154

ARM926EJ microcontrollers with USB High-speed OTG, SD/MMC, NAND flash controller, and audio codec

Rev. 0.12 — 27 May 2010

Preliminary data sheet

1. General description

The NXP LPC3152/3154 combine an 180 MHz ARM926EJ-S CPU core, High-speed USB 2.0 OTG, 192 kB SRAM, NAND flash controller, flexible external bus interface, an integrated audio codec, Li-ion charger, Real-Time Clock (RTC), and a myriad of serial and parallel interfaces in a single chip targeted at consumer, industrial, medical, and communication markets. To optimize system power consumption, the LPC3152/3154 have multiple power domains and a very flexible Clock Generation Unit (CGU) that provides dynamic clock gating and scaling.

The LPC3152/3154 are implemented as a multi-chip module with two side-by-side dies, one for digital functions and one for analog functions, which include Power Supply Unit (PSU), audio codec, RTC, and Li-ion battery charger.

2. Features and benefits

2.1 Key features

- CPU platform
 - ◆ 180 MHz, 32-bit ARM926EJ-S
 - ◆ 16 kB D-cache and 16 kB I-cache
 - ◆ Memory Management Unit (MMU)
- Internal memory
 - ◆ 192 kB embedded SRAM
- External memory interface
 - ◆ NAND flash controller with 8-bit ECC and AES decryption engine (LPC3154 only)
 - ◆ 8/16-bit Multi-Port Memory Controller (MPMC): SDRAM and SRAM
- Security
 - ◆ AES decryption engine (LPC3154 only)
 - ◆ Secure one-time programmable memory for AES key storage and customer use
 - ◆ 128 bit unique ID per device for DRM schemes
- Communication and connectivity
 - ◆ High-speed USB 2.0 (OTG, Host, Device) with on-chip PHY
 - ◆ Two I²S-bus interfaces
 - ◆ Integrated master/slave SPI
 - ◆ Two master/slave I²C-bus interfaces
 - ◆ Fast UART
 - ◆ Memory Card Interface (MCI): MMC/SD/SDIO/CE-ATA



- ◆ Three-channel 10-bit ADC
- ◆ Integrated 4/8/16-bit 6800/8080 compatible LCD interface
- ◆ Integrated audio codec with stereo ADC and Class AB headphone amplifier
- System functions
 - ◆ Dynamic clock gating and scaling
 - ◆ Multiple power domains
 - ◆ Selectable boot-up: SPI flash, NAND flash, SD/MMC cards, UART, or USB
 - ◆ On the LPC3154 only: secure booting using AES decryption engine from SPI flash, NAND flash, SD/MMC cards, UART, or USB
 - ◆ DMA controller
 - ◆ Four 32-bit timers
 - ◆ Watchdog timer
 - ◆ PWM module
 - ◆ Master/slave PCM interface
 - ◆ Random Number Generator (RNG)
 - ◆ General Purpose I/O (GPIO) pins
 - ◆ Flexible and versatile interrupt structure
 - ◆ JTAG interface with boundary scan and ARM debug access
 - ◆ Real-Time Clock (RTC)
- Power supply
 - ◆ Integrated power supply unit
 - ◆ Li-ion charger
 - ◆ USB charge pump
- Operating voltage and temperature
 - ◆ Core voltage: 1.2 V
 - ◆ I/O voltage: 1.8 V, 3.3 V
 - ◆ Temperature: -40 °C to +85 °C
- TFBGA208 package: 12 × 12 mm², 0.7 mm pitch

3. Ordering information

Table 1. Ordering information

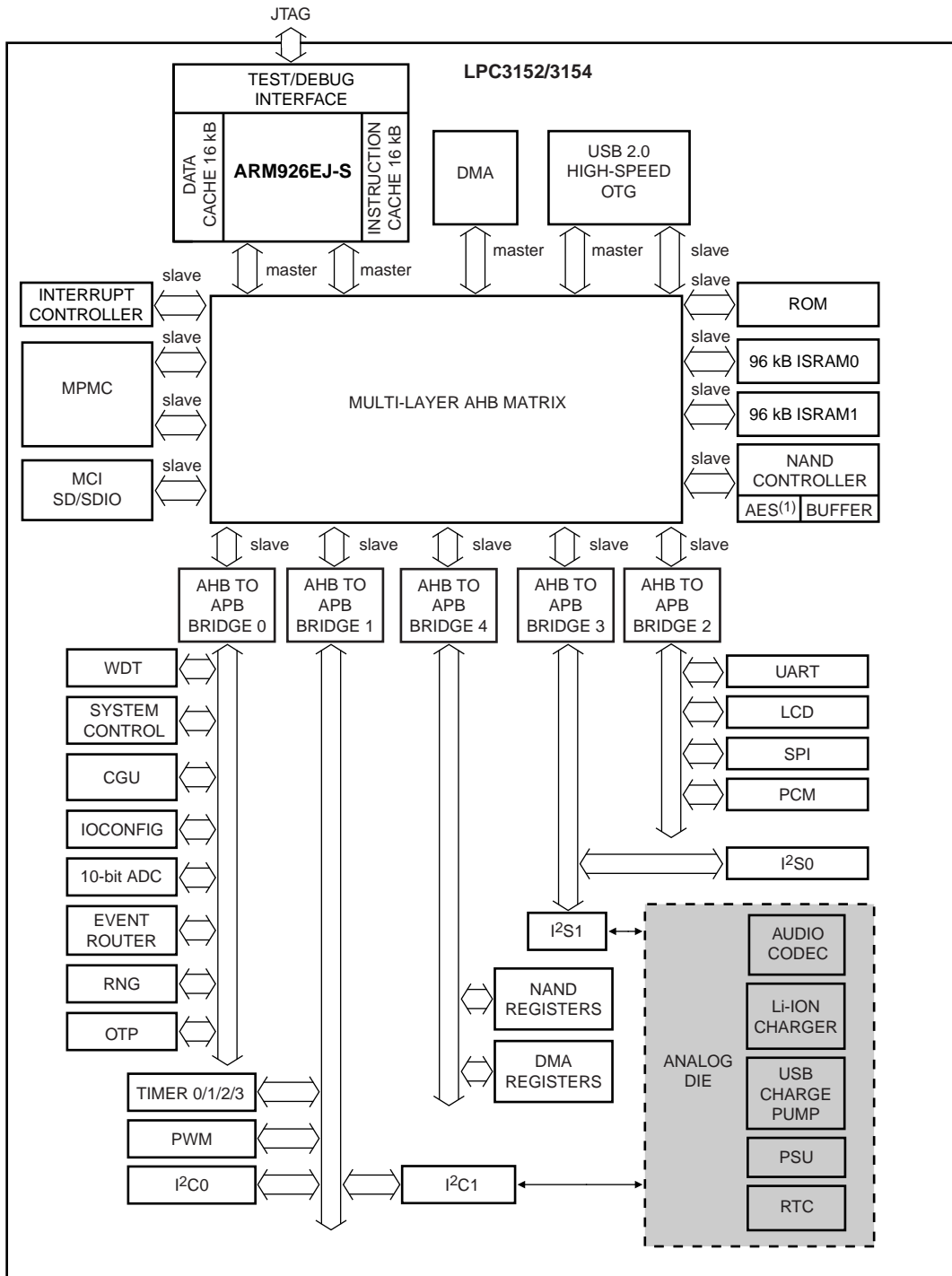
| Type number | Package | | Version |
|---------------|----------|---|----------|
| | Name | Description | |
| LPC3152FET208 | TFBGA208 | TFBGA208: plastic thin fine-pitch ball grid array package; 208 balls; body 12 x 12 x 0.7 mm | sot930-1 |
| LPC3154FET208 | TFBGA208 | TFBGA208: plastic thin fine-pitch ball grid array package; 208 balls; body 12 x 12 x 0.7 mm | sot930-1 |

3.1 Ordering options

Table 2. Ordering options for LPC3152/54

| Type number | Total SRAM | NAND Flash Controller | Security engine AES | High-speed USB | 10-bit ADC channels | Audio codec, PSU, RTC, Li-ion charger | MCI SDHC/SDIO/CE-ATA | Pins | Temperature range |
|---------------|------------|-----------------------|---------------------|-----------------|---------------------|---------------------------------------|----------------------|------|-------------------|
| LPC3152FET208 | 192 kB | yes | no | Device/Host/OTG | 3 | yes | yes | 208 | -40 °C to +85 °C |
| LPC3154FET208 | 192 kB | yes | yes | Device/Host/OTG | 3 | yes | yes | 208 | -40 °C to +85 °C |

4. Block diagram



002aae095

(1) AES decryption engine available in LPC3154 only.

Fig 1. LPC3152/3154 block diagram

5. Pinning information

5.1 Pinning

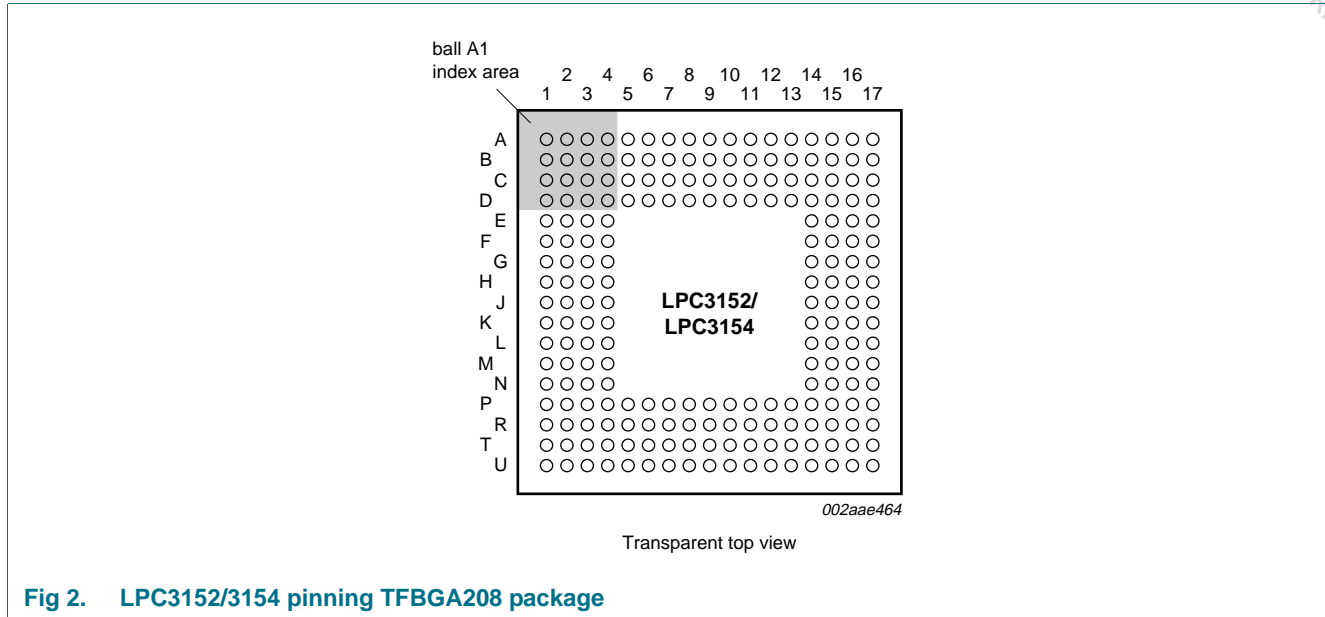


Fig 2. LPC3152/3154 pinning TFBGA208 package

Table 3. Pin allocation table

Pin names with prefix *m* are multiplexed pins. See Table 11 for pin function selection of multiplexed pins.

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|--------------|---------------|-----|-------------|-----|----------|-----|-------------|
| Row A | | | | | | | |
| 1 | n.c. | 2 | EBI_A_1_CLE | 3 | EBI_D_9 | 4 | VDDE_IOC |
| 5 | VSSE_IOC | 6 | VDDI | 7 | VSSI | 8 | SPI_MISO |
| 9 | I2C_SCL0 | 10 | FFAST_IN | 11 | n.c. | 12 | n.c. |
| 13 | ADC10B_GNDA | 14 | VSSE_IOC | 15 | VDDE_IOC | 16 | HP_VDDA33 |
| 17 | n.c. | - | - | - | - | - | - |
| Row B | | | | | | | |
| 1 | n.c. | 2 | n.c. | 3 | n.c. | 4 | n.c. |
| 5 | mNAND_RYBN0 | 6 | mGPIO9 | 7 | mGPIO6 | 8 | SPI_MOSI |
| 9 | n.c. | 10 | FFAST_OUT | 11 | VDDA12 | 12 | ADC10B_GPA0 |
| 13 | ADC10B_VDDA33 | 14 | n.c. | 15 | HP_FCR | 16 | HP_GNDA |
| 17 | HP_OUTL | - | - | - | - | - | - |
| Row C | | | | | | | |
| 1 | n.c. | 2 | EBI_D_10 | 3 | n.c. | 4 | EBI_A_0_ALE |
| 5 | mNAND_RYBN1 | 6 | mGPIO10 | 7 | mGPIO7 | 8 | SPI_SCK |
| 9 | VPP | 10 | I2C_SDA0 | 11 | VSSA12 | 12 | ADC10B_GPA2 |
| 13 | ADC10B_GPA1 | 14 | DAC_VDDA33 | 15 | HP_OUTR | 16 | HP_FCL |
| 17 | PSU_PLAY | - | - | - | - | - | - |
| Row D | | | | | | | |
| 1 | VDDE_IOA | 2 | EBI_D_11 | 3 | EBI_D_8 | 4 | mNAND_RYBN3 |

Table 3. Pin allocation table ...continued

Pin names with prefix *m* are multiplexed pins. See [Table 11](#) for pin function selection of multiplexed pins.

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|--------------|----------------|-----|------------------|-----|---------------|-----|------------------|
| 5 | mNAND_RYBN2 | 6 | mGPIO8 | 7 | mGPIO5 | 8 | SPI_CS_OUT0 |
| 9 | SPI_CS_IN | 10 | PWM_DATA | 11 | GPIO4 | 12 | GPIO3 |
| 13 | n.c. | 14 | HP_OUTC | 15 | PSU_STOP | 16 | PSU_VSSA |
| 17 | PSU_VSSA_CLEAN | - | - | - | - | - | - |
| Row E | | | | | | | |
| 1 | VSSE_IOA | 2 | EBI_D_12 | 3 | EBI_D_7 | 4 | EBI_D_6 |
| 14 | HP_VREF | 15 | RSTIN_N | 16 | PSU_VBAT | 17 | PSU_VOUT3 |
| Row F | | | | | | | |
| 1 | n.c. | 2 | EBI_D_13 | 3 | EBI_D_5 | 4 | EBI_D_4 |
| 14 | TDO | 15 | DAC_VREFN | 16 | DAC_VREFP | 17 | PSU_VBAT2 |
| Row G | | | | | | | |
| 1 | n.c. | 2 | EBI_D_14 | 3 | n.c. | 4 | EBI_D_3 |
| 14 | PSU_VOUT2 | 15 | VDDE_IOD | 16 | PSU_VIN1 | 17 | PSU_LX2 |
| Row H | | | | | | | |
| 1 | VSSI | 2 | EBI_D_15 | 3 | EBI_D_1 | 4 | EBI_D_2 |
| 14 | PSU_VOUT1 | 15 | PSU_LX1 | 16 | PSU_VSS1 | 17 | PSU_VBAT1 |
| Row J | | | | | | | |
| 1 | VDDI | 2 | EBI_NCAS_BLOUT_0 | 3 | EBI_D_0 | 4 | EBI_NRAS_BLOUT_1 |
| 14 | CHARGE_VBUS | 15 | CHARGE_VSS | 16 | PSU_VBUS | 17 | CHARGE_VNTC |
| Row K | | | | | | | |
| 1 | VSSE_IOB | 2 | n.c. | 3 | EBI_DQM_0_NOE | 4 | EBI_NWE |
| 14 | RTC_BACKUP | 15 | CHARGE_CC_REF | 16 | CHARGE_VBAT | 17 | CHARGE_BAT_SENSE |
| Row L | | | | | | | |
| 1 | VDDE_IOB | 2 | NAND_NCS_0 | 3 | NAND_NCS_1 | 4 | NAND_NCS_2 |
| 14 | VSSE_IOD | 15 | RTC_VDD36 | 16 | FSLOW_OUT | 17 | FSLOW_IN |
| Row M | | | | | | | |
| 1 | VDDE_IOA | 2 | NAND_NCS_3 | 3 | n.c. | 4 | CLOCK_OUT |
| 14 | VDDI_AD | 15 | VSSI_AD | 16 | RTC_INT | 17 | RTC_VSS |
| Row N | | | | | | | |
| 1 | VSSE_IOA | 2 | USB_VDDA12_PLL | 3 | USB_VBUS | 4 | USB_RREF |
| 14 | ADC_VDDA33 | 15 | ADC_VDDA18 | 16 | ADC_GNDA | 17 | UOS_VSS |
| Row P | | | | | | | |
| 1 | n.c. | 2 | USB_VSSA_REF | 3 | USB_ID | 4 | mLCD_DB_10 |
| 5 | mLCD_DB_9 | 6 | mLCD_DB_5 | 7 | mLCD_E_RD | 8 | mLCD_DB_1 |
| 9 | I2SRX_DATA0 | 10 | UART_TXD | 11 | mUART_CTS_N | 12 | GPIO2 |
| 13 | ADC_TINL | 14 | ADC_TINR | 15 | UOS_VBUS | 16 | UOS_VBAT |
| 17 | UOS_CX2 | - | - | - | - | - | - |
| Row R | | | | | | | |
| 1 | USB_DM | 2 | USB_VSSA_TERM | 3 | USB_VDDA33 | 4 | mLCD_DB_15 |
| 5 | mLCD_DB_6 | 6 | mLCD_DB_3 | 7 | mLCD_RS | 8 | mLCD_CSB |

Table 3. Pin allocation table ...continued

Pin names with prefix *m* are multiplexed pins. See [Table 11](#) for pin function selection of multiplexed pins.

| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
|-----|-----------|-----|----------|-----|-------------|-----|------------|
| 9 | I2SRX_WS0 | 10 | UART_RXD | 11 | mUART_RTS_N | 12 | mI2STX_WS0 |
| 13 | GPIO0 | 14 | ADC_VINR | 15 | ADC_MIC | 16 | ADC_VREFN |
| 17 | UOS_CX1 | - | - | - | - | - | - |

Row T

| | | | | | | | |
|----|--------------|----|-----------|----|----------------|----|-------------|
| 1 | USB_DP | 2 | USB_GNDA | 3 | USB_VDDA33_DRV | 4 | mLCD_DB_12 |
| 5 | mLCD_DB_7 | 6 | mLCD_DB_2 | 7 | mLCD_DB_0 | 8 | mLCD_RW_WR |
| 9 | I2SRX_BCK0 | 10 | TDI | 11 | mI2STX_CLK0 | 12 | mI2STX_BCK0 |
| 13 | mI2STX_DATA0 | 14 | GPIO1 | 15 | ADC_VINL | 16 | ADC_VREF |
| 17 | ADC_VREFFP | - | - | - | - | - | - |

Row U

| | | | | | | | |
|----|-----------|----|------------|----|------------|----|------------|
| 1 | n.c. | 2 | mLCD_DB_14 | 3 | mLCD_DB_13 | 4 | mLCD_DB_11 |
| 5 | mLCD_DB_8 | 6 | mLCD_DB_4 | 7 | VDDE_IOB | 8 | VSSE_IOB |
| 9 | TMS | 10 | JTAGSEL | 11 | TRST_N | 12 | TCK |
| 13 | VDDI | 14 | VSSI | 15 | VDDE_IOC | 16 | VSSE_IOC |
| 17 | RTC_CLK32 | - | - | - | - | - | - |

Table 4. Pin description

Pin names with prefix *m* are multiplexed pins. See [Table 11](#) for pin function selection of multiplexed pins.

| TFBGA pin name | TFB GA ball | Digital I/O level [1] | Application function | Pin state after reset [2] | Cell type [3] | Description |
|----------------|-------------|-----------------------|----------------------|---------------------------|---------------|-------------|
|----------------|-------------|-----------------------|----------------------|---------------------------|---------------|-------------|

Clock generation unit

| | | | | | | |
|-----------|-----|------|--------|------|------|--------------------------------------|
| FFAST_IN | A10 | SUP1 | AI | | AIO2 | 12 MHz oscillator clock input |
| FFAST_OUT | B10 | SUP1 | AO | | AIO2 | 12 MHz oscillator clock output |
| VDDA12 | B11 | SUP1 | Supply | | PS3 | 12 MHz oscillator/PLLs analog supply |
| VSSA12 | C11 | - | Ground | | CG1 | 12 MHz oscillator/PLLs analog ground |
| RSTIN_N | E15 | SUP3 | DI | I:PU | DIO2 | System reset input (active LOW) |
| CLOCK_OUT | M4 | SUP4 | DO | O | DIO4 | Clock output |

10-bit ADC

| | | | | | | |
|---------------|-----|------|--------|--|------|--------------------------|
| ADC10B_VDDA33 | B13 | SUP3 | Supply | | PS3 | 10-bit ADC analog supply |
| ADC10B_GNDA | A13 | - | Ground | | CG1 | 10-bit ADC analog ground |
| ADC10B_GPA0 | B12 | SUP3 | AI | | AIO1 | 10-bit ADC analog input |
| ADC10B_GPA1 | C13 | SUP3 | AI | | AIO1 | 10-bit ADC analog input |
| ADC10B_GPA2 | C12 | SUP3 | AI | | AIO1 | 10-bit ADC analog input |

Audio ADC

| | | | | | | |
|----------|-----|---|----|--|------|------------------------------|
| ADC_MIC | R15 | - | AI | | AIO2 | ADC microphone input |
| ADC_VINL | T15 | - | AI | | AIO2 | ADC line input left |
| ADC_VINR | R14 | - | AI | | AIO2 | ADC line input right |
| ADC_TINL | P13 | - | AI | | AIO2 | ADC tuner input left |
| ADC_TINR | P14 | - | AI | | AIO2 | ADC tuner input right |
| ADC_VREF | T16 | - | AO | | AIO2 | ADC reference voltage output |

Table 4. Pin description ...continued

Pin names with prefix *m* are multiplexed pins. See [Table 11](#) for pin function selection of multiplexed pins.

| TFBGA pin name | TFB GA ball | Digital I/O level [1] | Application function | Pin state after reset [2] | Cell type [3] | Description |
|---------------------------|-------------|-----------------------|----------------------|---------------------------|---------------|---|
| ADC_VREFN | R16 | - | AI | | AIO2 | ADC negative reference voltage |
| ADC_VREFP | T17 | - | AI | | AIO2 | ADC positive reference voltage |
| ADC_VDDA18 | N15 | SUP2 | Supply | | CS1 | ADC digital voltage supply |
| ADC_VDDA33 | N14 | SUP3 | Supply | | CS1 | ADC analog voltage supply |
| ADC_GNDA | N16 | - | Ground | | CG1 | ADC analog ground |
| Audio Stereo DAC | | | | | | |
| DAC_VDDA33 | C14 | SUP3 | Supply | | CS1 | SDAC analog supply |
| DAC_VREFP | F16 | SUP3 | AI | | AIO2 | SDAC positive reference voltage |
| DAC_VREFN | F15 | - | AI | | AIO2 | SDAC negative reference voltage |
| Class AB amplifier | | | | | | |
| HP_OUTC | D14 | - | AO | | AIO2 | Headphone common output reference for Class AB |
| HP_FCL | C16 | - | AI | | AIO2 | Headphone filter capacitor left |
| HP_FCR | B15 | - | AI | | AIO2 | Headphone filter capacitor right |
| HP_VREF | E14 | - | AI | | AIO2 | Analog reference supply for headphone and DAC |
| HP_OUTL | B17 | - | AO | | AIO2 | Headphone left output |
| HP_OUTR | C15 | - | AO | | AIO2 | Headphone right output |
| HP_VDDA33 | A16 | SUP3 | Supply | | CS1 | Headphone analog supply Class AB |
| HP_GNDA | B16 | - | Ground | | CG1 | Headphone analog ground |
| USB HS 2.0 OTG | | | | | | |
| USB_VBUS | N3 | SUP5 | AI | | AIO3 | USB supply detection line |
| USB_ID | P3 | SUP3 | AI | | AIO1 | Indicates to the USB transceiver whether in device (USB_ID HIGH) or host (USB_ID LOW) mode (contains internal pull-up resistor) |
| USB_RREF | N4 | SUP3 | AIO | | AIO1 | USB connection for external reference resistor (12 kΩ +/- 1%) to analog ground supply |
| USB_DP | T1 | SUP3 | AIO | | AIO1 | USB D+ connection with integrated 45 Ω termination resistor |
| USB_DM | R1 | SUP3 | AIO | | AIO1 | USB D- connection with integrated 45 Ω termination resistor |
| USB_VDDA12_PLL | N2 | SUP1 | Supply | | PS3 | USB PLL supply |
| USB_VDDA33_DRV | T3 | SUP3 | Supply | | PS3 | USB analog supply for driver |
| USB_VDDA33 | R3 | SUP3 | Supply | | PS3 | USB analog supply for PHY |
| USB_VSSA_TERM | R2 | - | Ground | | CG1 | USB analog ground for clean reference for on chip termination resistors |
| USB_GNDA | T2 | - | Ground | | CG1 | USB analog ground |
| USB_VSSA_REF | P2 | - | Ground | | CG1 | USB analog ground for clean reference |

Table 4. Pin description ...continued

Pin names with prefix *m* are multiplexed pins. See [Table 11](#) for pin function selection of multiplexed pins.

| TFBGA pin name | TFBGA ball | Digital I/O level [1] | Application function | Pin state after reset [2] | Cell type [3] | Description |
|--|-------------|-----------------------|----------------------|---------------------------|---------------|--|
| JTAG | | | | | | |
| JTAGSEL | U10 | SUP3 | DI / GPIO | I:PD | DIO1 | JTAG selection. Controls which digital die TAP controller is configured in the JTAG chain along with the analog die TAP controller. Must be LOW during power-on reset. |
| TDI | T10 | SUP3 | DI / GPIO | I:PU | DIO1 | JTAG data Input |
| TRST_N | U11 | SUP3 | DI / GPIO | I:PD | DIO1 | JTAG TAP Controller Reset Input. Must be LOW during power-on reset. |
| TCK | U12 | SUP3 | DI / GPIO | I:PD | DIO1 | JTAG clock input |
| TMS | U9 | SUP3 | DI / GPIO | I:PU | DIO1 | JTAG mode select input |
| TDO | F14 | SUP3 | DO | Z | DIO2 | JTAG data output |
| UART | | | | | | |
| mUART_CTS_N [4][6] | P11 | SUP3 | DI / GPIO | I | DIO1 | UART Clear-To-Send (CTS) (active LOW) |
| mUART_RTS_N [4][6] | R11 | SUP3 | DO / GPIO | O | DIO1 | UART Ready-To-Send (RTS) (active LOW) |
| UART_RXD [4] | R10 | SUP3 | DI / GPIO | I | DIO1 | UART serial input |
| UART_TXD [4] | P10 | SUP3 | DO / GPIO | O | DIO1 | UART serial output |
| I²C master/slave interface | | | | | | |
| I2C_SDA0 | C10 | SUP3 | DIO | I | IICD | I ² C-bus data line |
| I2C_SCL0 | A9 | SUP3 | DIO | I | IICC | I ² C-bus clock line |
| Serial Peripheral Interface (SPI) | | | | | | |
| SPI_CS_OUT0 [4] | D8 | SUP3 | DO | O | DIO4 | SPI chip select output (master) |
| SPI_SCK [4] | C8 | SUP3 | DIO | I | DIO4 | SPI clock input (slave) / clock output (master) |
| SPI_MISO [4] | A8 | SUP3 | DIO | I | DIO4 | SPI data input (master) / data output (slave) |
| SPI_MOSI [4] | B8 | SUP3 | DIO | I | DIO4 | SPI data output (master) / data input (slave) |
| SPI_CS_IN [4] | D9 | SUP3 | DI | I | DIO4 | SPI chip select input (slave) |
| Digital power supply | | | | | | |
| VDDI | J1; U13; A6 | SUP1 | Supply | | CS2 | Digital core supply |
| VDDI_AD | M14 | SUP2 | Supply | | CS2 | Core supply for digital logic on analog die - has to be connected to 1.4/1.8 V rail |
| VSSI | H1; U14; A7 | - | Ground | | CG2 | Digital core ground |
| VSSI_AD | M15 | - | Ground | | CG2 | Digital core ground of analog die |
| Peripheral power supply | | | | | | |
| VDDE_IOA | D1; M1 | SUP4 | Supply | | PS1 | Peripheral supply NAND flash controller |
| VDDE_IOB | L1; U7 | SUP8 | Supply | | PS1 | Peripheral supply LCD interface / SDRAM interface |

Table 4. Pin description ...continuedPin names with prefix *m* are multiplexed pins. See [Table 11](#) for pin function selection of multiplexed pins.

| TFBGA pin name | TFB GA ball | Digital I/O level [1] | Application function | Pin state after reset [2] | Cell type [3] | Description |
|---|---------------------|-----------------------|----------------------|---------------------------|---------------|---|
| VDDE_IOC | U15; A15; A4; | SUP3 | Supply | | PS1 | Peripheral supply |
| VDDE_IOD | G15 | SUP3 | Supply | | PS2 | Analog die peripheral supply |
| VSSE_IOA | E1; N1 | - | Ground | | PG1 | Peripheral ground NAND flash controller |
| VSSE_IOB | K1; U8 | - | Ground | | PG1 | Peripheral ground LCD interface / SDRAM interface |
| VSSE_IOC | U16; A14; A5; | - | Ground | | PG1 | Peripheral ground |
| VSSE_IOD | L14 | - | Ground | | PG2 | Analog die peripheral ground |
| LCD interface | | | | | | |
| mLCD_CSB [4] | R8 | SUP8 | DO | O | DIO4 | LCD chip select (active LOW) |
| mLCD_E_RD [4] | P7 | SUP8 | DO | O | DIO4 | LCD: 6800 enable, 8080 read enable (active HIGH) |
| mLCD_RS [4] | R7 | SUP8 | DO | O | DIO4 | LCD: instruction register (LOW)/ data register (HIGH) select |
| mLCD_RW_WR [4] | T8 | SUP8 | DO | O | DIO4 | LCD: 6800 read/write select, 8080 write enable (active HIGH) |
| mLCD_DB_0 [4] | T7 | SUP8 | DIO | O | DIO4 | LCD Data 0 |
| mLCD_DB_1 [4] | P8 | SUP8 | DIO | O | DIO4 | LCD Data 1 |
| mLCD_DB_2 [4] | T6 | SUP8 | DIO | O | DIO4 | LCD Data 2 |
| mLCD_DB_3 [4] | R6 | SUP8 | DIO | O | DIO4 | LCD Data 3 |
| mLCD_DB_4 [4] | U6 | SUP8 | DIO | O | DIO4 | LCD Data 4 |
| mLCD_DB_5 [4] | P6 | SUP8 | DIO | O | DIO4 | LCD Data 5 |
| mLCD_DB_6 [4] | R5 | SUP8 | DIO | O | DIO4 | LCD Data 6 |
| mLCD_DB_7 [4] | T5 | SUP8 | DIO | O | DIO4 | LCD Data 7 |
| mLCD_DB_8 [4] | U5 | SUP8 | DIO | O | DIO4 | LCD Data 8 / 8-bit Data 0 |
| mLCD_DB_9 [4] | P5 | SUP8 | DIO | O | DIO4 | LCD Data 9 / 8-bit Data 1 |
| mLCD_DB_10 [4] | P4 | SUP8 | DIO | O | DIO4 | LCD Data 10 / 8-bit Data 2 |
| mLCD_DB_11 [4] | U4 | SUP8 | DIO | O | DIO4 | LCD Data 11 / 8-bit Data 3 |
| mLCD_DB_12 [4] | T4 | SUP8 | DIO | O | DIO4 | LCD Data 12 / 8-bit Data 4 / 4-bit Data 0 |
| mLCD_DB_13 [4] | U3 | SUP8 | DIO | O | DIO4 | LCD Data 13 / 8-bit Data 5 / 4-bit Data 1 / serial clock output |
| mLCD_DB_14 [4] | U2 | SUP8 | DIO | O | DIO4 | LCD Data 14 / 8-bit Data 6 / 4-bit Data 2 / serial data input |
| mLCD_DB_15 [4] | R4 | SUP8 | DIO | O | DIO4 | LCD Data 15 / 8-bit Data 7 / 4-bit Data 3 / serial data output |
| I²S/Digital audio input | | | | | | |
| I2SRX_DATA0 [4] | P9 | SUP3 | DI / GPIO | I | DIO1 | I ² S input serial data receive |

Table 4. Pin description ...continued

Pin names with prefix *m* are multiplexed pins. See [Table 11](#) for pin function selection of multiplexed pins.

| TFBGA pin name | TFB GA ball | Digital I/O level [1] | Application function | Pin state after reset [2] | Cell type [3] | Description |
|---|-------------|-----------------------|----------------------|---------------------------|---------------|--|
| I2SRX_BCK0[4] | T9 | SUP3 | DIO / GPIO | I | DIO1 | I ² S input bitclock |
| I2SRX_WSO[4] | R9 | SUP3 | DIO / GPIO | I | DIO1 | I ² S input word select |
| I²S/Digital audio output | | | | | | |
| mI2STX_DATA0[4] | T13 | SUP3 | DO / GPIO | O | DIO1 | I ² S output serial data out |
| mI2STX_BCK0[4] | T12 | SUP3 | DO / GPIO | O | DIO1 | I ² S output bitclock |
| mI2STX_WSO[4] | R12 | SUP3 | DO / GPIO | O | DIO1 | I ² S output word select |
| mI2STX_CLK0[4] | T11 | SUP3 | DO / GPIO | O | DIO1 | I ² S output serial clock |
| General Purpose IO (I/OCONFIG module) | | | | | | |
| GPIO0[8] | R13 | SUP3 | GPIO | I:PD | DIO1 | General Purpose IO pin 0 (mode pin 0) |
| GPIO1[8] | T14 | SUP3 | GPIO | I:PD | DIO1 | General Purpose IO pin 1 (mode pin 1) |
| GPIO2[8] | P12 | SUP3 | GPIO | I | DIO1 | General Purpose IO pin 2 (mode pin 2/blinking LED) |
| GPIO3 | D12 | SUP3 | GPIO | I | DIO1 | General Purpose IO pin 3 (connect to PSU_STOP)[5] |
| GPIO4 | D11 | SUP3 | GPI | I | DIO1 | General Purpose Input pin 4 |
| mGPIO5[4] | D7 | SUP3 | GPIO | I | DIO4 | General Purpose IO pin 5 |
| mGPIO6[4] | B7 | SUP3 | GPIO | I | DIO4 | General Purpose IO pin 6 |
| mGPIO7[4] | C7 | SUP3 | GPIO | I | DIO4 | General Purpose IO pin 7 |
| mGPIO8[4] | D6 | SUP3 | GPIO | I | DIO4 | General Purpose IO pin 8 |
| mGPIO9[4] | B6 | SUP3 | GPIO | I | DIO4 | General Purpose IO pin 9 |
| mGPIO10[4] | C6 | SUP3 | GPIO | I | DIO4 | General Purpose IO pin 10 |
| External Bus Interface (NAND flash controller) | | | | | | |
| EBI_A_0_ALE[4] | C4 | SUP4 | DO | O | DIO4 | EBI Address Latch Enable (ALE) |
| EBI_A_1_CLE[4] | A2 | SUP4 | DO | O | DIO4 | EBI Command Latch Enable (CLE) |
| EBI_D_0[4] | J3 | SUP4 | DIO | I | DIO4 | EBI Data I/O 0 |
| EBI_D_1[4] | H3 | SUP4 | DIO | I | DIO4 | EBI Data I/O 1 |
| EBI_D_2[4] | H4 | SUP4 | DIO | I | DIO4 | EBI Data I/O 2 |
| EBI_D_3[4] | G4 | SUP4 | DIO | I | DIO4 | EBI Data I/O 3 |
| EBI_D_4[4] | F4 | SUP4 | DIO | I | DIO4 | EBI Data I/O 4 |
| EBI_D_5[4] | F3 | SUP4 | DIO | I | DIO4 | EBI Data I/O 5 |
| EBI_D_6[4] | E4 | SUP4 | DIO | I | DIO4 | EBI Data I/O 6 |
| EBI_D_7[4] | E3 | SUP4 | DIO | I | DIO4 | EBI Data I/O 7 |
| EBI_D_8[4] | D3 | SUP4 | DIO | I | DIO4 | EBI Data I/O 8 |
| EBI_D_9[4] | A3 | SUP4 | DIO | I | DIO4 | EBI Data I/O 9 |
| EBI_D_10[4] | C2 | SUP4 | DIO | I | DIO4 | EBI Data I/O 10 |
| EBI_D_11[4] | D2 | SUP4 | DIO | I | DIO4 | EBI Data I/O 11 |
| EBI_D_12[4] | E2 | SUP4 | DIO | I | DIO4 | EBI Data I/O 12 |
| EBI_D_13[4] | F2 | SUP4 | DIO | I | DIO4 | EBI Data I/O 13 |

Table 4. Pin description ...continued

Pin names with prefix *m* are multiplexed pins. See [Table 11](#) for pin function selection of multiplexed pins.

| TFBGA pin name | TFB GA ball | Digital I/O level [1] | Application function | Pin state after reset [2] | Cell type [3] | Description |
|----------------------|-------------|-----------------------|----------------------|---------------------------|---------------|-----------------------------------|
| EBI_D_14 [4] | G2 | SUP4 | DIO | I | DIO4 | EBI Data I/O 14 |
| EBI_D_15 [4] | H2 | SUP4 | DIO | I | DIO4 | EBI Data I/O 15 |
| EBI_DQM_0_NOE [4] | K3 | SUP4 | DO | O | DIO4 | EBI read enable (active LOW) |
| EBI_NWE [4] | K4 | SUP4 | DO | O | DIO4 | EBI write enable (active LOW) |
| NAND_NCS_0 [4] | L2 | SUP4 | DO | O | DIO4 | EBI chip enable 0 |
| NAND_NCS_1 [4] | L3 | SUP4 | DO | O | DIO4 | EBI chip enable 1 |
| NAND_NCS_2 [4] | L4 | SUP4 | DO | O | DIO4 | EBI chip enable 2 |
| NAND_NCS_3 [4] | M2 | SUP4 | DO | O | DIO4 | EBI chip enable 3 |
| mNAND_RYBN0 [4] | B5 | SUP4 | DI | I | DIO4 | EBI NAND ready/busy 0 |
| mNAND_RYBN1 [4] | C5 | SUP4 | DI | I | DIO4 | EBI NAND ready/busy 1 |
| mNAND_RYBN2 [4] | D5 | SUP4 | DI | I | DIO4 | EBI NAND ready/busy 2 |
| mNAND_RYBN3 [4] | D4 | SUP4 | DI | I | DIO4 | EBI NAND ready/busy 3 |
| EBI_NCAS_BLOUT_0 [4] | J2 | SUP4 | DO | O | DIO4 | EBI lower lane byte select (7:0) |
| EBI_NRAS_BLOUT_1 [4] | J4 | SUP4 | DO | O | DIO4 | EBI upper lane byte select (15:8) |

Secure one time programmable memory

| | | | | | | |
|---------|----|---------------|--------|--|-----|---------------------------------|
| VPP [7] | C9 | SUP1/ SUP3 | Supply | | PS3 | Supply for polyfuse programming |
|---------|----|---------------|--------|--|-----|---------------------------------|

Real Time Clock (RTC)

| | | | | | | |
|------------|-----|------|--------|---|------|---|
| RTC_VDD36 | L15 | SUP6 | Supply | | CS1 | RTC supply connected to battery |
| RTC_VSS | M17 | - | Ground | | CG1 | RTC ground |
| FSLOW_OUT | L16 | SUP7 | AO | | AIO2 | RTC 32.768 kHz clock output |
| FSLOW_IN | L17 | SUP7 | AI | | AIO2 | RTC 32.768 kHz clock input |
| RTC_INT | M16 | SUP6 | DO | O | AIO2 | RTC interrupt (HIGH active) |
| RTC_BACKUP | K14 | SUP7 | Supply | | CS1 | RTC backup capacitor connection |
| RTC_CLK32 | U17 | SUP6 | AO | O | AIO2 | RTC 32 kHz clock output for on-board applications such as tuner |

Power supply unit

| | | | | | | |
|----------------|-----|------|--------|---|------|--|
| PSU_VBUS | J16 | SUP5 | Supply | | CS1 | PSU USB supply voltage |
| PSU_VOUT1 | H14 | SUP3 | AO | | CS1 | PSU output1 |
| PSU_LX1 | H15 | - | AIO | | CS1 | PSU external coil terminal for output1 |
| PSU_LX2 | G17 | - | AIO | | CS1 | PSU external coil terminal for output2 |
| PSU_VSS1 | H16 | - | Ground | | CG1 | PSU ground |
| PSU_VIN1 | G16 | - | AI | | CS1 | PSU output1 input voltage |
| PSU_VOUT2 | G14 | SUP1 | AO | | CS1 | PSU output2 |
| PSU_VOUT3 | E17 | SUP2 | AO | | CS1 | PSU output3 |
| PSU_VSSA | D16 | - | Ground | | CG1 | PSU ground |
| PSU_VSSA_CLEAN | D17 | - | Ground | | CG1 | PSU reference circuit ground |
| PSU_PLAY | C17 | SUP3 | AI | I | AIO2 | PSU play button input (active HIGH) |

Table 4. Pin description ...continued

Pin names with prefix *m* are multiplexed pins. See [Table 11](#) for pin function selection of multiplexed pins.

| TFBGA pin name | TFB GA ball | Digital I/O level [1] | Application function | Pin state after reset [2] | Cell type [3] | Description |
|--------------------------------------|-------------|-----------------------|----------------------|---------------------------|---------------|--|
| PSU_STOP | D15 | SUP3 | AIO | I | AIO2 | PSU stop signal input (active HIGH) |
| PSU_VBAT1 | H17 | SUP6 | Supply | | CS1 | PSU DCDC1 supply input |
| PSU_VBAT2 | F17 | SUP6 | Supply | | CS1 | PSU DCDC2 supply input |
| PSU_VBAT | E16 | SUP6 | Supply | | CS1 | PSU Li-ion battery input |
| Li-Ion charger | | | | | | |
| CHARGE_VNTC | J17 | - | AI | | AIO2 | Charger NTC connection |
| CHARGE_VSS | J15 | - | Ground | | CG1 | Charger ground Li-Ion |
| CHARGE_CC_REF | K15 | - | AO | | CS1 | Charger constant current reference |
| CHARGE_VBUS | J14 | SUP5 | Supply | | CS1 | Charger 5 V supply |
| CHARGE_BAT_SENSE | K17 | - | AI | | AIO2 | Charger battery sense terminal |
| CHARGE_VBAT | K16 | SUP6 | AO | | CS1 | Charger positive battery terminal connection |
| USB charge pump (host mode) | | | | | | |
| UOS_VSS | N17 | - | Ground | | CG1 | USB charge pump ground |
| UOS_VBUS | P15 | SUP5 | AO | | CS1 | USB charge pump output to USB_VBUS |
| UOS_VBAT | P16 | SUP6 | Supply | | CS1 | USB charge-pump supply Li-ion battery input |
| UOS_CX2 | P17 | - | AIO | | CS1 | USB charge-pump capacitor terminal for voltage converter |
| UOS_CX1 | R17 | - | AIO | | CS1 | USB charge-pump capacitor terminal for voltage converter |
| Pulse Width Modulation module | | | | | | |
| PWM_DATA [4] | D10 | SUP3 | DO/GPIO | O | DIO1 | PWM output |

[1] Digital IO levels are explained in [Table 5](#).

[2] I = input; I:PU = input with internal weak pull-up; I:PD = input with internal weak pull-down; O = output.

[3] Cell types are explained in [Table 6](#).

[4] Pin can be configured as GPIO pin in the IOCONFIG block.

[5] GPIO3 is driven HIGH if the boot process fails. It is recommended to connect GPIO3 to PSU_STOP, so that the LPC3152/3154 will be powered down and further access prevented if the boot ROM detects an error.

[6] The UART flow control lines (mUART_CTS_N and mUART_RTS_N) are multiplexed. This means that if these balls are not required for UART flow control, they can be selected to be used for their alternative function: SPI chip select signals (SPI_CS_OUT1 and SPI_CS_OUT2).

[7] The polyfuses get unintentionally burned at random if VPP is powered to 2.3 V or greater before the VDDI is powered up to minimum nominal voltage. This will destroy the sample, and it can be locked (security) and the AES key can be corrupted. For this reason it is recommended that VPP be powered by SUP1 at power-on.

[8] To ensure that GPIO0, GPIO1 and GPIO2 pins come up as inputs, pins TRST_N and JTAGSEL must be LOW at power-on reset, see *UM10315 JTAG chapter* for details.

Table 5: Supply domains

| Supply domain | Voltage range | Related supply pins | Description |
|---------------|--|---|--|
| SUP1 | 1.0 V to 1.3 V | VDDI, VDDA12, USB_VDDA12_PLL, VPP (read) | Digital core supply |
| SUP2 | 1.4 V or 1.8 V | VDDI_AD, ADC_VDDA18 | Digital core supply for the analog die functions |
| SUP3 | 2.7 V to 3.6 V | VDDE_IOC, VDDE_IOD, ADC10B_VDDA33, ADC_VDDA33, DAC_VDDA33, HP_VDDA33, USB_VDDA33_DRV, USB_VDDA33, VPP (write) | Peripheral supply |
| SUP4 | 1.65 V to 1.95 V (in 1.8 V mode) 2.5 V to 3.6 V (in 3.3 V mode) | VDDE_IOA | Peripheral supply for NAND flash interface |
| SUP5 | 4.5 V to 5.5 V | PSU_VBUS, CHARGE_VBUS, UOS_VBUS, USB_VBUS | USB VBUS voltage |
| SUP6 | 3.2 V to 4.2 V | RTC_VDD36, PSU_VBAT1, PSU_VBAT2, PSU_VBAT | Li-ion battery voltage |
| SUP7 | 1.8 V | RTC_BACKUP | Real-time clock voltage domain (generated internally from SUP6) |
| SUP8 | 1.65 V to 1.95 V (in 1.8 V mode) 2.5 V to 3.6 V (in 3.3 V mode) | VDDE_IOB | Peripheral supply for SDRAM/SRAM/bus-based LCD [1] |

[1] When the SDRAM is used, the supply voltage of the NAND flash, SDRAM, and the LCD interface must be the same, i.e. SUP4 and SUP8 should be connected to the same rail. (See also [Section 6.28.3](#).)

Table 6: Cell types

| I/O pad name | Type | Function | Description |
|--------------|---------------------|----------------------|--|
| DIO1 | bspts3chp | Digital input/output | Bidirectional 3.3 V; 3-state output; 3 ns slew rate control; plain input; CMOS with hysteresis; programmable pull-up, pull-down, repeater. |
| DIO2 | bpts5pcph | Digital input/output | Bidirectional 5 V; plain input; 3-state output; CMOS with programmable hysteresis; programmable pull-up, pull-down, repeater. |
| DIO3 | bpts5pcph1v8 | Digital input/output | Bidirectional 1.8 V; plain input; 3-state output; CMOS with programmable hysteresis; programmable pull-up, pull-down, repeater. |
| DIO4 | mem1 bsptz40pchn | Digital input/output | Bidirectional 1.8 or 3.3 V; plain input; 3-state output; CMOS with programmable hysteresis; programmable pull-up, pull-down, repeater. |
| IICC | iic3m4scl | Digital input/output | I ² C-bus; clock signal; cell based ESD protection. |
| IICD | iic3mvsda | Digital input/output | I ² C-bus; data signal; cell based ESD protection. |
| AIO1 | apio3v3 | Analog input/output | Analog cell; analog input/output; protection to external 3.3 V supply rail. |
| AIO2 | apio | Analog input/output | Analog pad; analog input/output. |
| AIO3 | apio5v | Analog input/output | Analog cell; analog input/output; 5 V tolerant pad-based ESD protection. |
| CS1 | vddco | Core supply | - |
| CS2 | vddi | Core supply | - |

Table 6: Cell types

| I/O pad name | Type | Function | Description |
|--------------|---------|-------------------|-------------|
| PS1 | vdde3v3 | Peripheral supply | - |
| PS2 | vdde | Peripheral supply | - |
| CG1 | vssco | Core ground | - |
| CG2 | vssis | Core ground | - |
| PG1 | vsse | Peripheral ground | - |

6. Functional description

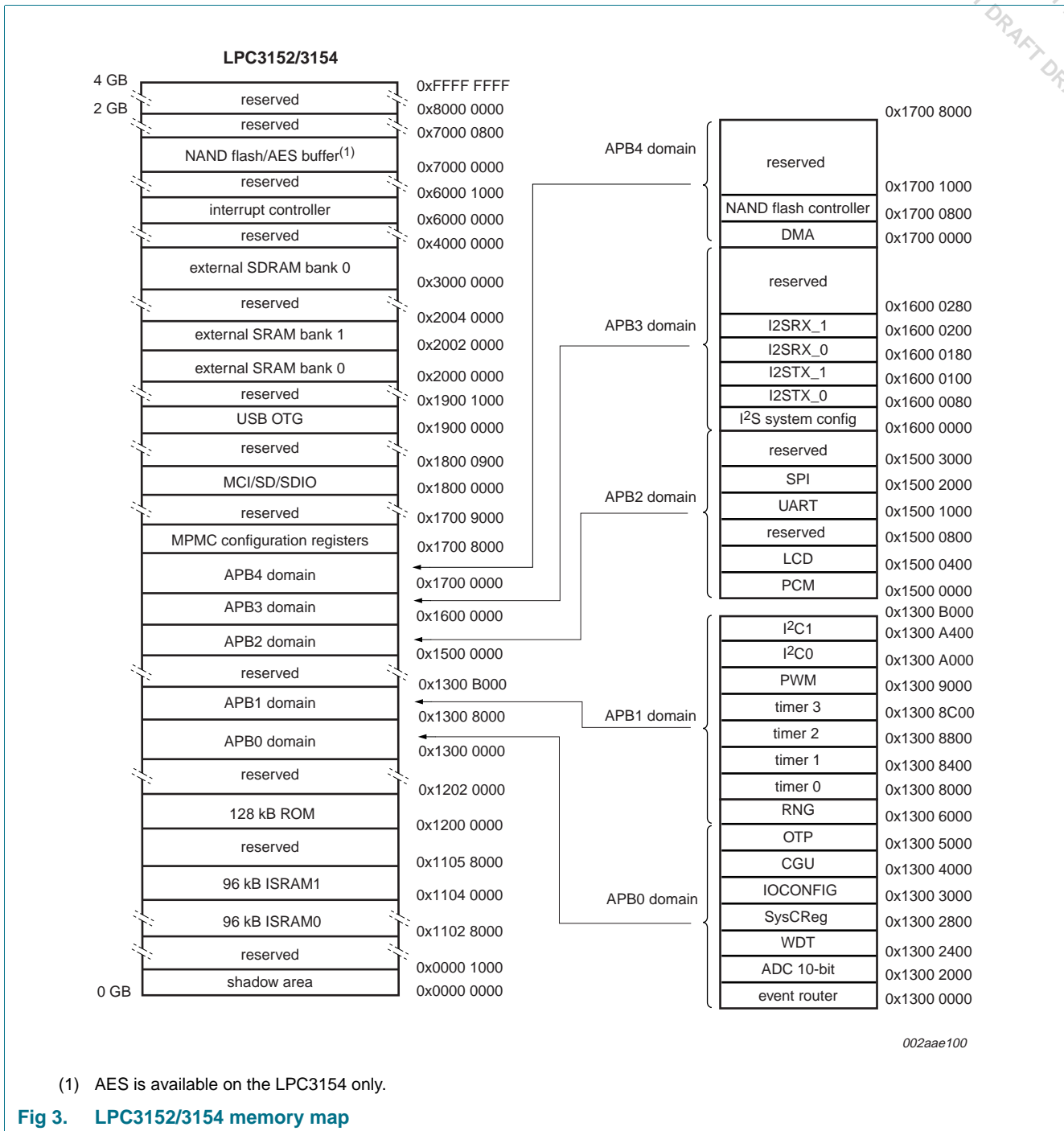
6.1 ARM926EJ-S

The processor embedded in the chip is the ARM926EJ-S. It is a member of the ARM9 family of general-purpose microprocessors. The ARM926EJ-S is intended for multi-tasking applications where full memory management, high performance, and low power are important.

This module has the following features:

- ARM926EJ-S processor core which uses a five-stage pipeline consisting of fetch, decode, execute, memory and write stages. The processor supports both the 32-bit ARM and 16-bit Thumb instruction sets, which allows a trade off between high performance and high code density. The ARM926EJ-S also executes an extended ARMv5TE instruction set which includes support for Java byte code execution.
- Contains an AMBA BIU for both data accesses and instruction fetches.
- Memory Management Unit (MMU).
- 16 kB instruction and 16 kB data separate cache memories with an 8 word line length. The caches are organized using Harvard architecture.
- Little Endian is supported.
- The ARM926EJ-S processor supports the ARM debug architecture and includes logic to assist in both hardware and software debugging.
- Supports dynamic clock gating for power reduction.
- The processor core clock can be set equal to the AHB bus clock or to an integer number times the AHB bus clock. The processor can be switched dynamically between these settings.
- ARM stall support.

6.2 Memory map



6.2.1 Analog die memory organization

The blocks on the analog die (Audio codec, RTC, Li-ion charger, and Power Supply Unit (PSU)) and their registers are accessed through the I²C1-bus interface as a single slave device with device address 0x0C using the following register addresses:

Table 7. Analog die register addresses (I²C1 slave device address 0x0C)

| Block | Address offset |
|--------------------|-----------------|
| PSU/Li-ion charger | 0x0000 - 0x000F |
| Audio codec | 0x0010 - 0x001F |
| RTC | 0x0020 - 0x002F |

6.3 JTAG

The JTAG interface allows the incorporation of the LPC3152/3154 in a JTAG scan chain.

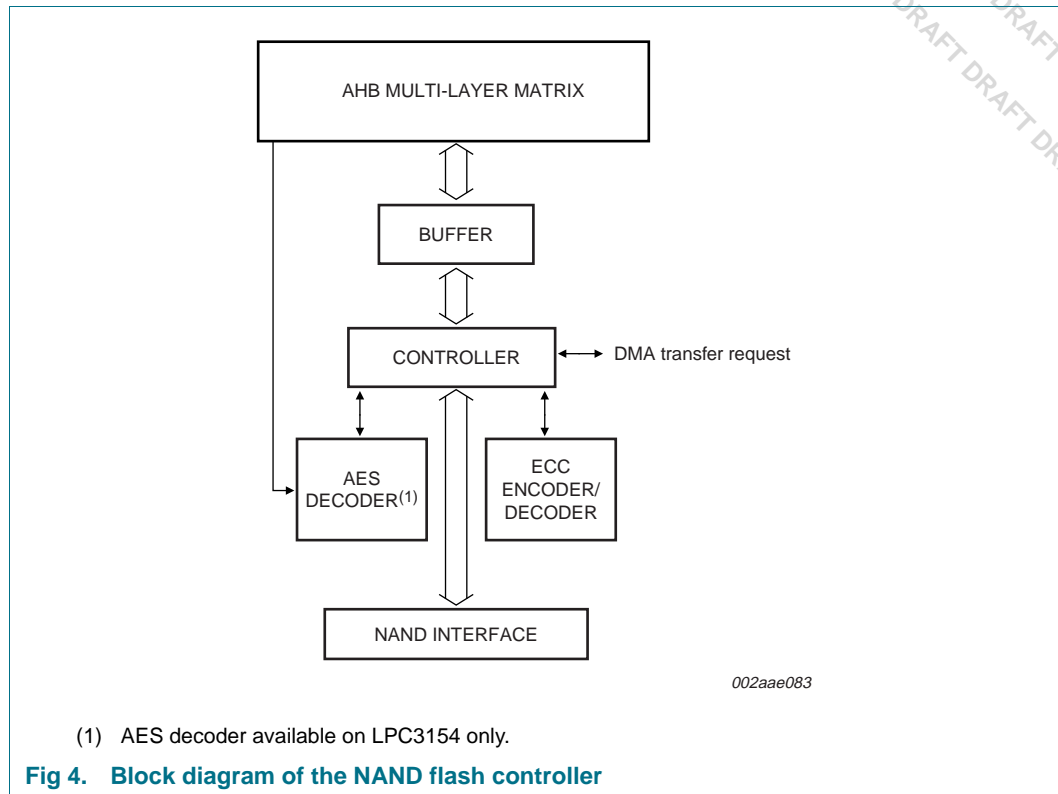
This module has the following features:

- ARM926 debug access
- Boundary scan
- The ARM926 debug access can be permanently disabled through the JTAG security bits in the One-Time Programmable memory (OTP) block.

6.4 NAND flash controller

The NAND flash controller is used as a dedicated interface to NAND flash devices. [Figure 4](#) shows a block diagram of the NAND flash controller module. The heart of the module is formed by a controller block that controls the flow of data from/to the AHB bus through the NAND flash controller block to/from the (external) NAND flash. An error correction encoder/decoder module allows for hardware error correction for support of Multi-Level Cell (MLC) NAND flash devices. In the LPC3154, the NAND flash controller is connected to the AES block to support secure (encrypted) code execution (see [Section 6.21](#)).

Before data is written from the buffer to the NAND flash, optionally it is first protected by an error correction code generated by the ECC module. After data is read from the NAND flash, the error correction module corrects errors, and/or the AES decryption module can decrypt data.



This module has the following features:

- Dedicated NAND flash interface with hardware controlled read and write accesses.
- Wear leveling support with 516-byte mode.
- Software controlled command and address transfers to support wide range of flash devices.
- Software control mode where the ARM is directly master of the flash device.
- Support for 8-bit and 16-bit flash devices.
- Support for any page size from 0.5 kB upwards.
- Programmable NAND flash timing parameters.
- Support for up to four NAND devices.
- Hardware AES decryption (LPC3154 only).
- Error Correction Module (ECC) for MLC NAND flash support:
 - Reed-Solomon error correction encoding and decoding.
 - Uses Reed-Solomon code words with 9-bit symbols over GF(2⁹), a total code word length of 469 symbols, including 10 parity symbols, giving a minimum Hamming distance of 11.
 - Up to 8 symbol errors can be corrected per codeword.
 - Error correction can be turned on and off to match the demands of the application.
 - Parity generator for error correction encoding.
 - Wear leveling information can be integrated into protected data.

- Interrupts generated after completion of error correction task with three interrupt registers.
- Error correction statistics distributed to ARM using interrupt scheme.
- Interface is compatible with the ARM External Bus Interface (EBI).

6.5 Multi-Port Memory Controller (MPMC)

The multi-port memory controller supports the interface to different memory types, for example:

- SDRAM
- Low-power SDRAM
- Static memory interface

This module has the following features:

- Dynamic memory interface support including SDRAM, JEDEC low-power SDRAM.
- Address line supporting up to 128 MB (two 64Mx8 devices connected to a single chip select) of dynamic memory.
- The MPMC has two AHB interfaces:
 - a. an interface for accessing external memory.
 - b. a separate control interface to program the MPMC. This enables the MPMC registers to be situated in memory with other system peripheral registers.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance, particularly for un-cached processors.
- Static memory features include:
 - asynchronous page mode read
 - programmable wait states
 - bus turnaround delay
 - output enable, and write enable delays
 - extended wait
- One chip select for synchronous memory and two chip selects for static memory devices.
- Power-saving modes.
- Dynamic memory self-refresh mode supported.
- Controller support for 2 k, 4 k, and 8 k row address synchronous memory parts.
- Support for all AHB burst types.
- Little and big-endian support.
- Support for the External Bus Interface (EBI) that enables the memory controller pads to be shared.

6.6 External Bus Interface (EBI)

The EBI module acts as multiplexer with arbitration between the NAND flash and the SDRAM/SRAM memory modules connected externally through the MPMC.

The main purpose for using the EBI module is to save external pins. However only data and address pins are multiplexed. Control signals towards and from the external memory devices are not multiplexed.

Table 8. Memory map of the external SRAM/SDRAM memory modules

| Module | Maximum address space | | Data width | Device size |
|-----------------|-----------------------|-------------|------------|-------------|
| External SRAM0 | 0x2000 0000 | 0x2000 FFFF | 8 bit | 64 kB |
| | 0x2000 0000 | 0x2001 FFFF | 16 bit | 128 kB |
| External SRAM1 | 0x2002 0000 | 0x2002 FFFF | 8 bit | 64 kB |
| | 0x2002 0000 | 0x2003 FFFF | 16 bit | 128 kB |
| External SDRAM0 | 0x3000 0000 | 0x37FF FFFF | 16 bit | 128 MB |

6.7 Internal ROM Memory

The internal ROM memory is used to store the boot code of the LPC3152/3154. After a reset, the ARM processor will start its code execution from this memory.

The LPC3154 ROM memory has the following features:

- Supports secure booting from SPI flash, NAND flash, SD/SDHC/MMC cards, UART, and USB (DFU class) interfaces.
- Supports SHA1 hash checking on the boot image.
- Supports un-secure boot from UART and USB (DFU class) interfaces during development. Once the AES key is programmed in the OTP, only secure boot is allowed through UART and USB.
- Supports secure booting from managed NAND devices such as moviNAND, iNAND, eMMC-NAND and eSD-NAND using SD/MMC boot mode.
- Contains pre-defined MMU table (16 kB) for simple systems.

The LPC3152 ROM memory has the following features:

- Supports non-secure booting from SPI flash, NAND flash, SD/SDHC/MMC cards, UART, and USB (DFU class) interfaces.
- Supports option to perform CRC32 checking on the boot image.
- Supports non-secure booting from UART and USB (DFU class) interfaces during development.
- Supports non-secure booting from managed NAND devices such as moviNAND, iNAND, eMMC-NAND and eSD-NAND using SD/MMC boot mode.
- Contains pre-defined MMU table (16 kB) for simple systems.

The boot ROM determines the boot mode based on the reset state of the GPIO0, GPIO1, and GPIO2 pins. To ensure that GPIO0, GPIO1 and GPIO2 pins come up as inputs, pins TRST_N and JTAGSEL must be low during power-on reset, see *UM10315 JTAG chapter* for details.

[Table 9](#) shows the various boot modes supported on the LPC3152/3154. If the boot process fails (e.g. due to tampering with security), the boot code drives pin GPIO3 HIGH. It is recommended to connect the GPIO3 pin to PSU_STOP, so that the LPC3152/3154 will be powered down and further access prevented when the boot ROM detects an error.

Table 9. LPC3152/3154 boot modes

| Boot mode | GPIO0 | GPIO1 | GPIO2 | Description |
|------------|-------|-------|-------|--|
| NAND | 0 | 0 | 0 | Boots from NAND flash. If proper image is not found, boot ROM will switch to DFU boot mode. |
| SPI | 0 | 0 | 1 | Boot from SPI NOR flash connected to SPI_CS_OUT0. If proper image is not found, boot ROM will switch to DFU boot mode. |
| DFU | 0 | 1 | 0 | Device boots via USB using DFU class specification. |
| SD/MMC | 0 | 1 | 1 | Boot ROM searches all the partitions on the SD/MMC/SDHC/MMC+/eMMC/eSD card for boot image. If partition table is missing, it will start searching from sector 0. A valid image is said to be found if a valid image header is found, followed by a valid image. If a proper image is not found, boot ROM will switch to DFU boot mode. |
| Reserved 0 | 1 | 0 | 0 | Reserved for testing. |
| NOR flash | 1 | 0 | 1 | Boot from parallel NOR flash connected to EBI_NSTCS_1. ^[1] |
| UART | 1 | 1 | 0 | Boot ROM tries to download boot image from UART ((115200 – 8 – n – 1) assuming 12 MHz FFAST clock). |
| Test | 1 | 1 | 1 | Boot ROM is testing ISRAM using memory pattern test and basic functionality of the analog audio block. Switches to UART boot mode on receiving three ASCII dots ("...") on UART. |

[1] For security reasons this mode is disabled when JTAG security feature is used.

6.8 Internal RAM memory

The ISRAM (Internal Static Memory Controller) module is used as controller between the AHB bus and the internal RAM memory. The internal RAM memory can be used as working memory for the ARM processor and as temporary storage to execute the code that is loaded by boot ROM from external devices such as SPI-flash, NAND flash and SD/MMC cards.

This module has the following features:

- Capacity of 192 kB
- Implemented as two independent 96 kB memory banks

6.9 Memory Card Interface (MCI)

The MCI controller interface can be used to access memory cards according to the Secure Digital (SD) and Multi-Media Card (MMC) standards. The host controller can be used to interface to small form factor expansion cards compliant to the SDIO card standard as well. Finally, the MCI supports CE-ATA 1.1 compliant hard disk drives.

This module has the following features:

- One 8-bit wide interface.
- Supports high-speed SD, versions 1.01, 1.10 and 2.0.
- Supports SDIO version 1.10.
- Supports MMCplus, MMCmobile, and MMCmicro cards based on MMC 4.1.
- Supports SDHC memory cards.
- CRC generation and checking.
- Supports 1/4-bit SD cards.
- Card detection and write protection.
- FIFO buffers of 16 bytes deep.
- Host pull-up control.
- SDIO suspend and resume.
- 1-byte to 65 535-byte blocks.
- Suspend and resume operations.
- SDIO Read-wait.
- Maximum clock speed of 52 MHz (MMC 4.1).
- Supports CE-ATA 1.1.
- Supports 1-bit, 4-bit, and 8-bit MMC cards and CE-ATA devices.

6.10 Universal Serial Bus 2.0 High Speed On-The-Go (OTG)

The USB OTG module allows the LPC3152/3154 to connect directly to a USB host such as a PC (in device mode) or to a USB device in host mode. In addition, the LPC3152/3154 has a special, built-in mode in which it enumerates as a Device Firmware Upgrade (DFU) class, which allows for a (factory) download of the device firmware through USB.

This module has the following features:

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Contains UTMI+ compliant transceiver (PHY).
- Supports Interrupts.

- This module has its own, integrated DMA engine.

USB-IF TestID for Hi-speed peripheral silicon and embedded host silicon: 40720018

6.11 DMA controller

The DMA Controller can perform DMA transfers on the AHB bus without using the CPU.

This module has the following features:

- Supported transfer types:
 - Memory to memory copy:
 - Memory can be copied from the source address to the destination address with a specified length, while incrementing the address for both the source and destination.
 - Memory to peripheral:
 - Data is transferred from incrementing memory to a fixed address of a peripheral. The flow is controlled by the peripheral.
 - Peripheral to memory:
 - Data is transferred from a fixed address of a peripheral to incrementing memory. The flow is controlled by the peripheral.
- Supports single data transfers for all transfer types.
- Supports burst transfers for memory to memory transfers. A burst always consists of multiples of 4 (32 bit) words.
- The DMA controller has 12 channels.
- Scatter-gather is used to gather data located at different areas of memory. Two channels are needed per scatter-gather action.
- Supports byte, half word and word transfers, and correctly aligns it over the AHB bus.
- Compatible with ARM flow control, for single requests, last single requests, terminal count info, and dma clearing.
- Supports swapping in endianness of the transported data.

Table 10: Peripherals that support DMA access

| Peripheral name | Supported Transfer Types |
|--|---|
| NAND flash controller/AES decryption engine ^[1] | Memory to memory |
| SPI | Memory to peripheral and peripheral to memory |
| MCI | Memory to peripheral and peripheral to memory |
| LCD Interface | Memory to peripheral |
| UART | Memory to peripheral and peripheral to memory |
| I ² C0/1-bus interfaces | Memory to peripheral and peripheral to memory |
| I ² S0/1 receive input | Peripheral to memory |
| I ² S0/1 transmit output | Memory to peripheral |
| PCM interface | Memory to peripheral and peripheral to memory |

[1] AES decryption engine is available on LPC3154 only.

6.12 Interrupt controller

The interrupt controller collects interrupt requests from multiple devices, masks interrupt requests, and forwards the combined requests to the processor. The interrupt controller also provides facilities to identify the interrupt requesting devices to be served.

This module has the following features:

- The interrupt controller decodes all the interrupt requests issued by the on-chip peripherals.
- Two interrupt lines (Fast Interrupt Request (FIQ) and Interrupt Request (IRQ)) to the ARM core. The ARM core supports two distinct levels of priority on all interrupt sources, FIQ for high priority interrupts and IRQ for normal priority interrupts.
- Software interrupt request capability associated with each request input.
- Visibility of interrupts request state before masking.
- Support for nesting of interrupt service routines.
- Interrupts routed to IRQ and to FIQ are vectored.
- Level interrupt support.

The following blocks can generate interrupts:

- NAND flash controller
- USB 2.0 HS OTG
- Event router
- 10 bit ADC
- UART
- LCD int
- MCI
- SPI
- I²C0-bus and I²C1-bus
- Timer 0, timer 1, timer 2, and timer 3
- I²S transmit: I2STX_0 and I2STX_1
- I²S receive: I2SRX_0 and I2SRX_1
- DMA

6.13 Multi-layer AHB

The multi-layer AHB is an interconnection scheme, based on the AHB protocol that enables parallel access paths between multiple masters and slaves in a system.

Multiple masters can have access to different slaves at the same time.

[Figure 5](#) gives an overview of the multi-layer AHB configuration in the LPC3152/3154. AHB masters and slaves are numbered according to their AHB port number.

- Supports all combinations of 32-bit masters and slaves (fully connected interconnect matrix).
- Round-Robin priority mechanism for bus arbitration: all masters have the same priority and get bus access in their natural order
- Four devices on a master port (listed in their natural order for bus arbitration):
 - DMA
 - ARM926 instruction port
 - ARM926 data port
 - USB OTG
- Devices on a slave port (some ports are shared between multiple devices):
 - AHB to APB Bridge 0
 - AHB to APB Bridge 1
 - AHB to APB Bridge 2
 - AHB to APB Bridge 3
 - AHB to APB Bridge 4
 - Interrupt controller
 - NAND flash controller
 - MCI SD/SDIO
 - USB 2.0 HS OTG
 - 96 kB ISRAM0
 - 96 kB ISRAM1
 - 128 kB ROM
 - MPMC (Multi-Purpose Memory Controller)

6.14 APB bridge

The APB Bridge is a bus bridge between AMBA Advanced High-performance Bus (AHB) and the ARM Peripheral Bus (APB) interface.

The module supports two different architectures:

- Single Clock Architecture, synchronous bridge. The same clock is used at the AHB side and at the APB side of the bridge. The AHB-to-APB4 bridge uses this architecture.
- Dual Clock Architecture, asynchronous bridge. Different clocks are used at the AHB side and at the APB side of the bridge. The AHB-to-APB0, AHB-to-APB1, AHB-to-APB2, and AHB-to-APB3 bridges use this architecture.

6.15 Clock Generation Unit (CGU)

The clock generation unit generates all clock signals in the system and controls the reset signals for all modules.

The structure of the CGU is shown in [Figure 6](#). Each output clock generated by the CGU belongs to one of the domains. Each clock domain is fed by a single base clock that originates from one of the available clock sources. Within a clock domain, fractional dividers are available to divide the base clock to a lower frequency.

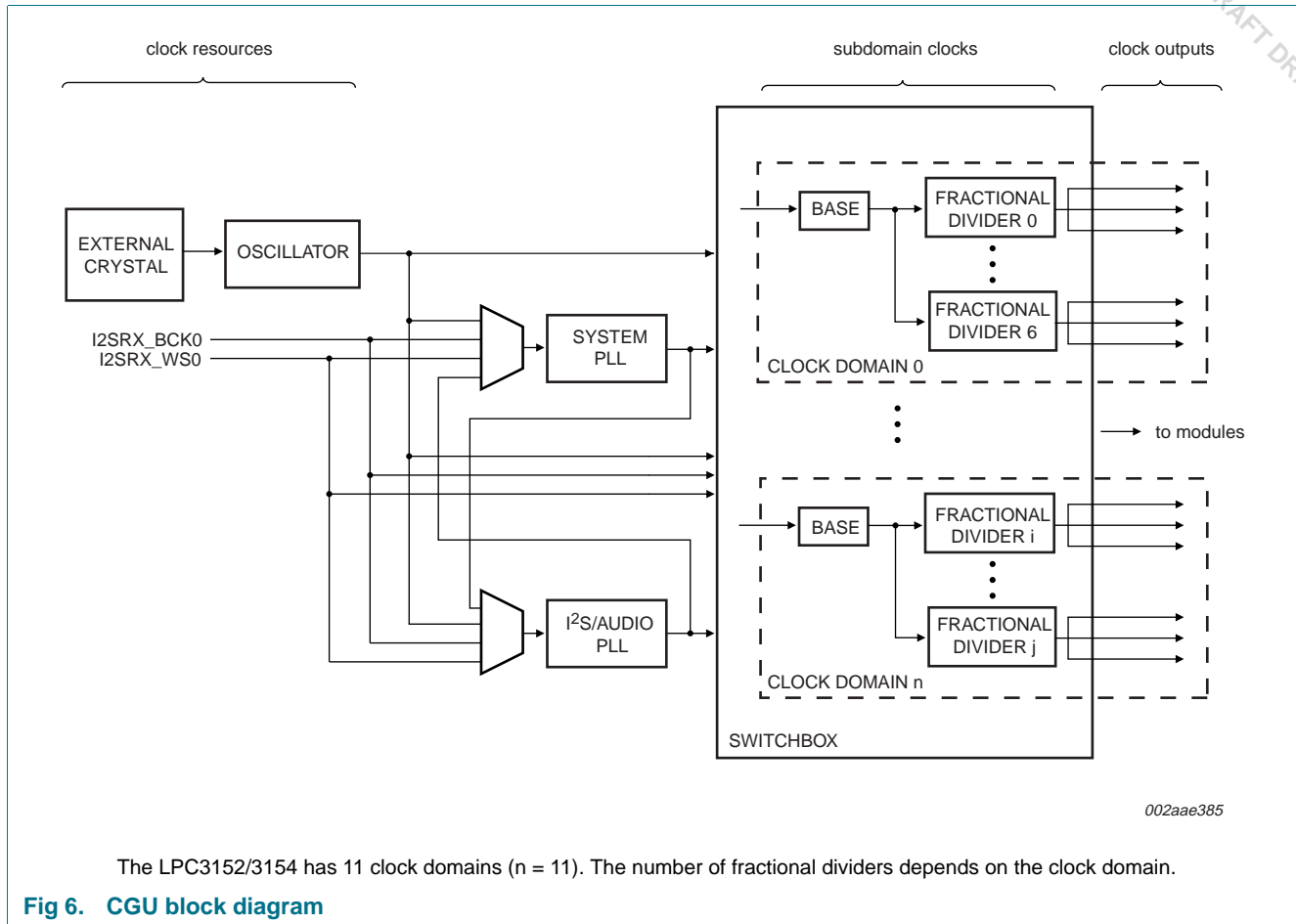
Within most clock domains, the output clocks are again grouped into one or more subdomains. All output clocks within one subdomain are either all generated by the same fractional divider or they are connected directly to the base clock. Therefore all output clocks within one subdomain have the same frequency and all output clocks within one clock domain are synchronous because they originate from the same base clock

The CGU reference clock is generated by the external crystal. Furthermore the CGU has several Phase Locked Loop (PLL) circuits to generate clock signals that can be used for system clocks and/or audio clocks. All clock sources, except the output of the PLLs, can be used as reference input for the PLLs.

This module has the following features:

- Advanced features to optimize the system for low power:
 - All output clocks can be disabled individually for flexible power optimization
 - Some modules have automatic clock gating: they are only active when (bus) access to the module is required.
 - Variable clock scaling for automatic power optimization of the AHB bus (high clock frequency when the bus is active, low clock frequency when the bus is idle).
 - Clock wake-up feature: module clocks can be programmed to be activated automatically on the basis of an event detected by the Event Router (see also [Section 6.19](#)). For example, all clocks (including the ARM /bus clocks) are off and activated automatically when a button is pressed.
- Supports three clock sources:
 - Reference clock generated by the oscillator with an external crystal.
 - Pins I2SRX_BCK0, I2SRX_WS0 are used to input external clock signals (used for generating audio frequencies in I²S receive / I²S transmit slave mode, see also [Section 6.4](#)).
- Two PLLs:
 - System PLL generates programmable system clock frequency from its reference input.
 - Audio PLL generates programmable audio clock frequency (typically $256 \times f_s$) from its reference input.
Remark: Both the System PLL and the audio PLL generate their frequencies based on their (individual) reference clocks. The reference clocks can be programmed to the oscillator clock or one of the external clock signals.
- Highly flexible switchbox to distribute the signals from the clock sources to the module clocks.
 - Each clock generated by the CGU is derived from one of the base clocks and optionally divided by a fractional divider.
 - Each base clock can be programmed to have any one of the clock sources as an input clock.
 - Fractional dividers can be used to divide a base clock by a fractional number to a lower clock frequency.
 - Fractional dividers support clock stretching to obtain a (near) 50% duty cycle output clock.
- Register interface to reset all modules under software control.

- Based on the input of the Watchdog timer (see also [Section 6.16](#)), the CGU can generate a system-wide reset in the case of a system stall.



The LPC3152/3154 has 11 clock domains (n = 11). The number of fractional dividers depends on the clock domain.

Fig 6. CGU block diagram

6.16 Watchdog Timer (WDT)

The Watchdog Timer can be used to generate a system reset if there is a CPU/software crash. In addition the watchdog timer can be used as an ordinary timer. [Figure 7](#) shows how the Watchdog Timer module is connected in the system.

This module has the following features:

- In the event of a software or hardware failure, generates a chip-wide reset request when its programmed time-out period has expired (output m1).
- Watchdog counter can be reset by a periodical software trigger.
- After a reset, a register will indicate whether a reset has occurred because of a watchdog generated reset.
- Watchdog timer can also be used as a normal timer in addition to the watchdog functionality (output m0).

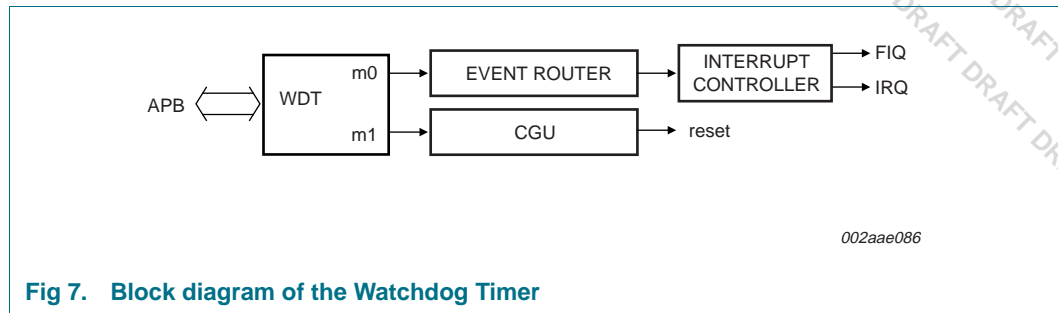


Fig 7. Block diagram of the Watchdog Timer

6.17 Input/Output configuration module (IOCONFIG)

The General Purpose Input/Output (GPIO) pins can be controlled through the register interface provided in the IOCONFIG module. Next to several dedicated GPIO pins, most digital IO pins can also be used as GPIO if they are not required for their normal, dedicated function.

This module has the following features:

- Provides control for the digital pins that can double as GPIO (next to their normal function). The pinning list in [Table 4](#) indicates which pins can double as GPIO.
- Each controlled pin can be configured for 4 operational modes:
 - Normal operation (i.e. controlled by a function block).
 - Driven low.
 - Driven high.
 - High impedance/input.
- A GPIO pin can be observed (read) in any mode.
- The register interface provides set and clear access methods for choosing the operational mode.

6.18 10-bit Analog-to-Digital Converter (ADC10B)

This module is a 10-bit successive approximation Analog-to-Digital Converter (ADC) with an input multiplexer to allow for multiple analog signals on its input. A common use of this module is to read out multiple keys on one input from a resistor network.

This module has the following features:

- Three analog input channels, selected by an analog multiplexer. A fourth channel is connected internally to the analog die to measure the battery level.
- Programmable ADC resolution from 2 bit to 10 bit.
- The maximum conversion rate is 400 ksample/s for 10 bit resolution and 1500 ksample/s for 2 bit resolution.
- Single A/D conversion scan mode and continuous A/D conversion scan mode.
- Power-down mode.

6.19 Event router

The event router extends the interrupt capability of the system by offering a flexible and versatile way of generating interrupts. Combined with the wake-up functionality of the CGU, it also offers a way to wake-up the system from suspend mode (with all clocks deactivated).

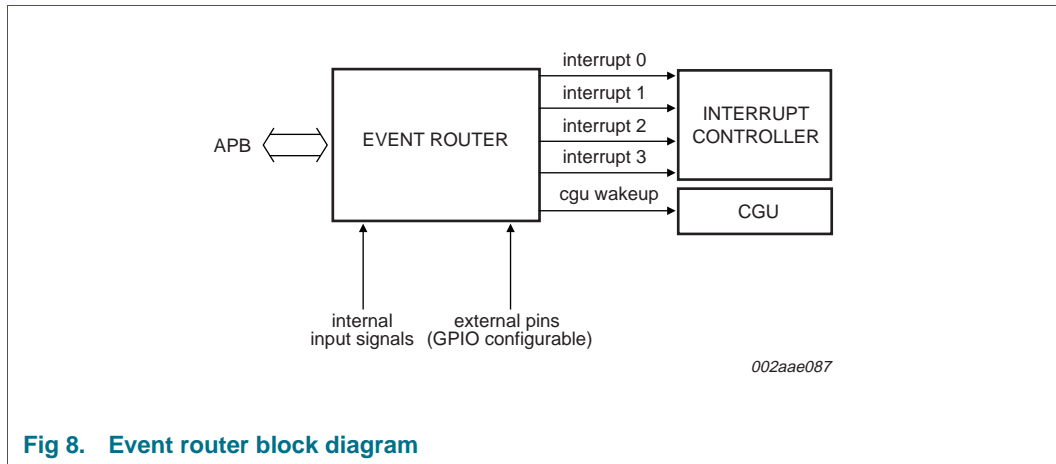


Fig 8. Event router block diagram

The event router has four interrupt outputs connected to the interrupt controller and one wake-up output connected to the CGU as shown in [Figure 8](#). The output signals are activated when an event (for instance a rising edge) is detected on one of the input signals. The input signals of the event router are connected to relevant internal (control) signals in the system or to external signals through pins of the LPC3152/3154.

This module has the following features:

- Provides programmable routing of input events to multiple outputs for use as interrupts or wake up signals.
- Input events can come from internal signals or from the pins that can be used as GPIO.
- Inputs can be used either directly or latched (edge detected) as an event source.
- The active level (polarity) of the input signal for triggering events is programmable.
- Direct events will disappear when the input becomes inactive.
- Latched events will remain active until they are explicitly cleared.
- Each input can be masked globally for all inputs at once.
- Each input can be masked for each output individually.
- Event detect status can be read for each output separately.
- Event detection is fully asynchronous (no active clock required).
- Module can be used to generate a system wake-up from suspend mode.

Remark: All pins that can be used as GPIO are connected to the event router (see [Figure 8](#)). Note that they can be used to trigger events when in normal, functional mode or in GPIO mode.

6.20 Random Number Generator (RNG)

The random number generator generates true random numbers for use in advanced security and Digital Rights Management (DRM) related schemes. These schemes rely upon truly random, i.e. completely unpredictable numbers.

This module has the following features:

- True random number generator.
- The random number register does not rely on any kind of reset.
- The generators are free running in order to ensure randomness and security.

6.21 AES decryption (LPC3154 only)

This module can be used for data decryption using the AES algorithm. The AES module has the following features:

- AES-128: 128 bit key, 128 bit data.
- CBC mode over blocks of 512 bytes.
- Each block of 512 bytes uses the same initial value.
- AES can be turned on and off.

6.22 Secure One-Time Programmable (OTP) memory

The OTP memory can be used for storing non-volatile information like serial number, security bits, etc. It consists of a polyfuse array, embedded data registers, and control registers. One of the main purposes of the OTP is storing a security key and a unique ID.

This module has the following features:

- 512-bit, one-time programmable memory
 - 128 bit are used for an unique ID which is pre-programmed in the wafer fab.
 - 40 bit are used for security and other features which are programmed at the customer production line.
 - 184 bit are available for customer use.
 - 32 bit are used for USB product ID and vendor ID by boot ROM in DFU mode.
 - 128 bit are for the secure key used by boot ROM to load secure images.

Remark: On the LPC3152 secure boot is not supported hence these bits are also available for customer use.

- Programmable at the customer production line
- Random read access via sixteen 32-bit registers
- Flexible read protection mechanism to hide security related data
- Flexible write protection mechanism

6.23 Serial Peripheral Interface (SPI)

The SPI module is used for synchronous serial data communication with other devices which support the SPI/SSI protocol. Examples of the devices that this SPI module can communicate with are memories, cameras, and WiFi-g.

The SPI/SSI-bus is a 5-wire interface, and it is suitable for low, medium, and high data rate transfers.

This module has the following features:

- Supports Motorola SPI frame format with a word size of 8/16 bits.
- Texas Instruments SSI (Synchronous Serial Interface) frame format with a word size of 4 bit to 16 bit.
- Receive FIFO and transmit FIFO of 64 half-words each.
- Serial clock rate master mode maximum 45 MHz.
- Serial clock rate slave mode maximum 25 MHz.
- Support for single data access DMA.
- Full-duplex operation.
- Supports up to three slaves.
- Supports maskable interrupts.
- Supports DMA transfers.

6.24 Universal Asynchronous Receiver Transmitter (UART)

The UART module supports the industry standard serial interface.

This module has the following features:

- Programmable baud rate with a maximum of 1049 kBd.
- Programmable data length (5 bit to 8 bit).
- Implements only asynchronous UART.
- Transmit break character length indication.
- Programmable one to two stops bits in transmission.
- Odd/even/force parity check/generation.
- Frame error, overrun error and break detection.
- Automatic hardware flow control.
- Independent control of transmit, receive, line status, data set interrupts, and FIFOs.
- SIR-IrDA encoder/decoder (from 2400 to 115 kBd).
- Supports maskable interrupts.
- Supports DMA transfers.

6.25 Pulse Code Modulation (PCM) interface

The PCM interface supports the PCM and IOM interfaces.

This module has the following features:

- Four-wire serial interface.
- Can function in both Master and Slave modes.
- Supports:
 - MP PCM (Multi-Protocol PCM): Configurable directional per slot.

- PCM (Pulse Code Modulation): Single clocking physical format.
- IOM-2 (Extended ISDN-Oriented modular): Double clocking physical format.
- Twelve 8 bit slots in a frame with enabling control per slot.
- Internal frame clock generation in master mode.
- Receive and transmit DMA handshaking using a request/clear protocol.
- Interrupt generation per frame.

PCM is a very common method used for transmitting analog data in digital format. Most common applications of PCM are digital audio as in audio CDs and computers, digital telephony, and digital videos.

The IOM (ISDN Oriented Modular) interface is primarily used to interconnect telecommunications ICs providing ISDN compatibility. It delivers a symmetrical full-duplex communication link containing user data, control/programming lines, and status channels.

6.26 LCD interface

The LCD interface contains logic to interface to a 6800 (Motorola) or 8080 (Intel) compatible LCD controller which supports 4/8/16 bit modes. This module also supports a serial interface mode. The speed of the interface can be adjusted in software to match the speed of the connected LCD display.

This module has the following features:

- 4/8/16 bit parallel interface mode: 6800-series, 8080-series.
- Serial interface mode.
- Supports multiple frequencies for the 6800/8080 bus to support high- and low-speed controllers.
- Supports polling the busy flag from LCD controller to off-load the CPU from polling.
- Contains an 16 byte FIFO for sending control and data information to the LCD controller.
- Supports maskable interrupts.
- Supports DMA transfers.

6.27 I²C-bus master/slave interface

The LPC3152/3154 contains two I²C master/slave interfaces. I²C-bus 0 can be used for communicating directly with I²C-compatible external devices. I²C-bus 1 is internally connected to support the following analog blocks: Li-ion charger, power supply unit, RTC, audio ADC, audio DAC, and class AB amplifier.

This module has the following features:

- **I²C0 interface:** I²C0 is a standard I²C-compliant bus interface with open-drain pins. This interface supports functions described in the I²C specification for speeds up to 400 kHz. This includes multi-master operation and allows powering off this device in a working system while leaving the I²C-bus functional.
- **I²C1 interface:** internally connected to control the functions on the analog die.
- Supports normal mode (100 kHz SCL).

- Fast mode (400 kHz SCL with 24 MHz APB clock; 325 kHz with 12 MHz APB clock; 175 kHz with 6 MHz APB clock).
- Interrupt support.
- Supports DMA transfers (single).
- Four modes of operation:
 - Master transmitter
 - Master receiver
 - Slave transmitter
 - Slave receiver

6.28 LCD/NAND flash/SDRAM multiplexing

The LPC3152/3154 contains a rich set of specialized hardware interfaces, but the TFBGA package does not contain enough pins to allow use of all signals of all interfaces simultaneously. Therefore a pin-multiplexing scheme is implemented, which allows the selection of the right interface for the application.

Pin multiplexing is enabled between the following interfaces:

- between the dedicated LCD interface and the External Bus Interface (EBI).
- between the NAND flash controller and the Memory Card Interface (MCI).
- between UART and SPI.
- between I2STX_0 output and the PCM interface.

The pin interface multiplexing is subdivided into five categories: storage, video, audio, NAND flash, and UART related pin multiplexing. Each category supports several modes, which can be selected by programming the corresponding registers in the SysCReg.

6.28.1 Pin connections

Table 11. Pin descriptions of multiplexed pins

| Pin name | Default signal | Alternate signal | Description |
|---------------------------------------|----------------|------------------|--|
| Video related pin multiplexing | | | |
| mLCD_CSB | LCD_CSB | EBI_NSTCS_0 | LCD_CSB — LCD chip select for external LCD controller. EBI_NSTCS_0 — EBI static memory chip select 0. |
| mLCD_DB_1 | LCD_DB_1 | EBI_NSTCS_1 | LCD_DB_1 — LCD bidirectional data line 1. EBI_NSTCS_1 — EBI static memory chip select 1. |
| mLCD_DB_0 | LCD_DB_0 | EBI_CLKOUT | LCD_DB_0 — LCD bidirectional data line 0. EBI_CLKOUT — EBI SDRAM clock signal. |
| mLCD_E_RD | LCD_E_RD | EBI_CKE | LCD_E_RD — LCD enable/read signal. EBI_CKE — EBI SDRAM clock enable. |
| mLCD_RS | LCD_RS | EBI_NDYCS | LCD_RS — LCD register select signal. EBI_NDYCS — EBI SDRAM chip select. |
| mLCD_RW_WR | LCD_RW_WR | EBI_DQM_1 | LCD_RW_WR — LCD read write/write signal. EBI_DQM_1 — EBI SDRAM data mask output 1. |
| mLCD_DB_2 | LCD_DB_2 | EBI_A_2 | LCD_DB_2 — LCD bidirectional data line 2. EBI_A_2 — EBI address line 2. |

Table 11. Pin descriptions of multiplexed pins

| Pin name | Default signal | Alternate signal | Description |
|------------|----------------|------------------|--|
| mLCD_DB_3 | LCD_DB_3 | EBI_A_3 | LCD_DB_3 — LCD bidirectional data line 3. EBI_A_3 — EBI address line 3. |
| mLCD_DB_4 | LCD_DB_4 | EBI_A_4 | LCD_DB_4 — LCD bidirectional data line 4. EBI_A_4 — EBI address line 4. |
| mLCD_DB_5 | LCD_DB_5 | EBI_A_5 | LCD_DB_5 — LCD bidirectional data line 5. EBI_A_5 — EBI address line 5. |
| mLCD_DB_6 | LCD_DB_6 | EBI_A_6 | LCD_DB_6 — LCD bidirectional data line 6. EBI_A_6 — EBI address line 6. |
| mLCD_DB_7 | LCD_DB_7 | EBI_A_7 | LCD_DB_7 — LCD bidirectional data line 7. EBI_A_7 — EBI address line 7. |
| mLCD_DB_8 | LCD_DB_8 | EBI_A_8 | LCD_DB_8 — LCD bidirectional data line 8. EBI_A_8 — EBI address line 8. |
| mLCD_DB_9 | LCD_DB_9 | EBI_A_9 | LCD_DB_9 — LCD bidirectional data line 9. EBI_A_9 — EBI address line 9. |
| mLCD_DB_10 | LCD_DB_10 | EBI_A_10 | LCD_DB_10 — LCD bidirectional data line 10. EBI_A_10 — EBI address line 10. |
| mLCD_DB_11 | LCD_DB_11 | EBI_A_11 | LCD_DB_11 — LCD bidirectional data line 11. EBI_A_11 — EBI address line 11. |
| mLCD_DB_12 | LCD_DB_12 | EBI_A_12 | LCD_DB_12 — LCD bidirectional data line 12. EBI_A_12 — EBI address line 12. |
| mLCD_DB_13 | LCD_DB_13 | EBI_A_13 | LCD_DB_13 — LCD bidirectional data line 13. EBI_A_13 — EBI address line 13. |
| mLCD_DB_14 | LCD_DB_14 | EBI_A_14 | LCD_DB_14 — LCD bidirectional data line 14. EBI_A_14 — EBI address line 14. |
| mLCD_DB_15 | LCD_DB_15 | EBI_A_15 | LCD_DB_15 — LCD bidirectional data line 15. EBI_A_15 — EBI address line 15. |

Storage related pin multiplexing

| | | | |
|---------|--------|-----------|--|
| mGPIO5 | GPIO5 | MCI_CLK | GPIO5 — General Purpose I/O pin 5. MCI_CLK — MCI card clock. |
| mGPIO6 | GPIO6 | MCI_CMD | GPIO_6 — General Purpose I/O pin 6. MCI_CMD — MCI card command input/output. |
| mGPIO7 | GPIO7 | MCI_DAT_0 | GPIO7 — General Purpose I/O pin 7. MCI_DAT_0 — MCI card data input/output line 0. |
| mGPIO8 | GPIO8 | MCI_DAT_1 | GPIO8 — General Purpose I/O pin 8. MCI_DAT_1 — MCI card data input/output line 1. |
| mGPIO9 | GPIO9 | MCI_DAT_2 | GPIO9 — General Purpose I/O pin 9. MCI_DAT_2 — MCI card data input/output line 2. |
| mGPIO10 | GPIO10 | MCI_DAT_3 | GPIO10 — General Purpose I/O pin 10. MCI_DAT_3 — MCI card data input/output line 3. |

Table 11. Pin descriptions of multiplexed pins

| Pin name | Default signal | Alternate signal | Description |
|------------|----------------|------------------|--|
| mLCD_DB_3 | LCD_DB_3 | EBI_A_3 | LCD_DB_3 — LCD bidirectional data line 3. EBI_A_3 — EBI address line 3. |
| mLCD_DB_4 | LCD_DB_4 | EBI_A_4 | LCD_DB_4 — LCD bidirectional data line 4. EBI_A_4 — EBI address line 4. |
| mLCD_DB_5 | LCD_DB_5 | EBI_A_5 | LCD_DB_5 — LCD bidirectional data line 5. EBI_A_5 — EBI address line 5. |
| mLCD_DB_6 | LCD_DB_6 | EBI_A_6 | LCD_DB_6 — LCD bidirectional data line 6. EBI_A_6 — EBI address line 6. |
| mLCD_DB_7 | LCD_DB_7 | EBI_A_7 | LCD_DB_7 — LCD bidirectional data line 7. EBI_A_7 — EBI address line 7. |
| mLCD_DB_8 | LCD_DB_8 | EBI_A_8 | LCD_DB_8 — LCD bidirectional data line 8. EBI_A_8 — EBI address line 8. |
| mLCD_DB_9 | LCD_DB_9 | EBI_A_9 | LCD_DB_9 — LCD bidirectional data line 9. EBI_A_9 — EBI address line 9. |
| mLCD_DB_10 | LCD_DB_10 | EBI_A_10 | LCD_DB_10 — LCD bidirectional data line 10. EBI_A_10 — EBI address line 10. |
| mLCD_DB_11 | LCD_DB_11 | EBI_A_11 | LCD_DB_11 — LCD bidirectional data line 11. EBI_A_11 — EBI address line 11. |
| mLCD_DB_12 | LCD_DB_12 | EBI_A_12 | LCD_DB_12 — LCD bidirectional data line 12. EBI_A_12 — EBI address line 12. |
| mLCD_DB_13 | LCD_DB_13 | EBI_A_13 | LCD_DB_13 — LCD bidirectional data line 13. EBI_A_13 — EBI address line 13. |
| mLCD_DB_14 | LCD_DB_14 | EBI_A_14 | LCD_DB_14 — LCD bidirectional data line 14. EBI_A_14 — EBI address line 14. |
| mLCD_DB_15 | LCD_DB_15 | EBI_A_15 | LCD_DB_15 — LCD bidirectional data line 15. EBI_A_15 — EBI address line 15. |

Storage related pin multiplexing

| | | | |
|---------|--------|-----------|--|
| mGPIO5 | GPIO5 | MCI_CLK | GPIO5 — General Purpose I/O pin 5. MCI_CLK — MCI card clock. |
| mGPIO6 | GPIO6 | MCI_CMD | GPIO_6 — General Purpose I/O pin 6. MCI_CMD — MCI card command input/output. |
| mGPIO7 | GPIO7 | MCI_DAT_0 | GPIO7 — General Purpose I/O pin 7. MCI_DAT_0 — MCI card data input/output line 0. |
| mGPIO8 | GPIO8 | MCI_DAT_1 | GPIO8 — General Purpose I/O pin 8. MCI_DAT_1 — MCI card data input/output line 1. |
| mGPIO9 | GPIO9 | MCI_DAT_2 | GPIO9 — General Purpose I/O pin 9. MCI_DAT_2 — MCI card data input/output line 2. |
| mGPIO10 | GPIO10 | MCI_DAT_3 | GPIO10 — General Purpose I/O pin 10. MCI_DAT_3 — MCI card data input/output line 3. |

Table 11. Pin descriptions of multiplexed pins

| Pin name | Default signal | Alternate signal | Description |
|--|----------------|------------------|---|
| NAND flash related pin multiplexing | | | |
| mNAND_RYBN0 | NAND_RYBN0 | MCI_DAT_4 | NAND_RYBN0 — NAND flash controller Read/Not busy signal 0. MCI_DAT_4 — MCI card data input/output line 4. |
| mNAND_RYBN1 | NAND_RYBN1 | MCI_DAT_5 | NAND_RYBN1 — NAND flash controller Read/Not busy signal 1. MCI_DAT_5 — MCI card data input/output line 5. |
| mNAND_RYBN2 | NAND_RYBN2 | MCI_DAT_6 | NAND_RYBN2 — NAND flash controller Read/Not busy signal 2. MCI_DAT_6 — MCI card data input/output line 6. |
| mNAND_RYBN3 | NAND_RYBN3 | MCI_DAT_7 | NAND_RYBN3 — NAND flash controller Read/Not busy signal 3. MCI_DAT_7 — MCI card data input/output line 7. |
| Audio related pin multiplexing | | | |
| ml2STX_DATA0 | I2STX_DATA0 | PCM_DA | I2STX_DATA0 — I2S interface 0 transmit data signal. PCM_DA — PCM serial data line A. |
| ml2STX_BCK0 | I2STX_BCK0 | PCM_FSC | I2STX_BCK0 — I2S interface 0 transmit bitclock signal. PCM_FSC — PCM frame synchronization signal. |
| ml2STX_WS0 | I2STX_WS0 | PCM_DCLK | I2STX_WS0 — I2S interface 0 transmit word select signal. PCM_DCLK — PCM data clock output. |
| ml2STX_CLK0 | I2STX_CLK0 | PCM_DB | I2STX_CLK0 — I2S interface 0 transmit clock signal. PCM_DB — PCM serial data line B. |
| UART related pin multiplexing | | | |
| mUART_CTS_N | UART_CTS_N | SPI_CS_OUT1 | UART_CTS_N — UART modem control Clear-to-Send signal. SPI_CS_OUT1 — SPI chip select out for slave 1 (used in master mode). |
| mUART_RTS_N | UART_RTS_N | SPI_CS_OUT2 | UART_RTS_N — UART modem control Request-to-Send signal. SPI_CS_OUT2 — SPI chip select out for slave 2 (used in master mode). |

6.28.2 Multiplexing between LCD and MPMC

The multiplexing between the LCD interface and MPMC allows for the following two modes of operation:

- MPMC-mode: SDRAM and bus-based LCD or SRAM.
- LCD-mode: Dedicated LCD-Interface.

The external NAND flash is accessible in both modes.

The block diagram [Figure 9](#) gives a high level overview of the modules in the chip that are involved in the pin interface multiplexing between the EBI, NAND flash controller, MPMC, and RAM-based LCD interface.

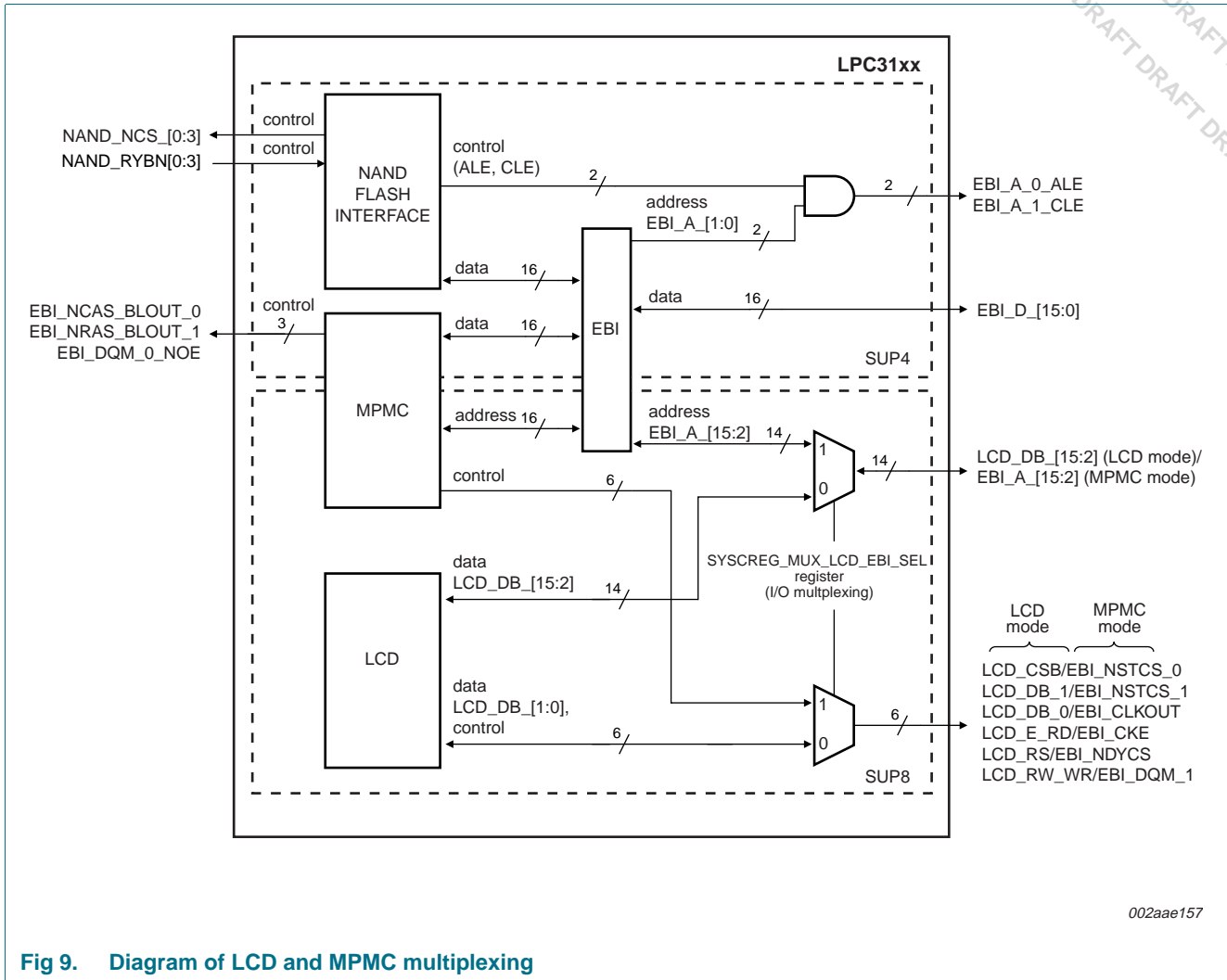


Fig 9. Diagram of LCD and MPMC multiplexing

Figure 9 only shows the signals that are involved in pad-muxing, so not all interface signals are visible.

The EBI unit between the NAND flash interface and the MPMC contains an arbiter that determines which interface is muxed to the outside world. Both NAND flash and SDRAM/SRAM initiate a request to the EBI unit. This request is granted using round-robin arbitration (see Section 6.6).

6.28.3 Supply domains

As is shown in Figure 9 the EBI (NAND flash/MPMC-control/data) is connected to a different supply domain than the LCD interface. The EBI control and address signals are muxed with the LCD interface signals and are part of supply domain SUP8. The SDRAM/SRAM data lines are shared with the NAND flash through the EBI and are part of supply domain SUP4. Therefore the following rules apply for connecting memories:

1. SDRAM and bus-based LCD or SRAM: This is the MPMC mode. The supply voltage for SDRAM/SRAM/bus-based LCD and NAND flash must be the same. The dedicated LCD interface is not available in this MPMC mode.

2. Dedicated LCD interface only: This is the LCD mode. The NAND flash supply voltage (SUP4) can be different from the LCD supply voltage (SUP8).

6.29 Timer module

The LPC3152/3154 contains four fully independent timer modules, which can be used to generate interrupts after a pre-set time interval has elapsed.

This module has the following features:

- Each timer is a 32 bit wide down-counter with selectable pre-scale. The pre-scaler allows using either the module clock directly or the clock divided by 16 or 256.
- Two modes of operation:
 - Free-running timer: The timer generates an interrupt when the counter reaches zero. The timer wraps around to 0xFFFF FFFF and continues counting down.
 - Periodic timer: The timer generates an interrupt when the counter reaches zero. It reloads the value from a load register and continues counting down from that value. An interrupt will be generated every time the counter reaches zero. This effectively gives a repeated interrupt at a regular interval.
- At any time the current timer value can be read.
- At any time the value in the load register may be re-written, causing the timer to restart.

6.30 Pulse Width Modulation (PWM) module

This PWM can be used to generate a pulse width modulated or a pulse density modulated signal. With an external low pass filter, the module can be used to generate a low frequent analog signal. A typical use of the output of the module is to control the backlight of an LCD display.

This module has the following features:

- Supports Pulse Width Modulation (PWM) with software controlled duty cycle.
- Supports Pulse Density Modulation (PDM) with software controlled pulse density.

6.31 System control registers

The System Control Registers (SysCReg) module provides a register interface for some of the high-level settings in the system such as multiplexers and mode settings. This is an auxiliary module included in this overview for the sake of completeness.

6.32 Audio Subsystem (ADSS)

The audio subsystem consists of the following blocks:

- I²S interfaces on the digital die (see [Section 6.32.1](#)):
 - I²S0 digital audio input/output (I2SRX_0/I2STX_0)
 - I²S1 (I2SRX_1/I2STX_1) interface to the audio analog block (I²S1 signals not pinned out)
 - Edge detector

- Audio codec on the analog die (see [Section 7.2](#)):
 - Class AB amplifier
 - Stereo Analog-to-Digital Converter (SADC)
 - analog inputs/outputs
 - Analog Volume Control (AVC)
 - Stereo Digital-to-Analog Converter (SDAC)
- I²S and I²C interfaces on the analog die for communication with the digital die.

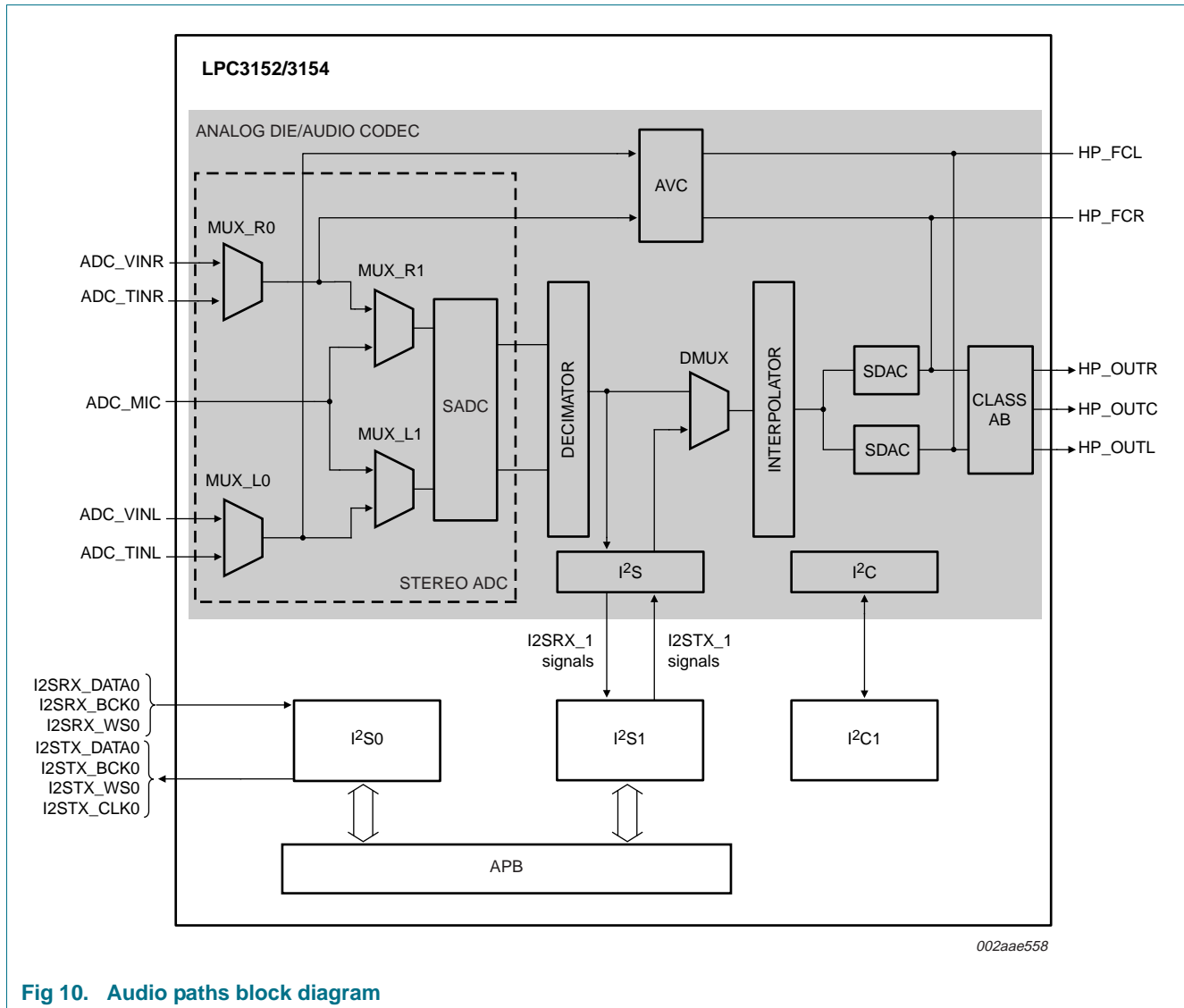


Fig 10. Audio paths block diagram

6.32.1 I²S0/1 digital audio input/output

The I²S0/1 audio module provides a 3-wire digital audio interface that complies with the I²S standard.

Remark: In the LPC3152/3154, the I²S0 interface is pinned out. The I²S1 interface is internally connected to the analog die.

The I²S0/1 module has the following features:

- Receive input supports master mode and slave mode.
- Transmit output supports master mode.
- Supports LSB justified words of 16, 18, 20 and 24 bits.
- Supports a configurable number of bit clock periods per word select period (up to 128 bit clock periods).
- Supports DMA transfers.
- Transmit FIFO or receive FIFO of 4 stereo samples.
- Supports single 16-bit transfers to/from the left or right FIFO.
- Supports single 24-bit transfers to/from the left or right FIFO.
- Supports 32-bit interleaved transfers, with the lower 16 bits representing the left audio sample and the higher 16 bits representing the right audio sample.
- Supports two 16-bit samples audio samples combined in a 32-bit word (2 left or 2 right samples) to reduce bus load.
- Provides maskable interrupts for audio status.
(FIFO underrun/overrun/full/half_full/not empty for left and right channel separately).

7. Functional description of the analog die blocks

7.1 Analog die

The analog die part of the LPC3152/3154 contains the audio codec, the Real-Time Clock (RTC), the Power Supply Unit (PSU), the Li-ion charger, and the USB charge pump.

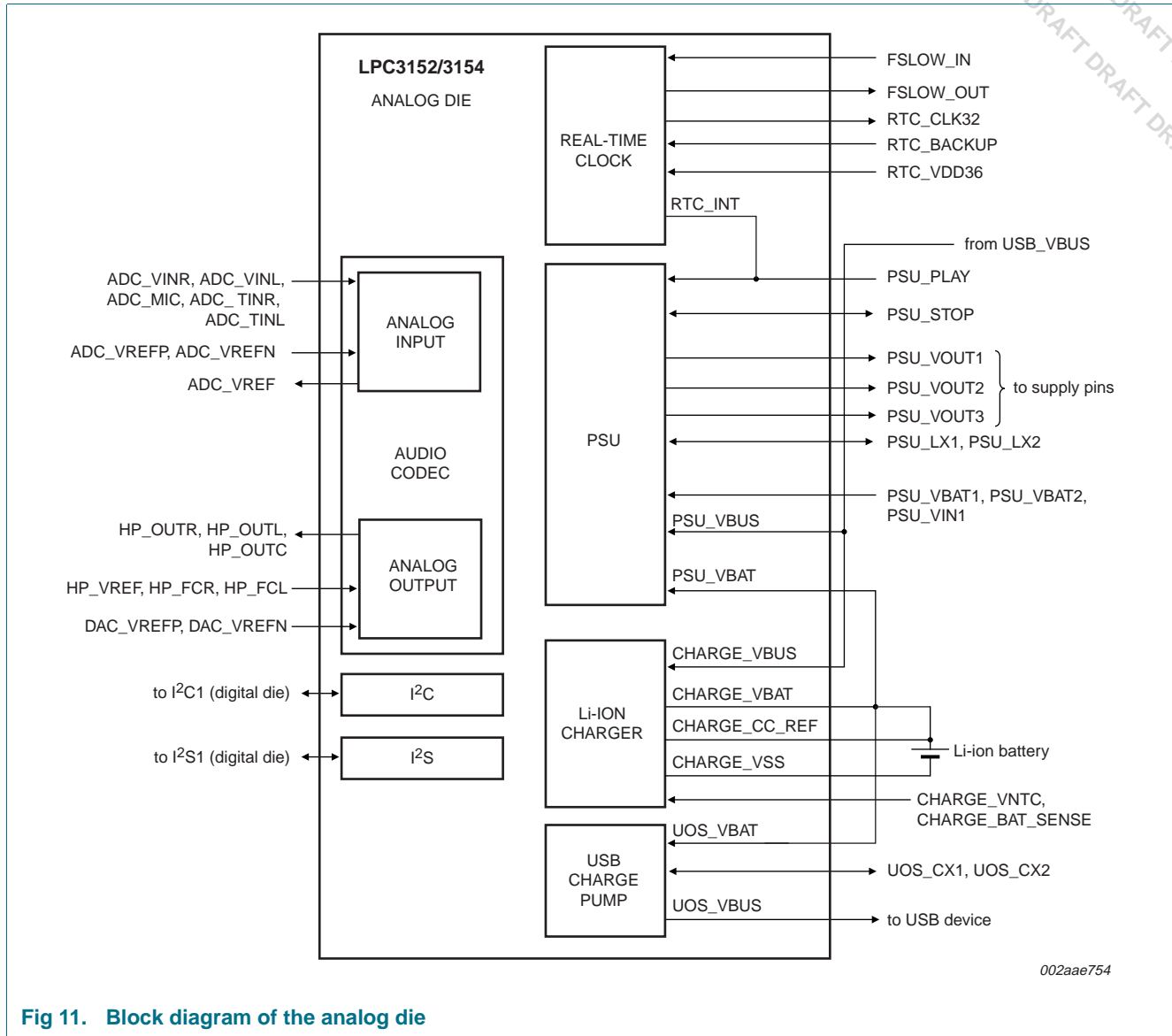


Fig 11. Block diagram of the analog die

7.2 Audio codec

7.2.1 Stereo Digital-to-Analog Converter (SDAC)

The Stereo Digital-to-Analog Converter converts a digital audio signal into an analog audio signal. The output of this module is connected to the input of the class AB headphone amplifier.

This module has the following features:

- Stereo Digital-to-Analog converter with support for 24-bit audio samples.
- Supports sample rates from 8 kHz up to 96 kHz.
- Filter implementations have a 24-bit data path with 16-bit coefficients.
- Full FIR filter implementation for all of the up-sampling filters.

- Controlled power down sequence comprising a raised cosine mute function followed by a DC ramp down to zero to avoid audible plops or clicks.
- Digital dB-linear volume control in 0.25 dB steps.
- Digital de-emphasis for 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz.
- Selection for the up-sampling filter characteristics (sharp/slow roll-off).
- Support for 2fs and 8fs input signals.
- Soft mute with a raised cosine function.

7.2.2 Class AB headphone amplifier

The class AB headphone amplifier amplifies an analog input signal to levels appropriate for a headphone output. Its input can be chosen from the Stereo Digital-to-Analog Converter (SADC) or from the analog bypass from the tuner input (through the Analog Volume Control (AVC) block). The class AB amplifier offers a solution in cases where high output levels are required or when the headphone wire is also used as an antenna for tuner reception.

This module has the following features:

- Stereo headphone amplifier.
- Three outputs: left, right, and a common signal ground output.
- Common signal ground output enables DC coupling of headphone without electrolytic capacitors.
- 16 Ω and higher output drive capability.
- Individual power down modes for each output.
- Programmable short-circuit current protection for each amplifier.
- Additional input with Analog Volume Control (AVC) directly connected to the tuner input pins.

7.2.3 Stereo Analog-to-Digital Converter (SADC) for Audio

The Stereo ADC can convert analog audio input signals into digital audio signals as shown in [Figure 12](#). The module has three input signals: stereo line-in (ADC_VINL/ADC_VINR), stereo tuner-in (ADC_TINL/ADC_TINR), and mono microphone in (ADC_MIC). These signals can be pre-processed by a Low-Noise Amplifier (LNA, microphone input only), a Programmable Gain Amplifier (PGA), and a Single-to-Differential Converter (SDC) before they arrive at the input of the actual SADC.

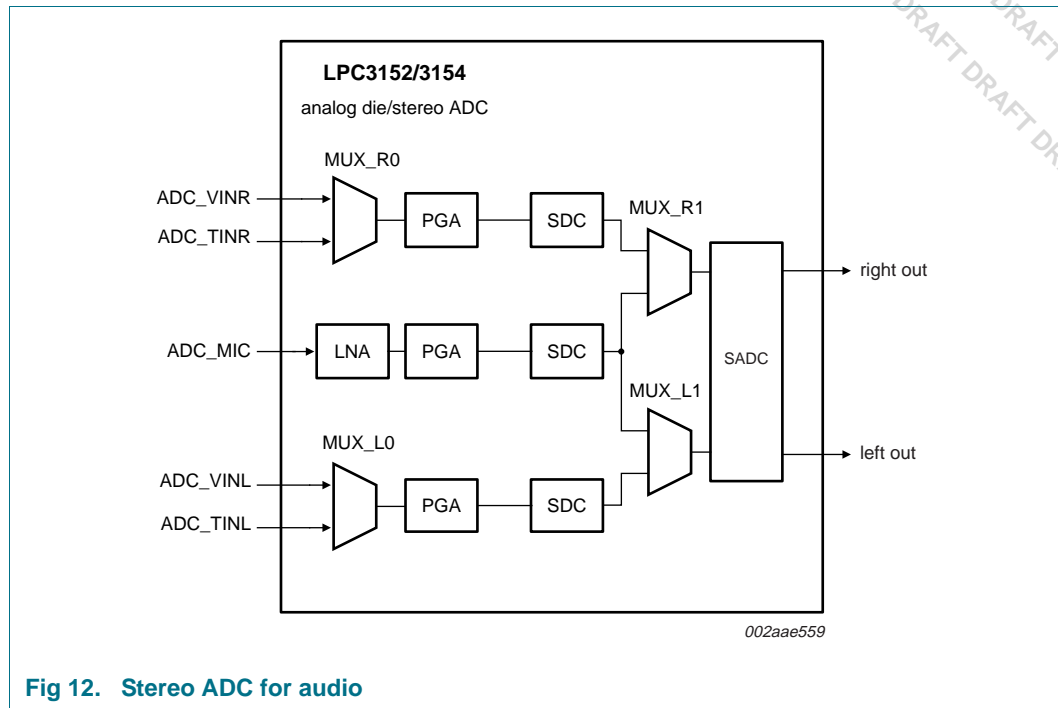


Fig 12. Stereo ADC for audio

This module has the following features:

- Three input options: line-in (stereo), tuner-in (stereo), microphone-in (mono).
- Low-Noise Amplifier (LNA) with a fixed 30 dB gain for the microphone input.
- Programmable Gain Amplifier (PGA). Gain can be set in steps of 3 dB up to 24 dB.
- Single-to-Differential Converter (SDC).
- SADC (switched cap).
- Supported audio sample frequencies are 8 kHz to 55 kHz.
- Oversampling rate 128 times the sample frequency.
- High dynamic range.
- Digital dB-linear volume control in 0.5 dB steps.
- DC blocking filter (optional).
- Soft start-up.
- Mute and overflow detection.

7.3 Li-ion charger

The built-in charger allows a Li-ion battery to be charged from the power supplied by a USB connection or by an AC adapter.

This module has the following features:

- Monitors for battery voltage, charge current, battery temperature feedback (NTC), and chip temperature (programmable temperature limits).
- Maximum charge current 250 mA.

- The nominal charge current is programmed with an external program-resistor. This allows the charge current to be adapted to the USB enumeration.
- Uses a widespread method to charge a Li-ion battery with the following stages:
 - Trickle charging with a small current for an (almost) empty battery.
 - Fast charging in Constant Current mode (CC mode) to the maximum battery voltage of $4.2\text{ V} \pm 1\%$.
 - Switch from CC mode to Constant Voltage charging (CV mode) keeping the battery voltage at 4.2 V and monitoring the current for ending the charge process.
- Short circuit resistant.
- Charger state can be observed through a register.

7.4 USB charge pump (host mode)

The USB charge pump uses the Li-ion battery to provide a low-power USB VBUS signal for the USB controller in host mode.

7.5 Power Supply Unit (PSU)

The integrated PSU allows the system to run directly from the battery voltage or the USB power supply voltage USB_VBUS. It converts the battery voltage or the USB_VBUS voltage into the supply voltages required for both the digital and analog blocks in the rest of the system.

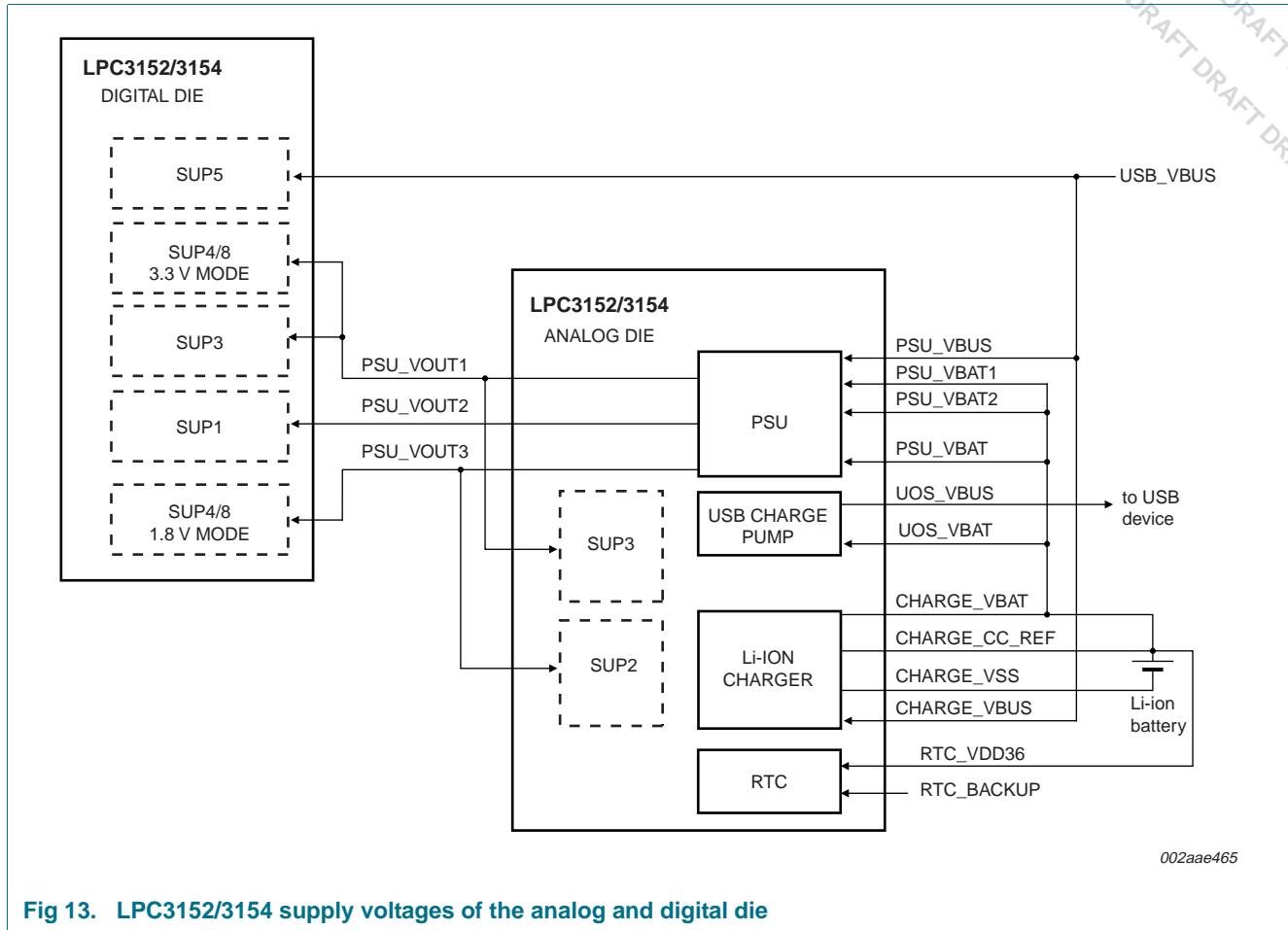


Fig 13. LPC3152/3154 supply voltages of the analog and digital die

This module has the following features:

- Takes power from the Li-Ion battery or the USB power supply.
- Outputs in Li-Ion battery mode:
 - PSU_VOUT1, 2.4 V to 3.2 V (software programmable in 8 levels), 100 mA (analog power supply and I/O).
 - PSU_VOUT2, 0.9 V to 1.4 V (software programmable in 8 levels), 100 mA (digital power supply).
 - PSU_VOUT3, 1.4 V or 1.8 V (software selectable), 50 mA (digital power supply).
 - PSU_VOUT1 and PSU_VOUT2 are generated by two inductive DC-to-DC buck converters with internal power switches.
 - PSU_VOUT3 is generated by an LDO from PSU_VOUT1.
- Outputs in USB power supply mode:
 - PSU_VOUT1, 3.3 V, 80 mA.
 - PSU_VOUT2, 1.2 V, 80 mA.
 - PSU_VOUT3, 1.4 V or 1.8 V (software selectable), 50 mA.
 - PSU_VOUT1 is generated by an LDO from the 5 V USB power supply.
 - PSU_VOUT2 and PSU_VOUT3 are generated by an LDO from PSU_VOUT1.

- Provides 'Supply_OK' detection connected to the system reset signal.

7.6 Real-Time Clock (RTC)

The Real-Time Clock module keeps track of the actual date and time, also when the system is switched off. Advanced Digital Rights Management (DRM) schemes require a secure and accurate real-time clock for managing rights such as time-limited playback rights.

This module has the following features:

- Normal power supply directly from Li-ion battery (PSU is by-passed).
- Backup power supply from (external) capacitor.
- Automatic switching between normal power supply and backup power supply.
- Signals power loss to indicate invalid real time clock readings.
- Runs on a 32 kHz oscillator.
- Ultra-low power consumption.
- The clock is implemented as a 32-bit counter at the rate of 1 Hz (derived from the 32 kHz clock).
- Alarm timer that can generate an interrupt. This interrupt is available both as an internal signal as well as a signal on an external pin.
- The external interrupt (RTC_INT) can be used to switch on the system by switching on the PSU through the PSU_PLAY pin.
- The internal interrupt signal can be used to wake-up the system from suspend mode through the event router.
- Dedicated permanent supply domain.

8. Limiting values

Table 12. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|---------------------------------|----------------------|------|-----|------|------|
| All digital I/O pins | | | | | | |
| V_i | input voltage | | -0.5 | - | +3.6 | V |
| V_o | output voltage | | -0.5 | - | +3.6 | V |
| I_o | output current | VDDE_IOC = 3.3 V | - | 4 | - | mA |
| Temperature values | | | | | | |
| T_j | junction temperature | | -40 | 25 | 125 | °C |
| T_{stg} | storage temperature | [2] | -65 | - | +150 | °C |
| T_{amb} | ambient temperature | | -40 | +25 | +85 | °C |
| Electrostatic handling | | | | | | |
| V_{ESD} | electrostatic discharge voltage | human body model [3] | -500 | - | +500 | V |
| | | machine model | -100 | - | +100 | V |
| | | charged device model | - | 500 | - | V |

[1] The following applies to the limiting values:

- a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Dependent on package type.

[3] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 k Ω series resistor.

9. Static characteristics

9.1 Digital die

Table 13: Static characteristics

$T_{amb} = -40\text{ °C to }+85\text{ °C unless otherwise specified.}$

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|-----------------------------|--|------|-----|------|------|
| Supply pins | | | | | | |
| $V_{DD(IO)}$ | input/output supply voltage | NAND flash controller pads (SUP4) and LCD interface (SUP8); 1.8 V mode | 1.65 | 1.8 | 1.95 | V |
| | | NAND flash controller pads (SUP4) and LCD interface (SUP8); 3.3 V mode | 2.5 | 3.3 | 3.6 | V |
| | | other peripherals (SUP 3) | 2.7 | 3.3 | 3.6 | V |
| $V_{DD(CORE)}$ | core supply voltage | (SUP1) | 1.1 | 1.2 | 1.3 | V |

Table 13: Static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-----------------------------------|--|-----|-----|-----|------|
| $V_{DD(OSC_PLL)}$ | oscillator and PLL supply voltage | on pin VDDA12; for 12 MHz oscillator (SUP1) | 1.0 | 1.2 | 1.3 | V |
| $V_{DD(ADC)}$ | ADC supply voltage | on pin ADC10B_VDDA33; for 10-bit ADC (SUP 3) | 2.7 | 3.3 | 3.6 | V |
| $V_{prog(pf)}$ | polyfuse programming voltage | on pin VPP; write | 3.0 | 3.3 | 3.6 | V |
| | | on pin VPP; read | 1.1 | - | 1.3 | V |
| V_{BUS} | bus supply voltage | on pin USB_VBUS (SUP5) | - | 5.0 | - | V |
| $V_{DDA(USB)(3V3)}$ | USB analog supply voltage (3.3 V) | on pin USB_VDDA33 (SUP 3) | 3.0 | 3.3 | 3.6 | V |
| | | on pin USB_VDDA33_DRV (SUP 3); driver | 2.7 | 3.3 | 3.6 | V |
| $V_{DDA(PLL)(1V2)}$ | PLL analog supply voltage (1.2 V) | on pin USB_VDDA12_PLL (SUP1) | 1.1 | 1.2 | 1.3 | V |

Input pins and I/O pins configured as input

| | | | | | | | |
|-------------|--------------------------|--|---------------------------------|-------|---------------------------------|---------------|---------------|
| V_I | input voltage | | 0 | - | VDDE_IOC | V | |
| V_{IH} | HIGH-level input voltage | SUP3; SUP4; SUP8 | $0.7VDDE_IOx$ (x = A, B, C) | - | - | V | |
| V_{IL} | LOW-level input voltage | SUP3; SUP4; SUP8 | - | - | $0.3VDDE_IOx$ (x = A, B, C) | V | |
| V_{hys} | hysteresis voltage | SUP4; SUP8; | | | | V | |
| | | 1.8 V mode | 400 | - | 600 | mV | |
| | | 3.3 V mode | 550 | - | 850 | mV | |
| | | SUP3 | $0.1VDDE_IOC$ | - | - | V | |
| I_{IL} | LOW-level input current | $V_I = 0\text{ V}$; no pull-up | - | - | <tbd> | μA | |
| I_{IH} | HIGH-level input current | $V_I = V_{DD(IO)}$; no pull-down | - | - | <tbd> | μA | |
| I_{latch} | I/O latch-up current | $-(1.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$ | [1] | - | 100 | mA | |
| I_{pu} | pull-up current | inputs with pull-up; $V_I = 0$; | | | | | |
| | | SUP4; SUP8; 1.8 V mode | [1] | <tbd> | 65 | <tbd> | μA |
| | | SUP4; SUP8; 3.3 V mode | [1] | <tbd> | 50 | <tbd> | μA |
| | | SUP3 | | <tbd> | 50 | <tbd> | μA |
| I_{pd} | pull-down current | inputs with pull-down; $V_I = V_{DD}$; | | | | | |
| | | SUP4; SUP8; 1.8 V mode | [1] | <tbd> | 75 | <tbd> | μA |

Table 13: Static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---|--|----------------------|------|---------------|---------------|
| | | SUP4; SUP8; 3.3 V mode | [1] <td> | 50 | <td> | μA |
| | | SUP3 | [1] <td> | 50 | <td> | μA |
| C_i | input capacitance | excluding bonding pad capacitance | - | - | <td> | pF |
| Output pins and I/O pins configured as output | | | | | | |
| V_O | output voltage | | <td> | - | $V_{DD(I/O)}$ | V |
| V_{OH} | HIGH-level output voltage | SUP4; SUP8; $I_{OH} = 6\text{ mA}$; 1.8 V mode | <td> | <td> | <td> | V |
| | | 3.3 V mode | $V_{DD(I/O)} - 0.26$ | <td> | <td> | V |
| | | SUP3; $I_{OH} = 6\text{ mA}$ | $V_{DD(I/O)} - 0.26$ | - | - | V |
| | | SUP3; $I_{OH} = 30\text{ mA}$ | $V_{DD(I/O)} - 0.38$ | - | - | V |
| V_{OL} | LOW-level output voltage | SUP4; SUP8 outputs; $I_{OL} = 4\text{ mA}$; 1.8 V mode | <td> | <td> | <td> | V |
| | | 3.3 V mode | [1] <td> | 0.65 | <td> | V |
| | | SUP3; $I_{OL} = 4\text{ mA}$ | - | - | <td> | V |
| I_{OH} | HIGH-level output current | $V_{DD} = VDDE_IOx$ (x = A, B, C); $V_{OH} = V_{DD} - 0.4\text{ V}$ | <td> | - | - | mA |
| | | $V_{DD} = VDDE_IOx$ (x = A, B, C); $V_{OH} = V_{DD} - 0.4\text{ V}$ | <td> | - | - | mA |
| I_{OL} | LOW-level output current | $V_{DD} = VDDE_IOx$ (x = A, B, C); $V_{OL} = 0.4\text{ V}$ | <td> | - | - | mA |
| | | $V_{DD} = VDDE_IOx$ (x = A, B, C); $V_{OL} = 0.4\text{ V}$ | <td> | - | - | mA |
| I_{OZ} | OFF-state output current | $V_O = 0\text{ V}$; $V_O = V_{DD}$; no pull-up/down | - | - | 0.064 | μA |
| I_{OHS} | HIGH-level short-circuit output current | $V_{DD} = VDDE_IOx$ (x = A, B, C); $V_{OH} = 0\text{ V}$ | - | - | <td> | mA |
| | | $V_{DD} = VDDE_IOx$ (x = A, B, C); $V_{OH} = 0\text{ V}$ | - | - | <td> | mA |
| I_{OLS} | LOW-level short-circuit output current | $V_{DD} = VDDE_IOx$ (x = A, B, C); $V_{OL} = V_{DD}$ | - | - | <td> | mA |
| | | $V_{DD} = VDDE_IOx$ (x = A, B, C); $V_{OL} = V_{DD}$ | - | - | <td> | mA |
| Z_o | output impedance | $V_{DD} = VDDE_IOx$ (x = A, B, C) | | | | |
| | | 1.8 V mode | [1] <td> | 45 | <td> | Ω |
| | | 3.3 V mode | [1] <td> | 35 | <td> | Ω |

Table 13: Static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|---------------------------------|----------------------------|--|-------------|-----|-------------|------|----|
| I²C0-bus pins | | | | | | | |
| I _{OZ} | OFF-state output current | V _O = 0 V; V _O = V _{DD} ; no pull-up/down | - | - | 7.25 | μA | |
| V _{IH} | HIGH-level input voltage | [1] | 0.7VDDE_IOC | - | - | V | |
| V _{IL} | LOW-level input voltage | [1] | - | - | 0.3VDDE_IOC | V | |
| V _{hys} | hysteresis voltage | | 0.1VDDE_IOC | - | - | V | |
| V _{OL} | LOW-level output voltage | I _{OLS} = 3 mA | - | - | 0.298 | V | |
| I _{LI} | input leakage current | VDDE voltage domain; T _{amb} = 25 °C | [1] | - | 1.7 | <td> | μA |
| | | VDD voltage domain; T _{amb} = 25 °C | [1] | - | 0.01 | <td> | μA |
| USB | | | | | | | |
| V _{i(cm)} | common-mode input voltage | high-speed mode | -50 | 200 | 500 | mV | |
| | | full-speed/low-speed mode | 800 | - | 2500 | mV | |
| | | chirp mode | -50 | - | 600 | mV | |
| V _{i(dif)} | differential input voltage | | 100 | 400 | 1100 | mV | |

[1] The parameter values specified are simulated values.

Table 14. Static characteristics of the 10 bit ADC

V_{DD(ADC)} = 2.7 V to 3.6 V; T_{amb} = -40 °C to +85 °C unless otherwise specified; ADC frequency <td>.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|-------------------------------------|------------|------|-----|----------------------|------|
| V _{IA} | analog input voltage | | 0[1] | - | V _{DD(ADC)} | V |
| C _{ia} | analog input capacitance | | - | - | <td> | pF |
| N _{res(ADC)} | ADC resolution | | 2 | - | 10 | bit |
| E _D | differential linearity error | [2][3][4] | - | - | ±1 | LSB |
| E _{L(adj)} | integral non-linearity | [2][5] | - | - | ±1 | LSB |
| E _O | offset error | [2][6] | - | - | <td> | LSB |
| E _G | gain error | [2][7] | - | - | <td> | % |
| E _T | absolute error | [2][8] | - | - | <td> | LSB |
| V _{err(O)} | offset error voltage | | -20 | - | +20 | mV |
| V _{err(FS)} | full-scale error voltage | | <td> | - | <td> | mV |
| R _{vsi} | voltage source interface resistance | | - | - | <td> | kΩ |

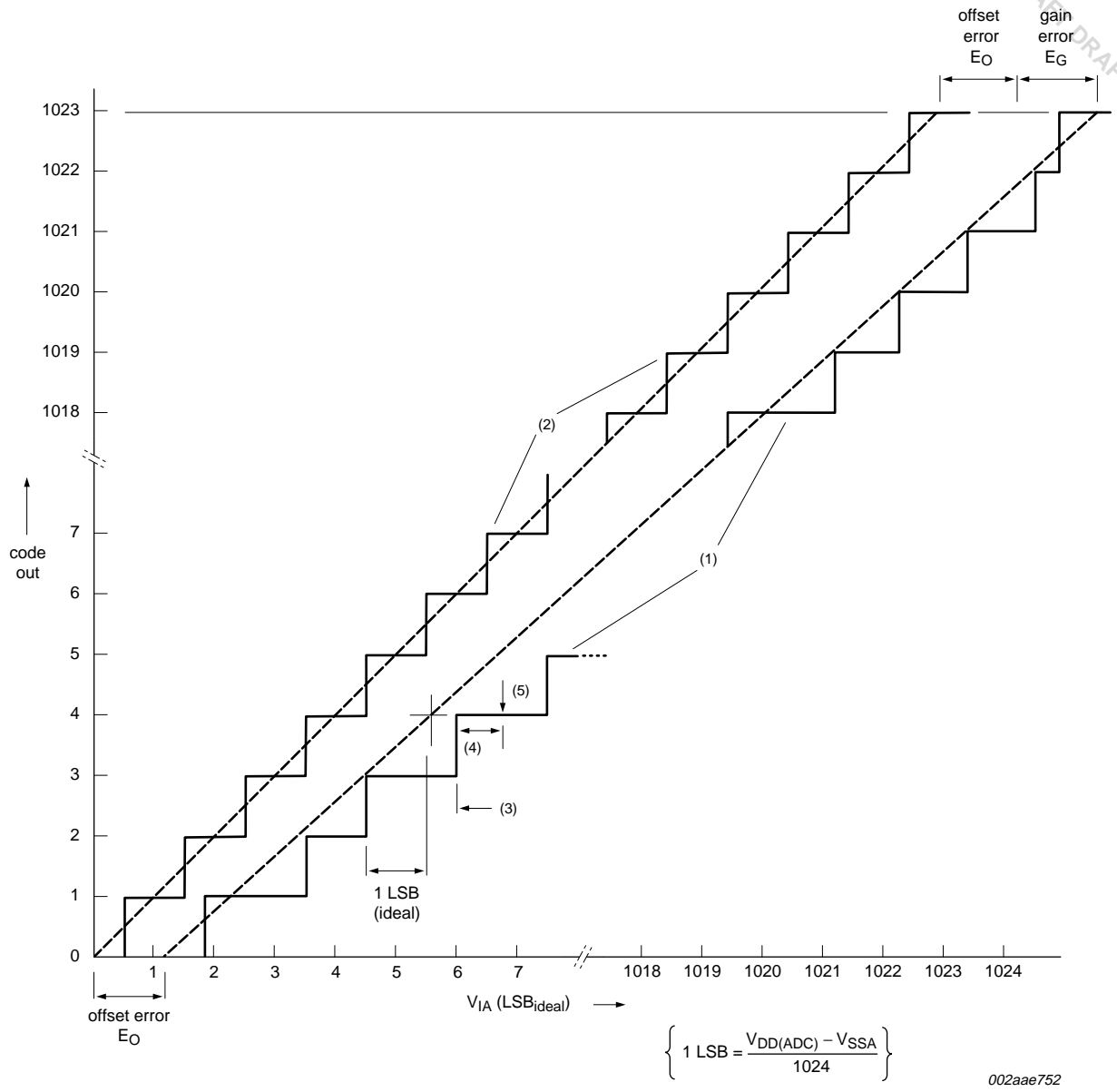
[1] On pin ADC10B_GNDA.

[2] Conditions: V_{SSA} = 0 V on pin ADC10B_GNDA, V_{DD(ADC)} = 3.3 V.

[3] The ADC is monotonic, there are no missing codes.

[4] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See [Figure 14](#).

- [5] The integral non-linearity ($E_{L(\text{adj})}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See [Figure 14](#).
- [6] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See [Figure 14](#).
- [7] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See [Figure 14](#).
- [8] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See [Figure 14](#).
- [9] See [Figure 15](#).



- (1) Example of an actual transfer curve.
- (2) The ideal transfer curve.
- (3) Differential linearity error (E_D).
- (4) Integral non-linearity ($E_{L(adj)}$).
- (5) Center of a step of the actual transfer curve.

Fig 14. ADC characteristics

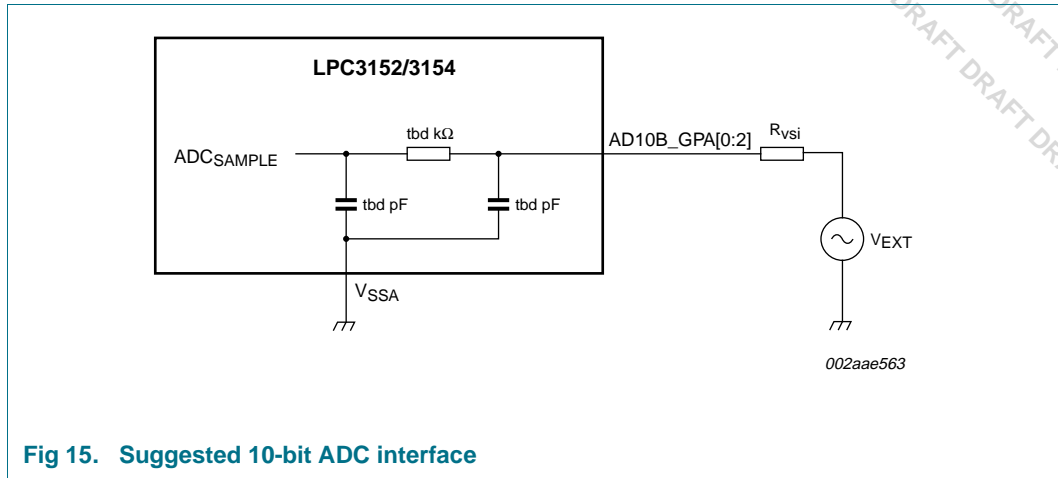


Fig 15. Suggested 10-bit ADC interface

9.2 Analog die

Table 15. Static characteristics of the analog die supply pins

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|-----------------------------|---|-----|-----|------|------|
| $V_{DD(I/O)}$ | input/output supply voltage | peripheral supply of the analog die; SUP3 | 2.7 | 3.3 | 3.6 | V |
| $V_{DD(CORE)}$ | core supply voltage | core supply of the analog die; SUP2 | 1.3 | 1.4 | 1.95 | V |

9.2.1 PSU

Table 16: Static characteristics of the PSU

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------|--------------------------|--|------|-----|------|------|
| $V_i(V_{BUS})$ | V_{BUS} input voltage | on pin PSU_VBUS | 4.0 | 5 | 5.5 | V |
| V_{BAT} | battery supply voltage | on pin PSU_VBAT | 2.7 | 3.7 | 4.2 | V |
| output PSU_VOUT1 | | | | | | |
| V_o | output voltage | generated from PSU_VBAT (programmable in 8 levels) | 2.4 | 2.8 | 3.2 | V |
| | | generated from PSU_VBUS | 3.1 | 3.3 | 3.5 | V |
| ΔV_o | output voltage deviation | output voltage generated from PSU_VBAT [1] | -100 | - | +100 | mV |
| I_o | output current | on pin PSU_VOUT1 | - | - | 80 | mA |
| $I_{L(LDO)(max)}$ | maximum LDO load current | on LDO1 | 200 | 250 | - | mA |

Table 16: Static characteristics of the PSU ...continued $T_{amb} = -40\text{ °C to }+85\text{ °C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|-------------------------------|---|------|------|------|------|
| output PSU_VOUT2 | | | | | | |
| V_O | output voltage | generated from PSU_VBAT (programmable in 8 levels) | 0.9 | 1.04 | 1.4 | V |
| | | generated from PSU_VBUS (LDO1 on) | 1.15 | 1.2 | 1.25 | V |
| ΔV_O | output voltage deviation | output voltage generated from PSU_VBAT ^[1] | -50 | - | +50 | mV |
| I_O | output current | on pin PSU_VOUT2 | - | - | 80 | mA |
| $I_{L(LDO)(max)}$ | maximum LDO load current | on LDO2 | 80 | 100 | - | mA |
| output PSU_VOUT3 | | | | | | |
| V_O | output voltage | generated from either PSU_VBAT or PSU_VBUS (programmable in 2 levels) | - | 1.4 | 1.8 | V |
| | | on LDO3 of $V_O = 1.4\text{ V}$ (default) | 1.35 | 1.4 | 1.45 | V |
| | | on LDO3 of $V_O = 1.8\text{ V}$ (default) | 1.75 | 1.8 | 1.85 | V |
| I_O | output current | on pin PSU_VOUT3 | - | - | 50 | mA |
| $I_{L(LDO)(max)}$ | maximum LDO load current | on LDO3 | - | 50 | - | mA |
| DC-to-DC converter | | | | | | |
| $\eta_{(DCDC)}$ | DC-to-DC converter efficiency | | - | 85 | - | % |
| f_{clk} | clock frequency | | - | 12 | - | MHz |
| f_{osc} | oscillator frequency | | 8 | 10 | 12 | MHz |
| f_{sw} | switching frequency | | - | 1 | - | MHz |

[1] Deviation of output voltage on pin PSU_VOUTn from its nominal, programmed value.

Table 17: Static characteristics of the analog input

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-----------------------------------|---|-----|-------------------|-----|------------------|
| $I_{DDA(ADC)(3V3)}$ | ADC analog supply current (3.3 V) | per mono ADC; normal operation | - | 2.2 | - | mA |
| $I_{DDA(ADC)(1V8)}$ | ADC analog supply current (1.8 V) | per mono ADC; normal operation | - | - | 20 | μA |
| $I_{ref(neg)}$ | negative reference current | per mono ADC; normal operation | - | 20 | - | μA |
| $I_{ref(pos)}$ | positive reference current | per mono ADC; normal operation | - | 20 | - | μA |
| $I_{DDA(SDC)}$ | SDC analog supply current | | - | 0.4 | - | mA |
| $I_{DDA(PGA)}$ | PGA analog supply current | | - | 430 | - | μA |
| G_{PGA} | PGA gain | | - | -1.94 | - | dB |
| $I_{DDA(bias)}$ | bias analog supply current | N = 13 for all modules on; normal operation | - | $190+N \times 10$ | - | μA |
| $I_{DDA(LNA)}$ | LNA analog supply current | | - | 0.85 | 1.2 | mA |
| G_{LNA} | LNA gain | In a bandwidth between 300 Hz and 5 kHz. | 28 | 30 | 32 | dB |
| R_{ref} | reference resistance | headphone and DAC | - | 11.25 | | $\text{k}\Omega$ |
| R_{com} | common resistance | headphone | - | 11.25 | | $\text{k}\Omega$ |
| G | gain | step size 3 dB | 0 | - | 24 | dB |

9.2.1.1 PSU_VOUT1 efficiency

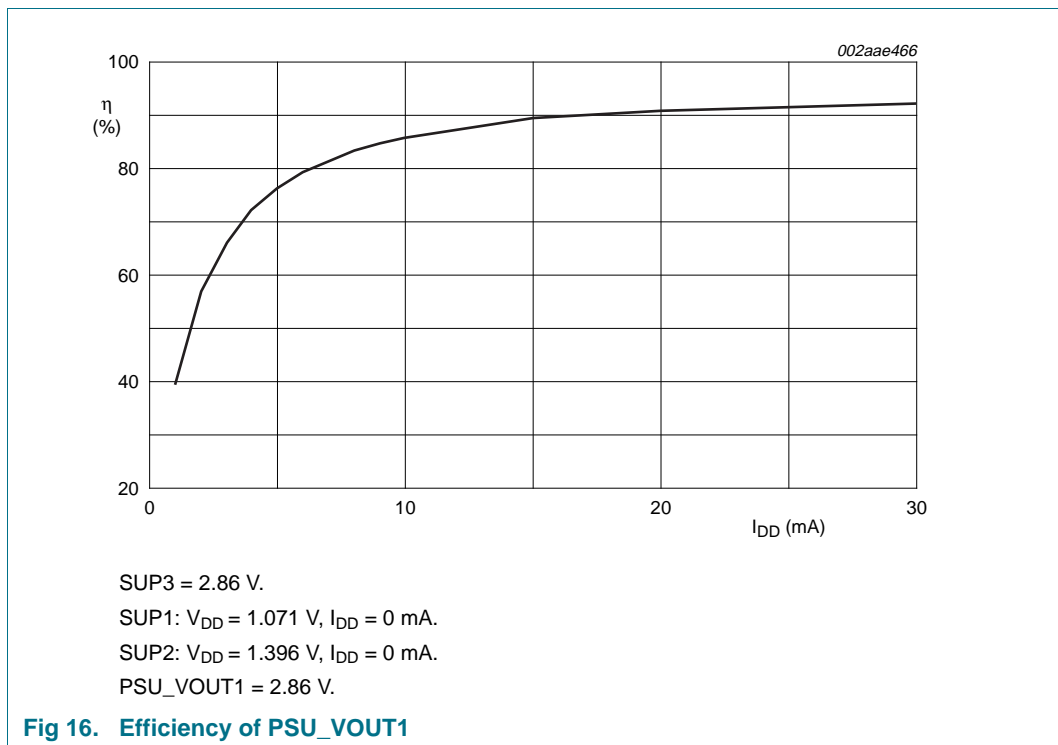


Table 18. Efficiency of output on PSU_VOUT1 (PSU_VOUT1 programmed to 2.86 V)

| I_{BAT} / mA on pin PSU_VBAT | V_{BAT} / V | I_{DD} / mA (SUP3) | V_{DD} / V (SUP4) | Efficiency / % |
|-----------------------------------|---------------|-------------------------|------------------------|----------------|
| 2 | 3.602 | 1 | 2.8676 | 39.80566352 |
| 2.8 | 3.6016 | 2 | 2.864 | 56.80015231 |
| 3.598 | - | 3 | 2.8605 | 66.22816876 |
| 4.396 | 3.601 | 4 | 2.8569 | 72.18953182 |
| 5.195 | 3.6006 | 5 | 2.8533 | 76.27057345 |
| 5.994 | 3.6003 | 6 | 2.8498 | 79.23374865 |
| 6.793 | 3.5999 | 7 | 2.8462 | 81.47256753 |
| 7.59 | 3.5995 | 8 | 2.8426 | 83.23802841 |
| 8.388 | 3.5992 | 9 | 2.83991 | 84.63671469 |
| 9.231 | 3.5988 | 10 | 2.8542 | 85.9167695 |
| 13.32 | 3.597 | 15 | 2.8549 | 89.37941277 |
| 17.368 | 3.595 | 20 | 2.837 | 90.87420537 |
| 25.59 | 3.591 | 30 | 2.8198 | 92.056375145 |

9.2.1.2 PSU_VOUT2 efficiency

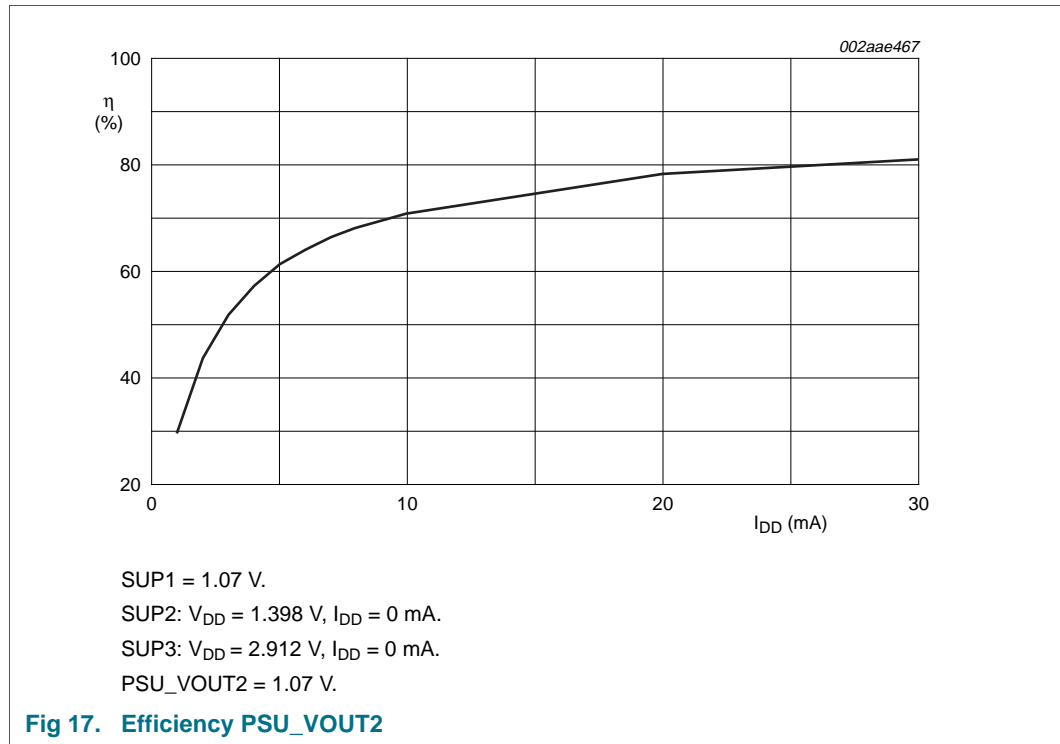


Table 19. Efficiency of output on PSU_VOUT2 (PSU_VOUT2 programmed to 1.07 V)

| I_{BAT} / mA on pin PSU_VBAT | V_{BAT} / V | I_{DD} / mA for supply domain SUP1 | V_{DD} / V | Efficiency / % |
|---|----------------------------|---|---------------------------|-----------------------|
| 1.002 | 3.602 | 1 | 1.072 | 29.70184007 |
| 1.357 | 3.6022 | 2 | 1.069 | 43.7381119 |
| 1.71 | 3.6021 | 3 | 1.068 | 52.0164407 |
| 2.063 | 3.6019 | 4 | 1.067 | 57.43723586 |
| 2.415 | 3.6018 | 5 | 1.0664 | 61.29900313 |
| 2.77 | 3.6016 | 6 | 1.0655 | 64.08102616 |
| 3.122 | 3.6015 | 7 | 1.0647 | 66.28404084 |
| 3.472 | 3.6013 | 8 | 1.0638 | 68.06297931 |
| 3.822 | 3.6011 | 9 | 1.0628 | 69.49734136 |
| 4.172 | 3.601 | 10 | 1.0619 | 70.68319948 |
| 5.7 | 3.6003 | 15 | 1.0218 | 74.68675856 |
| 7.292 | 3.5997 | 20 | 1.0258 | 78.15913105 |
| 10.466 | 3.5983 | 30 | 1.0151 | 80.86339729 |

9.2.2 Li-ion charger

Table 20: Static characteristics of the Li-ion charger

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|--|-------|------|-------|------|
| V_{bat} | battery voltage | cs_bits at 0000 | - | - | 4.25 | V |
| I_{load} | load current | due to charger when 5 V is disconnected ^[1] | - | 3 | - | mA |
| constant-current charge (fast charge) mode | | | | | | |
| I_{bat} | battery current | $R_{ext} = 1.00 \text{ k}\Omega$ | 95 | 100 | 105 | mA |
| | | $R_{ext} = 400 \Omega$ | 237.5 | 250 | 262.5 | mA |
| trickle charge mode | | | | | | |
| $V_{th(trch)bat}$ | battery trickle charge threshold voltage | battery voltage rising | - | 2.8 | - | V |
| | | battery voltage falling | - | 2.7 | - | V |
| constant-voltage charge mode | | | | | | |
| $V_{th(cvch)bat}$ | battery constant-voltage charge threshold voltage | After compensation using cs_bits | 4.158 | 4.2 | 4.242 | V |
| recharge mode | | | | | | |
| $V_{th(rech)bat}$ | battery recharge threshold voltage | | - | 4.05 | - | V |

[1] Reversed current spec: For $V_{bat} = 3.2 \text{ V}$ (no USB and $100 \text{ k}\Omega$ to ground).

10. Dynamic characteristics

10.1 Digital die

10.1.1 LCD controller

10.1.1.1 Intel 8080 mode

Table 21. Dynamic characteristics: LCD controller in Intel 8080 mode

$C_L = 25\text{ pF}$, $T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, unless otherwise specified; $V_{DD(I/O)} = 1.8\text{ V}$ and 3.3 V (SUP8) .

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|------------------------------|------------|-------|---------------------------|-----|------|
| $t_{su(A)}$ | address set-up time | | - | $1 \times \text{LCDCLK}$ | - | ns |
| $t_{h(A)}$ | address hold time | | - | $2 \times \text{LCDCLK}$ | - | ns |
| $t_{cy(a)}$ | access cycle time | [1] | - | $5 \times \text{LCDCLK}$ | - | ns |
| $t_{w(en)W}$ | write enable pulse width | [1] | - | $2 \times \text{LCDCLK}$ | - | ns |
| $t_{w(en)R}$ | read enable pulse width | [1] | - | $2 \times \text{LCDCLK}$ | - | ns |
| t_r | rise time | | 2 | - | 5 | ns |
| t_f | fall time | | 2 | - | 5 | ns |
| $t_{su(D)}$ | data input set-up time | | <tbd> | - | - | ns |
| $t_{h(D)}$ | data input hold time | | <tbd> | - | - | ns |
| $t_{d(QV)}$ | data output valid delay time | | - | $-1 \times \text{LCDCLK}$ | - | ns |
| $t_{dis(Q)}$ | data output disable time | | - | $2 \times \text{LCDCLK}$ | - | ns |

[1] Timing is determined by the LCD Interface Control Register fields: $\text{INVERT_CS} = 1$; $\text{MI} = 0$; $\text{PS} = 0$; $\text{INVERT_E_RD} = 0$. See the *LPC315x user manual*.

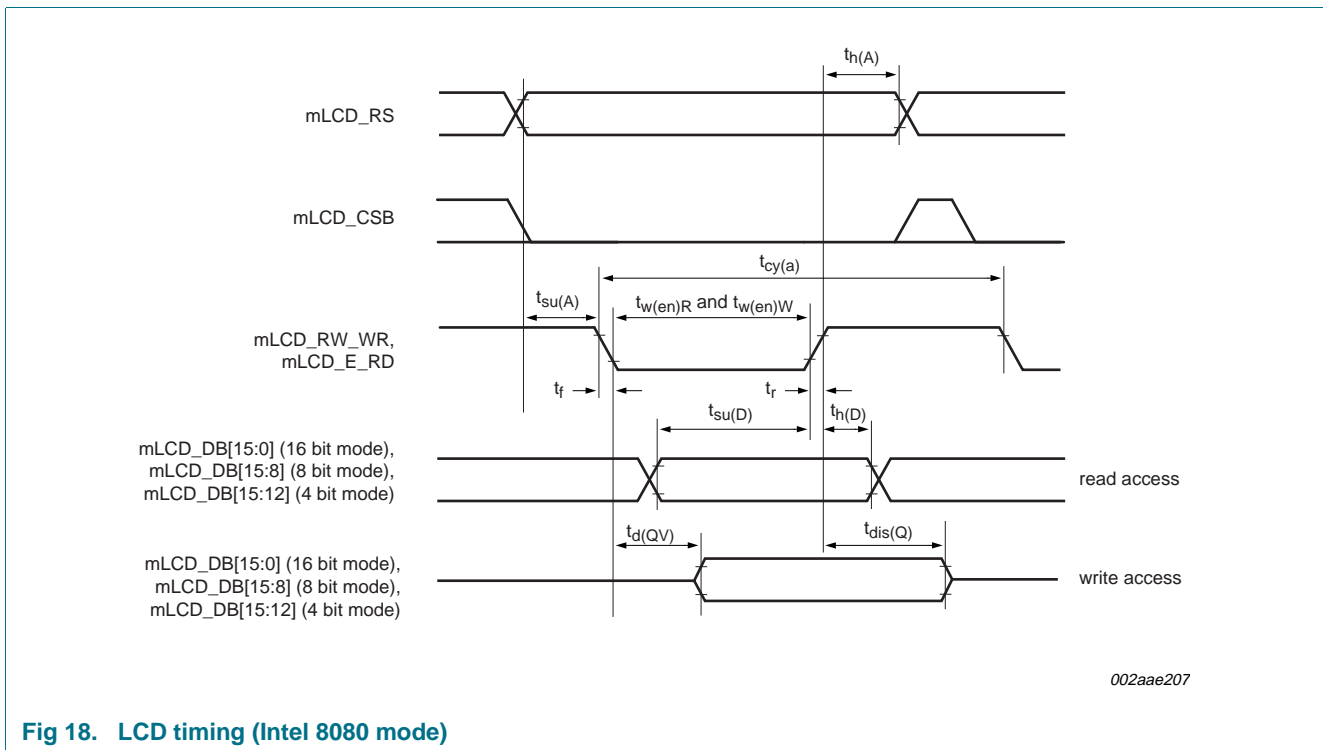


Fig 18. LCD timing (Intel 8080 mode)

10.1.1.2 Motorola 6800 mode

Table 22. Dynamic characteristics: LCD controller in Motorola 6800 mode

$C_L = 25\text{ pF}$, $T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, unless otherwise specified; $V_{DD(I/O)} = 1.8\text{ V}$ and 3.3 V (SUP8) .

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|------------------------------|-------------|------|---------------------------|-----|------|
| $t_{su(A)}$ | address set-up time | | - | $1 \times \text{LCDCLK}$ | - | ns |
| $t_{h(A)}$ | address hold time | | - | $2 \times \text{LCDCLK}$ | - | ns |
| $t_{cy(a)}$ | access cycle time | [1] | - | $5 \times \text{LCDCLK}$ | - | ns |
| t_r | rise time | | 2 | - | 5 | ns |
| t_f | fall time | | 2 | - | 5 | ns |
| $t_{su(D)}$ | data input set-up time | | <td> | - | - | ns |
| $t_{h(D)}$ | data input hold time | | <td> | - | - | ns |
| $t_{d(QV)}$ | data output valid delay time | | - | $-1 \times \text{LCDCLK}$ | - | ns |
| $t_{dis(Q)}$ | data output disable time | | - | $2 \times \text{LCDCLK}$ | - | ns |
| $t_{w(en)}$ | enable pulse width | read cycle | - | $2 \times \text{LCDCLK}$ | - | ns |
| | | write cycle | - | $2 \times \text{LCDCLK}$ | - | ns |

[1] Timing is derived from the LCD Interface Control Register fields: INVERT_CS = 1; MI = 1; PS = 0; INVERT_E_RD = 0. See the *LPC315x user manual*.

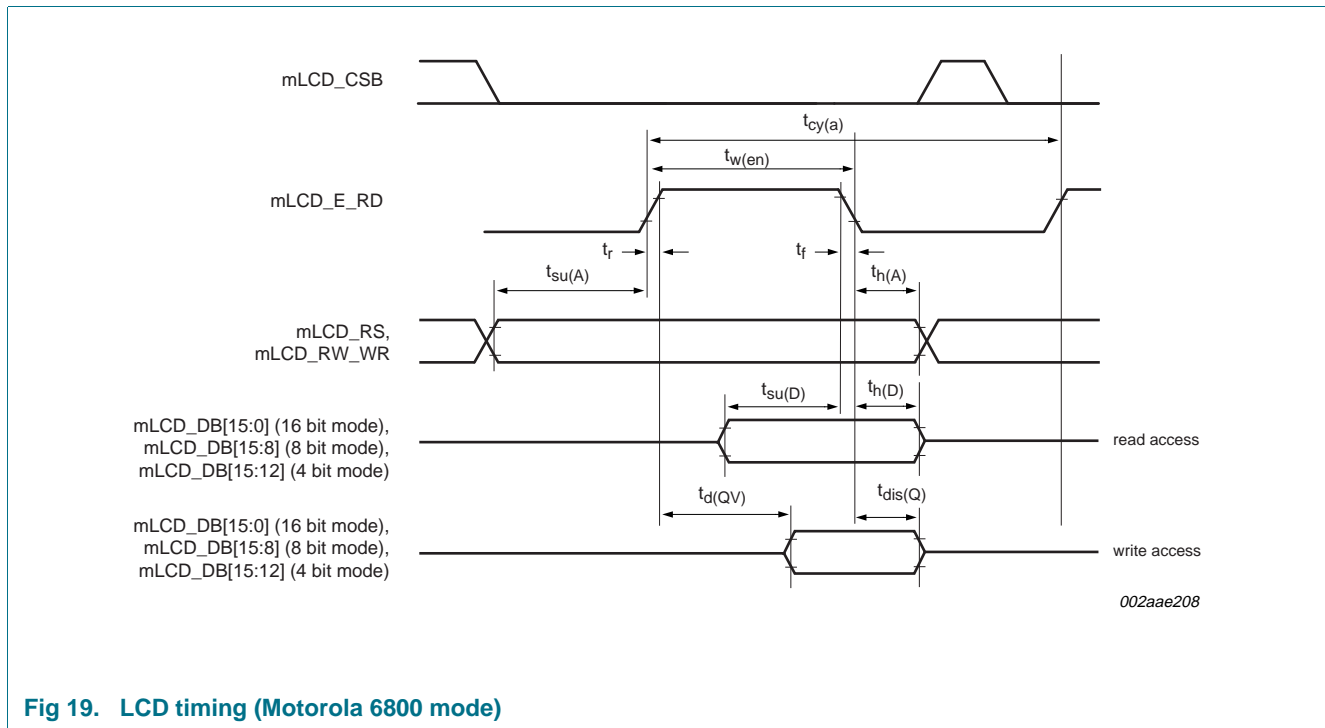


Fig 19. LCD timing (Motorola 6800 mode)

10.1.1.3 Serial mode

Table 23. Dynamic characteristics: LCD controller serial mode

$C_L = 25\text{ pF}$, $T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, unless otherwise specified; $V_{DD(I/O)} = 1.8\text{ V}$ and 3.3 V (SUP8) .

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|------------------------------|------------|-------|---------------------------|-----|------|
| $T_{cy(\text{clk})}$ | clock cycle time | | [1] | $5 \times \text{LCDCLK}$ | - | ns |
| $t_{w(\text{clk})H}$ | HIGH clock pulse width | | [1] | $3 \times \text{LCDCLK}$ | - | ns |
| $t_{w(\text{clk})L}$ | LOW clock pulse width | | [1] | $2 \times \text{LCDCLK}$ | - | ns |
| t_r | rise time | | 2 | - | 5 | ns |
| t_f | fall time | | 2 | - | 5 | ns |
| $t_{su(A)}$ | address set-up time | | - | $3 \times \text{LCDCLK}$ | - | ns |
| $t_{h(A)}$ | address hold time | | - | $2 \times \text{LCDCLK}$ | - | ns |
| $t_{su(D)}$ | data input set-up time | | <tdb> | - | - | ns |
| $t_{h(D)}$ | data input hold time | | <tdb> | - | - | ns |
| $t_{su(S)}$ | chip select set-up time | | - | $3 \times \text{LCDCLK}$ | - | ns |
| $t_{h(S)}$ | chip select hold time | | - | $1 \times \text{LCDCLK}$ | - | ns |
| $t_{d(QV)}$ | data output valid delay time | | - | $-1 \times \text{LCDCLK}$ | - | ns |

[1] Timing is determined by the LCD Interface Control Register fields: PS = 1; SERIAL_CLK_SHIFT = 3; SERIAL_READ_POS = 3. See the *LPC315x user manual*.

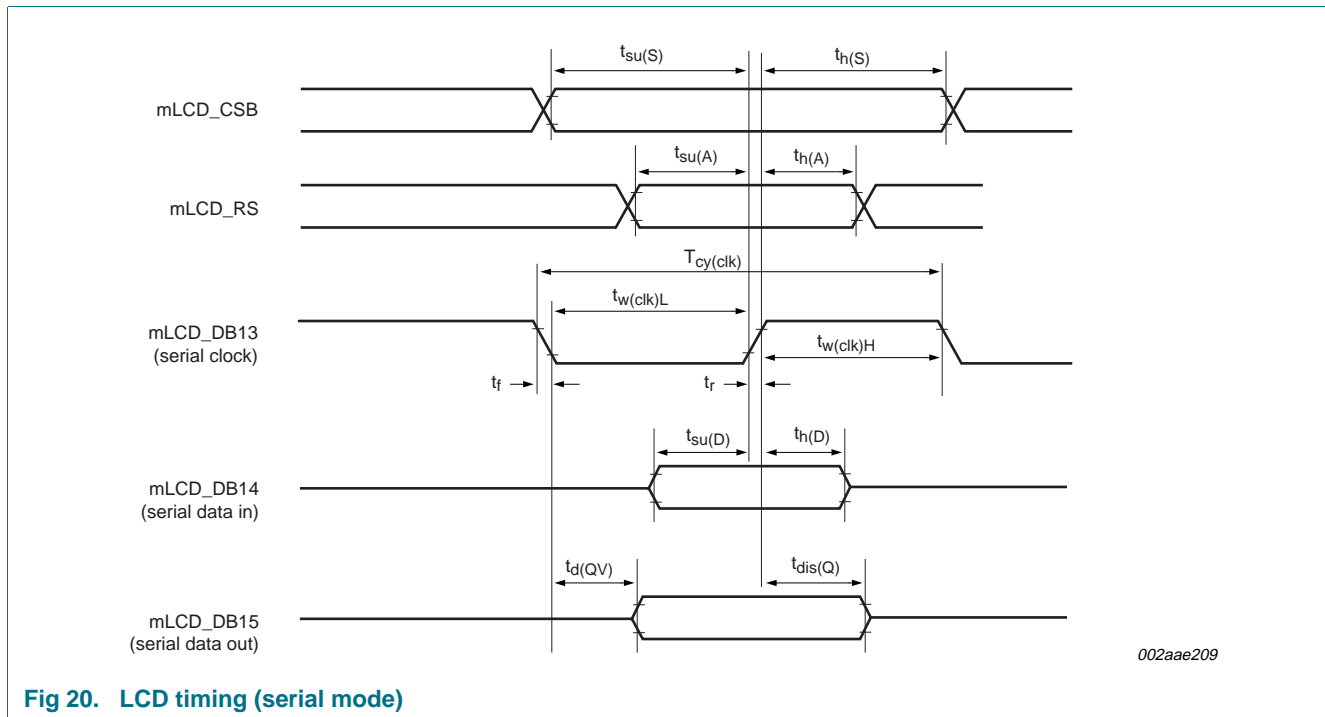


Fig 20. LCD timing (serial mode)

10.1.2 SRAM controller

Table 24. Dynamic characteristics: static external memory interface

$C_L = 25\text{ pF}$, $T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, unless otherwise specified; $V_{DD(I/O)} = 1.8\text{ V}$ and 3.3 V (SUP8).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|------------|-----------|-------------------------------|-----|------|
| Common to read and write cycles | | | | | | |
| t_{CSLAV} | \overline{CS} LOW to address valid time | | -1.8 | 0 | 4 | ns |
| Read cycle parameters | | | | | | |
| t_{OELAV} | \overline{OE} LOW to address valid time | | [1] | 0 – WAITOEN × HCLK | - | ns |
| t_{BLSLAV} | \overline{BLS} LOW to address valid time | | [1] | 0 – WAITOEN × HCLK | - | ns |
| t_{CSLOEL} | \overline{CS} LOW to \overline{OE} LOW time | | - | 0 + WAITOEN × HCLK | - | ns |
| $t_{CSLBLSL}$ | \overline{CS} LOW to \overline{BLS} LOW time | | [1] | 0 + WAITOEN × HCLK | - | ns |
| t_{OELOEH} | \overline{OE} LOW to \overline{OE} HIGH time | | [1][2][3] | (WAITRD – WAITOEN + 1) × HCLK | - | ns |
| $t_{BLSLBLSH}$ | \overline{BLS} LOW to \overline{BLS} HIGH time | | [1][2][3] | (WAITRD – WAITOEN + 1) × HCLK | - | ns |
| $t_{su(D)}$ | data input set-up time | | 9 | - | - | ns |
| $t_{h(D)}$ | data input hold time | | - | 0 | - | ns |
| t_{CSHOEH} | \overline{CS} HIGH to \overline{OE} HIGH time | | 3 | 0 | - | ns |
| $t_{CSHBLSH}$ | \overline{CS} HIGH to \overline{BLS} HIGH time | | - | 0 | - | ns |
| t_{OEHANV} | \overline{OE} HIGH to address invalid time | | 10 | - | - | ns |
| $t_{BLSHANV}$ | \overline{BLS} HIGH to address invalid time | | - | 1 × HCLK | - | ns |
| Write cycle parameters | | | | | | |
| t_{CSLDV} | \overline{CS} LOW to data valid time | | - | - | 9 | ns |
| t_{CSLWEL} | \overline{CS} LOW to \overline{WE} LOW time | | [4] | (WAITWEN + 1) × HCLK | - | ns |
| $t_{CSLBLSL}$ | \overline{CS} LOW to \overline{BLS} LOW time | | [4] | WAITWEN × HCLK | - | ns |
| t_{WELDV} | \overline{WE} LOW to data valid time | | [4] | 0 – (WAITWEN + 1) × HCLK | - | ns |
| t_{WELWEH} | \overline{WE} LOW to \overline{WE} HIGH time | | [4][5][6] | (WAITWR – WAITWEN + 1) × HCLK | - | ns |
| $t_{BLSLBLSH}$ | \overline{BLS} LOW to \overline{BLS} HIGH time | | [4][5] | (WAITWR – WAITWEN + 3) × HCLK | - | ns |
| t_{WEHANV} | \overline{WE} HIGH to address invalid time | | - | 1 × HCLK | - | ns |
| t_{WEHDNV} | \overline{WE} HIGH to data invalid time | | - | 1 × HCLK | - | ns |
| $t_{BLSHANV}$ | \overline{BLS} HIGH to address invalid time | | - | 1 × HCLK | - | ns |
| $t_{BLSHDNV}$ | \overline{BLS} HIGH to data invalid time | | - | 1 × HCLK | - | ns |

- [1] Refer to the *LPC315x user manual* for the programming of WAITOEN and HCLK.
- [2] Refer to the *LPC315x user manual* for the programming of WAITRD and HCLK.
- [3] (WAITRD – WAITOEN + 1) = 3 min at 60 MHz.
- [4] Refer to the *LPC315x user manual* for the programming of WAITWEN and HCLK.
- [5] Refer to the *LPC315x user manual* for the programming of WAITWR and HCLK.
- [6] (WAITWR – WAITWEN + 1) = 3 min at 60 MHz.

Table 25. Dynamic characteristics of SDR SDRAM memory interface ...continued

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.^{[1][2][3]}

| Symbol | Parameter | Conditions | Min | Typical | Max | Unit |
|-------------|---------------------------------|--|-----------|---------|--------------|------|
| $t_{h(o)}$ | output hold time | on pin EBI_CKE | [5] 0.13 | - | 3.6 | ns |
| | | on pins EBI_NRAS_BLOUT, EBI_NCAS_BLOUT, EBI_NWE, EBI_NDYCS | -0.1 | - | 3.6 | ns |
| | | on pins EBI_DQM_1, EBI_DQM_0_NOE | 1.7 | - | 5 | ns |
| $t_{d(AV)}$ | address valid delay time | | [5] - | - | 5 | ns |
| $t_{h(A)}$ | address hold time | | [5] -0.1 | - | 5 | ns |
| $t_{d(QV)}$ | data output valid delay time | | [5] - | - | 9 | ns |
| $t_{h(Q)}$ | data output hold time | | [5] 4 | - | 10 | ns |
| $t_{su(D)}$ | data input set-up time | | [6] <tbd> | - | - | ns |
| $t_{h(D)}$ | data input hold time | | [6] <tbd> | - | - | ns |
| t_{QZ} | data output high-impedance time | | - | - | < T_{CLCL} | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] All values valid for pads set to high slew rate. $VDDE_{IOA} = VDDE_{IOB} = 1.8 \pm 0.15\text{ V}$. $VDDI = 1.2 \pm 0.1\text{ V}$.

[3] Refer to the LPC3152/3154 user manual for the programming of MPMCDynamicReadConfig and SYSCREG_MPMP_DELAYMODES registers.

[4] $f_{oper} = 1 / T_{CLCL}$

[5] $t_{d(o)}$, $t_{h(o)}$, $t_{d(AV)}$, $t_{h(A)}$, $t_{d(QV)}$, $t_{h(Q)}$ times are dependent on MPMCDynamicReadConfig register value and SYSCREG_MPMP_DELAYMODES register bits 11:6.

[6] $t_{su(D)}$, $t_{h(D)}$ times are dependent on SYSCREG_MPMP_DELAYMODES register bits 5:0.

10.2 NAND flash memory controller

Table 26. Dynamic characteristics of the NAND Flash memory controller

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

| Symbol | Parameter | Typical | Unit |
|-----------|--------------------------------|---------------------------------------|------|
| t_{REH} | \overline{RE} HIGH hold time | [1][2][3] $T_{HCLK} \times (T_{REH})$ | ns |
| t_{RP} | \overline{RE} pulse width | [1][2][3] $T_{HCLK} \times (T_{RP})$ | ns |
| t_{WH} | \overline{WE} HIGH hold time | [1][2][3] $T_{HCLK} \times (T_{WH})$ | ns |
| t_{WP} | \overline{WE} pulse width | [1][2][3] $T_{HCLK} \times (T_{WP})$ | ns |
| t_{CLS} | CLE set-up time | [1][2][3] $T_{HCLK} \times (T_{CLS})$ | ns |
| t_{CLH} | CLE hold time | [1][2][3] $T_{HCLK} \times (T_{CLH})$ | ns |
| t_{ALS} | ALE set-up time | [1][2][3] $T_{HCLK} \times (T_{ALS})$ | ns |
| t_{ALH} | ALE hold time | [1][2][3] $T_{HCLK} \times (T_{ALH})$ | ns |
| t_{CS} | \overline{CE} set-up time | [1][2][3] $T_{HCLK} \times (T_{CS})$ | ns |
| t_{CH} | \overline{CE} hold time | [1][2][3] $T_{HCLK} \times (T_{CH})$ | ns |

[1] $T_{HCLK} = 1 / \text{NANDFLASH_NAND_CLK}$, see *LPC315x user manual*.

[2] See registers NandTiming1 and NandTiming2 in the *LPC315x user manual*.

[3] Each timing parameter can be set from 7 nand_clk clock cycles to 1 nand_clk clock cycle. (A programmed zero value is treated as a one).

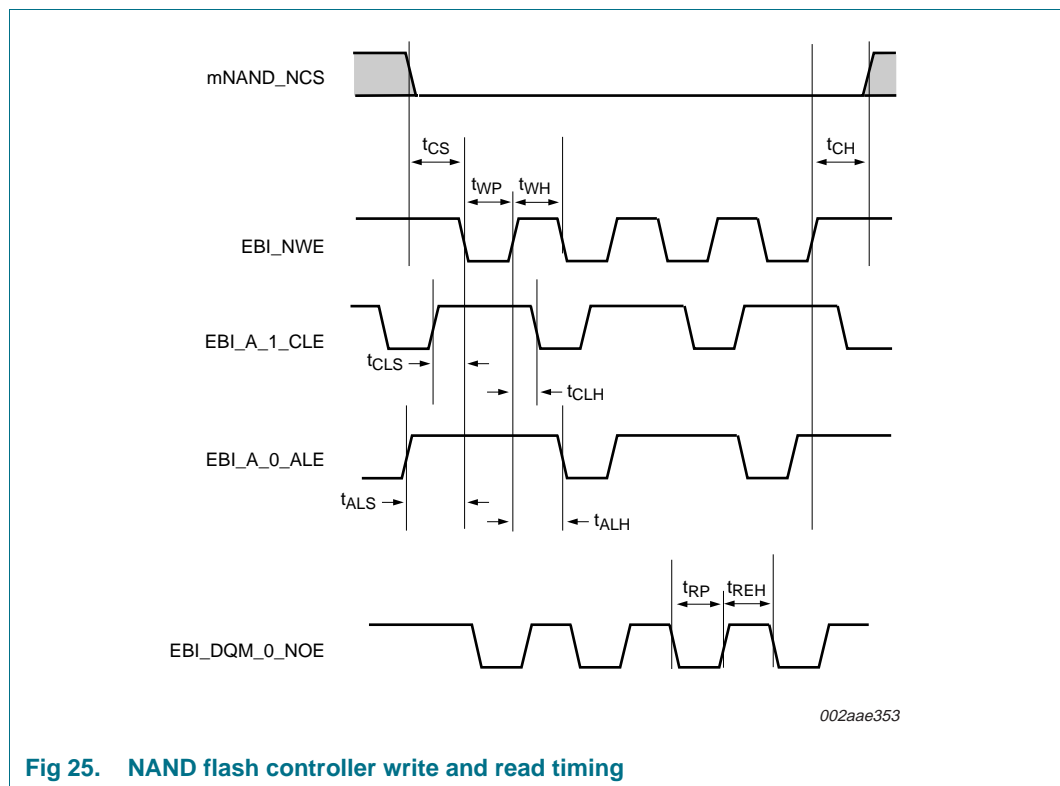


Fig 25. NAND flash controller write and read timing

10.2.1 Crystal oscillator

Table 27: Dynamic characteristics: crystal oscillator

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|----------------------|--------------------------|-----|-----|------|---------|
| f_{osc} | oscillator frequency | | 10 | 12 | 25 | MHz |
| δ_{clk} | clock duty cycle | | 45 | 50 | 55 | % |
| C_{xtal} | crystal capacitance | input; on pin FFAST_IN | - | - | 2 | pF |
| | | output; on pin FFAST_OUT | - | - | 0.74 | pF |
| $t_{startup}$ | start-up time | | - | 500 | - | μ s |
| P_{drive} | drive power | | 100 | - | 500 | μ W |

10.2.2 SPI

Table 28. Dynamic characteristics of SPI pins

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial applications

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------|----------------------------|-------|-------|-------|------|
| SPI master | | | | | |
| T_{SPICYC} | SPI cycle time | 22.2 | - | - | ns |
| $t_{SPICLKH}$ | SPICLK HIGH time | 11.09 | - | 11.14 | ns |
| $t_{SPICLKL}$ | SPICLK LOW time | 11.09 | - | 11.14 | ns |
| t_{SPIDSU} | SPI data set-up time | <tbd> | <tbd> | <tbd> | ns |
| t_{SPIDH} | SPI data hold time | <tbd> | <tbd> | <tbd> | ns |
| t_{SPIQV} | SPI data output valid time | - | - | 14 | ns |
| t_{SPIOH} | SPI output data hold time | 9.9 | - | - | ns |
| SPI slave | | | | | |
| T_{SPICYC} | SPI cycle time | <tbd> | 40 | <tbd> | ns |
| $t_{SPICLKH}$ | SPICLK HIGH time | <tbd> | 20 | <tbd> | ns |
| $t_{SPICLKL}$ | SPICLK LOW time | <tbd> | 20 | <tbd> | ns |
| t_{SPIDSU} | SPI data set-up time | <tbd> | <tbd> | <tbd> | ns |
| t_{SPIDH} | SPI data hold time | <tbd> | <tbd> | <tbd> | ns |
| t_{SPIQV} | SPI data output valid time | <tbd> | <tbd> | 14 | ns |
| t_{SPIOH} | SPI output data hold time | 9.9 | - | - | ns |

Remark: Note that the signal names SCK, MISO, and MOSI correspond to signals on pins SPI_SCK, SPI_MOSI, and SPI_MISO in the following SPI timing diagrams.

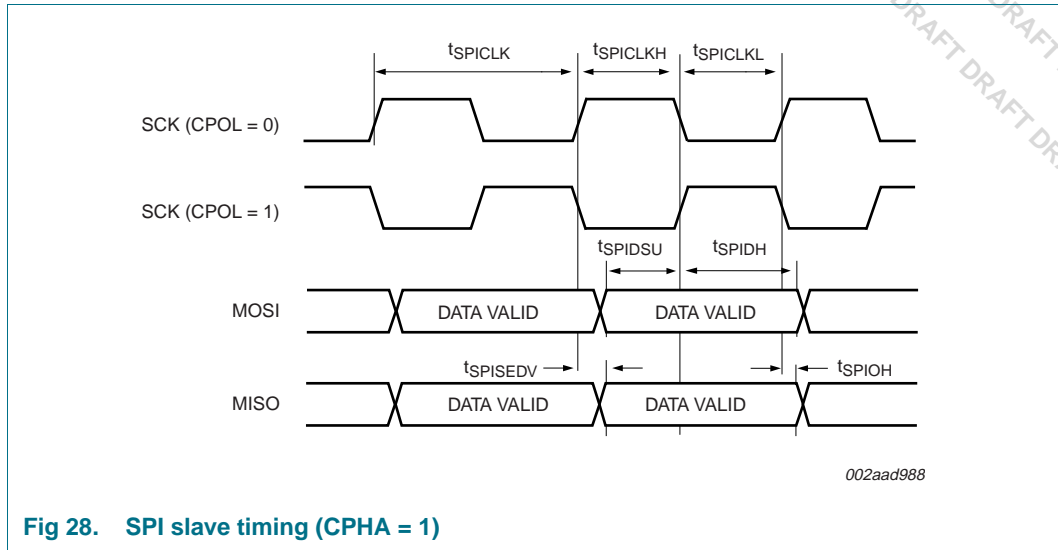


Fig 28. SPI slave timing (CPHA = 1)

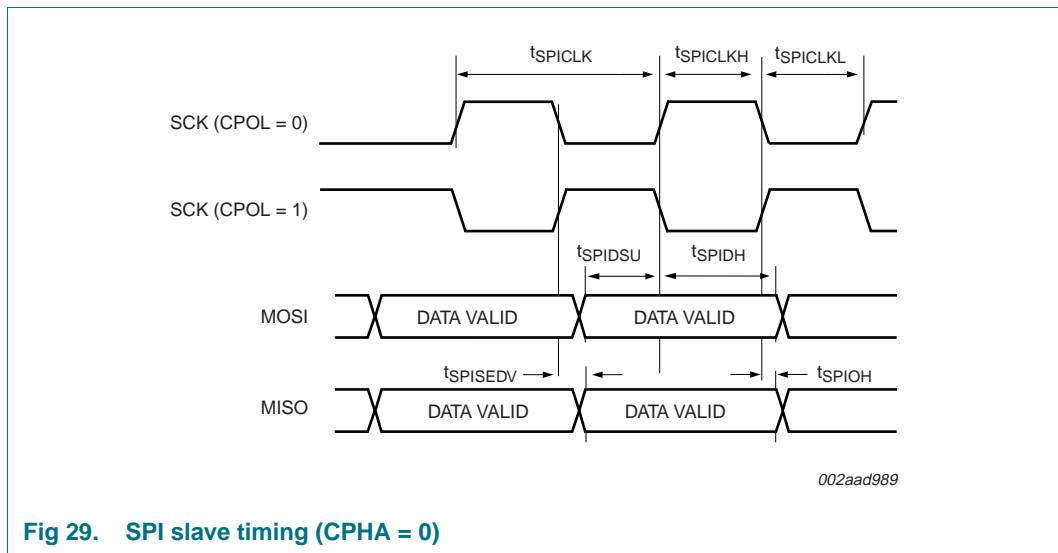


Fig 29. SPI slave timing (CPHA = 0)

10.2.2.1 Texas Instruments synchronous serial mode (SSP mode)

Table 29. Dynamic characteristic: SPI interface (SSP mode)

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{DD(10)}$ (SUP3) over specified ranges.^[1]

| Symbol | Parameter | Conditions | Min | Typ ^[2] | Max | Unit |
|---------------------|----------------------|---|-----|--------------------|-----|------|
| $t_{su}(SPI_MISO)$ | SPI_MISO set-up time | $T_{amb} = 25\text{ }^{\circ}\text{C}$; measured in SPI Master mode; see Figure 30 | - | 11 | - | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

Remark: Note that the signal names SCK, MISO, and MOSI correspond to signals on pins SPI_SCK, SPI_MOSI, and SPI_MISO in the following SPI timing diagram.

10.2.3 I²S-interface

Table 30. Dynamic characteristics: I²S-interface pins

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial applications

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------------|------------------------|-----------------------------------|------|------|------|------|
| common to input and output | | | | | | |
| $T_{cy}(clk)$ | clock cycle time | | <td> | <td> | <td> | ns |
| t_f | fall time | | 3.5 | <td> | <td> | ns |
| t_r | rise time | | 3.5 | <td> | <td> | ns |
| output | | | | | | |
| t_{WH} | pulse width HIGH | | <td> | <td> | <td> | ns |
| t_{WL} | pulse width LOW | | <td> | <td> | <td> | ns |
| $t_{v(Q)}$ | data output valid time | on pin I2STX_DATAx ^[1] | <td> | <td> | <td> | ns |
| | | on pin I2STX_WSx ^[1] | <td> | <td> | <td> | ns |
| input | | | | | | |
| $t_{su(D)}$ | data input set-up time | on pin I2SRX_DATAx ^[1] | <td> | <td> | <td> | ns |
| | | on pin I2SRX_WSx ^[1] | <td> | <td> | <td> | ns |
| $t_h(D)$ | data input hold time | on pin I2SRX_DATAx ^[1] | <td> | <td> | <td> | ns |
| | | on pin I2SRX_WSx ^[1] | <td> | <td> | <td> | ns |

[1] x = 0 or 1.

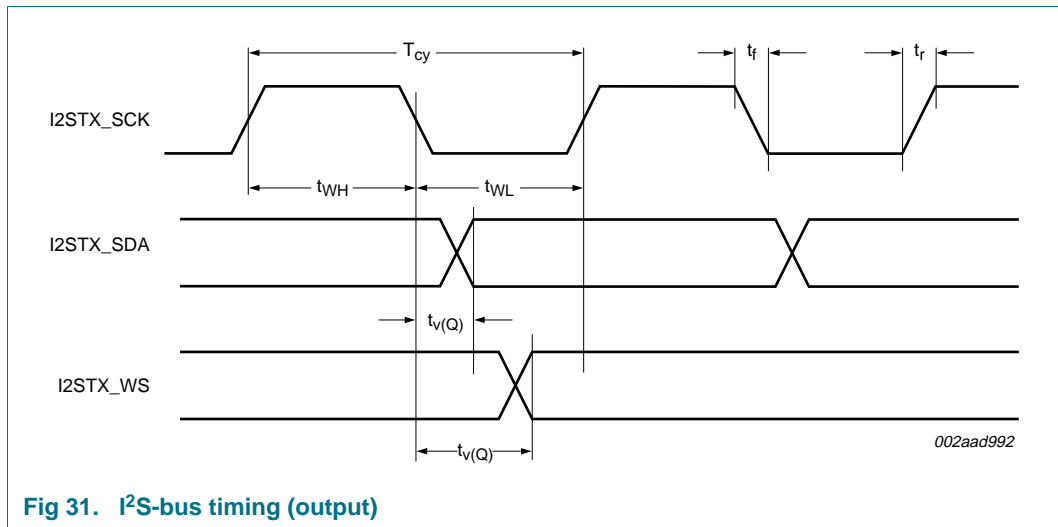


Fig 31. I²S-bus timing (output)

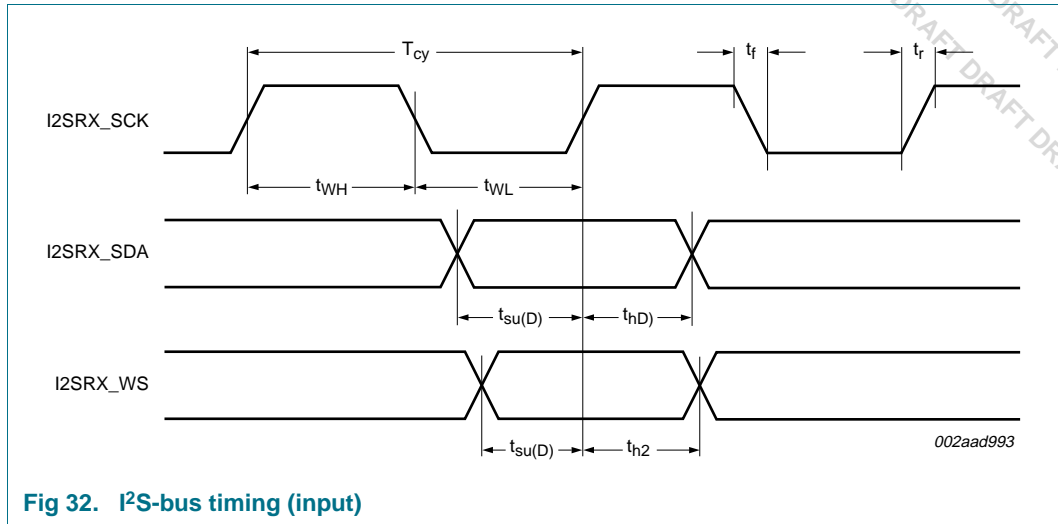


Fig 32. I²S-bus timing (input)

10.2.4 I²C-bus

Table 31. Dynamic characteristic: I²C-bus pins

$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$. [1]

| Symbol | Parameter | Conditions | Min | Typ ^[2] | Max | Unit |
|--------------|--|----------------------|---------------------------|--------------------|------|---------------|
| f_{SCL} | SCL clock frequency | Standard mode | 0 | <td> | 100 | kHz |
| | | Fast mode | 0 | <td> | 400 | kHz |
| $t_{f(o)}$ | output fall time | V_{IH} to V_{IL} | $20 + 0.1 \times C_b$ [3] | - | - | ns |
| t_r | rise time | Standard mode | <td> | <td> | 1000 | ns |
| | | Fast mode | $20 + 0.1 \times C_b$ [3] | <td> | 300 | ns |
| t_f | fall time | Standard mode | <td> | <td> | 300 | ns |
| | | Fast mode | $20 + 0.1 \times C_b$ [3] | <td> | 300 | ns |
| t_{BUF} | bus free time between a STOP and START condition | - | <td> | <td> | <td> | |
| t_{LOW} | LOW period of the SCL clock | Standard mode | 4.7 | <td> | <td> | μs |
| | | Fast mode | 1.3 | <td> | <td> | μs |
| $t_{HD,STA}$ | hold time (repeated) START condition | - | <td> | <td> | <td> | |
| t_{HIGH} | HIGH period of the SCL clock | Standard mode | 4.0 | <td> | <td> | μs |
| | | Fast mode | 0.6 | <td> | <td> | μs |
| $t_{SU,DAT}$ | data set-up time | Standard mode | 250 | <td> | <td> | ns |
| | | Fast mode | 100 | <td> | <td> | ns |
| $t_{SU,STA}$ | set-up time for a repeated START condition | - | <td> | <td> | <td> | |
| $t_{SU,STO}$ | set-up time for STOP condition | Standard mode | 4.0 | <td> | <td> | μs |
| | | Fast mode | 0.6 | <td> | <td> | μs |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

10.2.5 USB interface

Table 32. Dynamic characteristics: USB pins (high-speed)

$C_L = 50\text{ pF}$; $R_{pu} = 1.5\text{ k}\Omega$ on $D+$ to $V_{DD(I/O)}$ (SUP3), unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|---|---|----------|-----|------|------|
| t_r | rise time | 10 % to 90 % | <td> | - | <td> | ns |
| t_f | fall time | 10 % to 90 % | <td> | - | <td> | ns |
| t_{FRFM} | differential rise and fall time matching | t_r / t_f | - | - | <td> | % |
| V_{CRS} | output signal crossover voltage | | <td> | - | <td> | V |
| t_{FEOPT} | source SE0 interval of EOP | see Figure 34 | <td> | - | <td> | ns |
| t_{FDEOP} | source jitter for differential transition to SE0 transition | see Figure 34 | <td> | - | <td> | ns |
| t_{JR1} | receiver jitter to next transition | | <td> | - | <td> | ns |
| t_{JR2} | receiver jitter for paired transitions | 10 % to 90 % | <td> | - | <td> | ns |
| t_{EOPR1} | EOP width at receiver | must reject as EOP; see Figure 34 | [1] <td> | - | - | ns |
| t_{EOPR2} | EOP width at receiver | must accept as EOP; see Figure 34 | [1] <td> | - | - | ns |

[1] Characterized but not implemented as production test. Guaranteed by design.

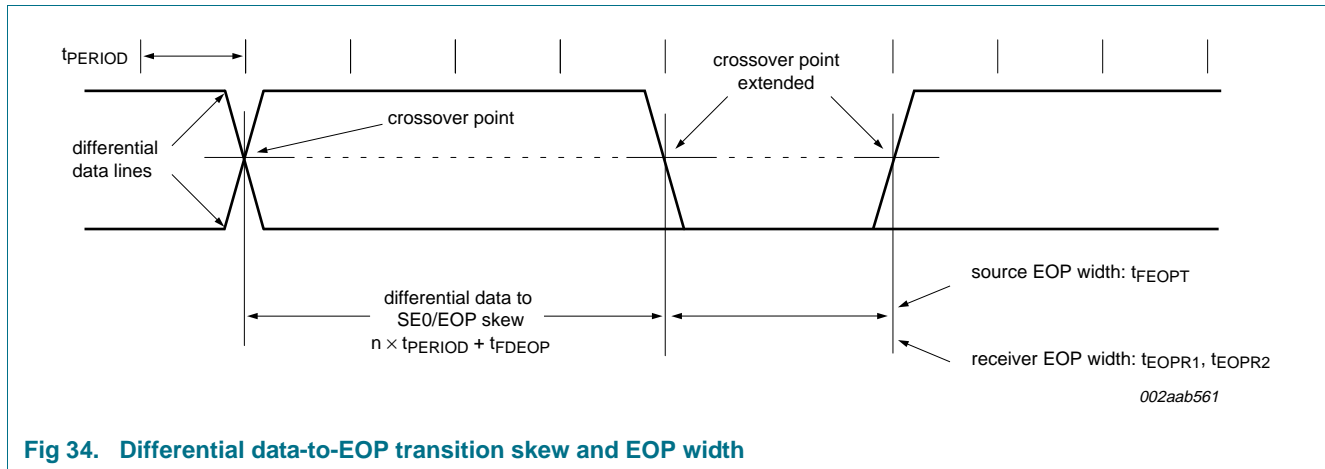


Fig 34. Differential data-to-EOP transition skew and EOP width

10.2.6 10-bit ADC

Table 33: Dynamic characteristics: 10-bit ADC

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|--------------------|-------------------|-----|-----|------|--------------|
| f_s | sampling frequency | 10 bit resolution | 400 | - | - | kSamples/s |
| | | 2 bit resolution | - | - | 1500 | kSamples/s |
| t_{conv} | conversion time | 10 bit resolution | - | - | 11 | clock cycles |
| | | 2 bit resolution | 3 | - | - | clock cycles |

10.3 Analog die/audio system

Table 34. Dynamic characteristics of Class AB amplifier

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified. $V_{DD(ADC)} = 3.3\text{ V}$ on pin ADC_VDDA33.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|--|--|-----|-----|------|---------|
| V_o | output voltage | HP unloaded | - | 800 | - | mV(RMS) |
| P_o | output power | per channel; $R_L=16\text{ }\Omega$ | | | 23.5 | mW |
| (THD+N)/S | Total harmonic distortion plus noise-to-signal ratio | at 0 dBFS; $f_{in} = 1\text{ kHz}$; [1] $R_L=16\text{ }\Omega$ | - | -60 | - | dB |
| | | at -60 dBFS; $f_{in} = 1\text{ kHz}$; $R_L=16\text{ }\Omega$ | - | -40 | -30 | dBA |
| S/N | Signal-to-noise ratio | [1] | - | 100 | - | dBA |
| PSRR | power supply ripple rejection | | - | 6 | - | dB |
| $\alpha_{ct(ch)}$ | channel crosstalk | $R_L=16\text{ }\Omega$; between left channel and right channel | - | -55 | - | dB |

[1] Measured with 20 kHz block filter.

Table 35: Dynamic characteristic for analog in

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|--|---|-----|-----|-----|------------|
| B | Bandwidth | | - | - | 20 | kHz |
| Tuner | | | | | | |
| (THD+N)/S | Total harmonic distortion plus noise-to-signal ratio | at 0 dBFS; $f_{in} = 1\text{ kHz}$; Line input level = 1 V; PGA setting +12 dB; external resistor of 36 k Ω | - | -83 | -80 | dB |
| | | at 0 dBFS; $f_{in} = 1\text{ kHz}$; Line input level = 1 V, PGA setting 0 dB | - | -70 | - | dB |
| | | at -60 dBFS; A-weighted; $f_{in} = 1\text{ kHz}$; Line input level = 1mV, PGA setting 0dB | - | -34 | -30 | dBA |
| S/N | Signal-to-noise ratio | A-weighted; line input = 1 V, PGA setting 0 dB | 90 | 94 | - | dBA |
| Z_i | input impedance | line in (tuner mode) | - | 12 | - | k Ω |
| Microphone | | | | | | |
| THD | total harmonic distortion | $V_i = 20\text{ mV}$; $f_{in} = 1\text{ kHz}$ | - | -70 | -60 | dB |
| | | $V_i = 0.3\text{ mV}$; $f_{in} = 1\text{ kHz}$ | - | -90 | -80 | dB |
| Z_i | input impedance | microphone mode | - | 5 | - | k Ω |

12. Marking

Table 37. LPC3152/3154 Marking

| Line | Marking | Description |
|------|--------------|-------------|
| A | LPC3152/3154 | BASIC_TYPE |

13. Package outline

TFBGA208: plastic thin fine-pitch ball grid array package; 208 balls; body 12 x 12 x 0.7 mm

SOT930-1

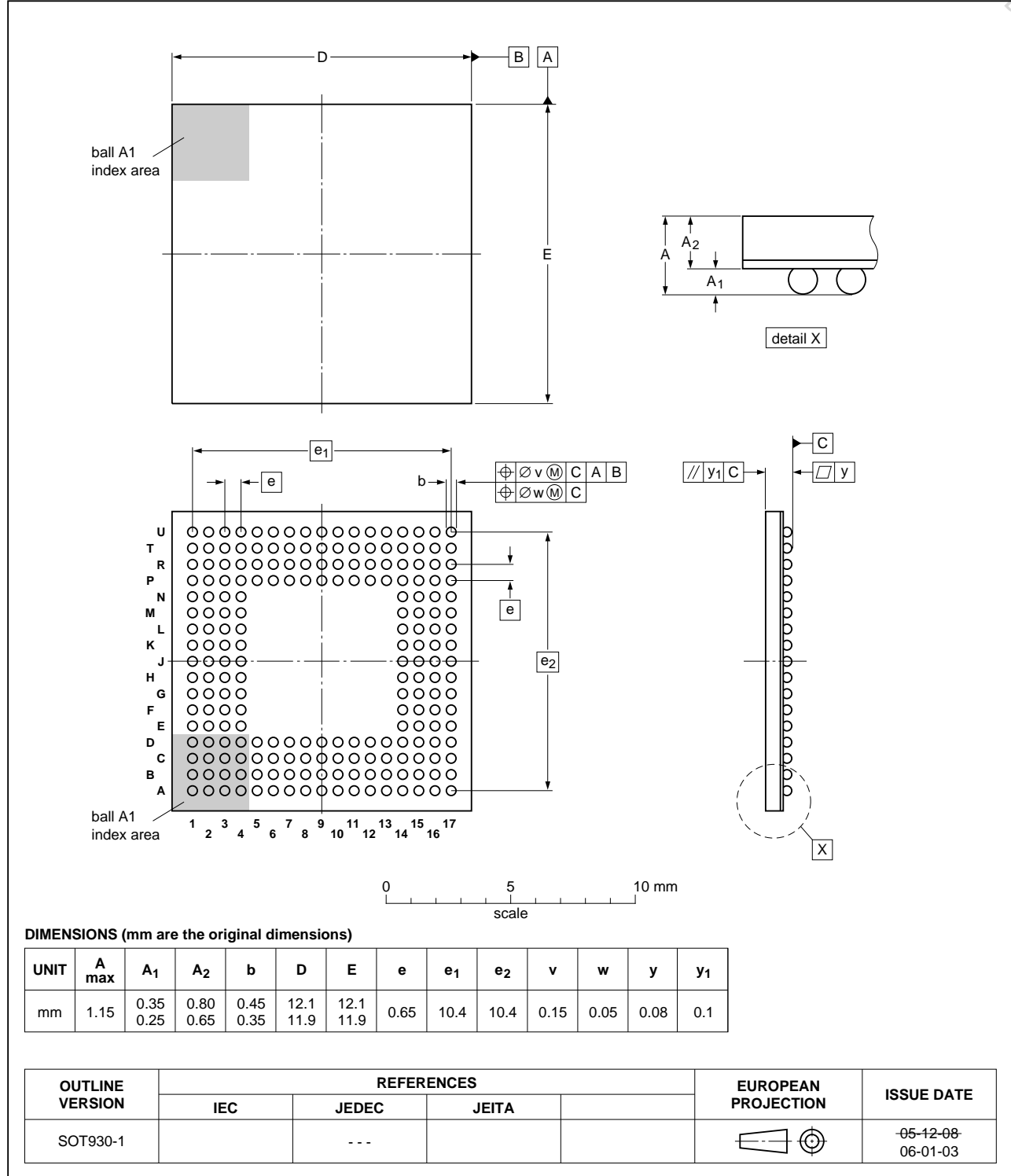


Fig 35. LPC3152/3154 TFBGA208 package outline

14. Abbreviations

Table 38: Abbreviations

| Acronym | Description |
|----------|--------------------------------------|
| ADC | Analog-to-Digital Converter |
| ADC10B | 10 Bit Analogue to Digital Converter |
| AES | Advanced Encryption Standard |
| AVC | Analog Volume Control |
| BIU | Bus Interface Unit |
| CBC | Cipher Block Chaining |
| CD | Compact Disk |
| CGU | Clock Generation Unit |
| DFU | Device Firmware Upgrade |
| DMA | Direct Memory Access Controller |
| DRM | Digital Rights Management |
| ECC | Error Correction Code |
| FIR | Finite Input Response |
| HP | Headphones |
| IOCONFIG | Input Output Configuration |
| ROM | Read Only Memory |
| IrDA | Infrared Data Association |
| JTAG | Joint Test Action Group |
| ISRAM | Internal Static RAM Memory |
| JTAG | Joint Test Action Group |
| LCD | Liquid Crystal Display |
| LDO | Low Drop voltage Output regulator |
| LNA | Low-Noise Amplifier |
| MMU | Memory Management Unit |
| NTC | Negative Temperature Coefficient |
| OTP | One-Time Programmable Memory |
| PCM | Pulse Code Modulation |
| PGA | Programmable Gain Amplifier |
| PHY | Physical Layer |
| PLL | Phase Locked Loop |
| PSU | Power Supply Unit |
| PWM | Pulse Width Modulation |
| RNG | Random Number Generator |
| SDC | |
| SHA1 | Secure Hash Algorithm 1 |
| SIR | Serial IrDA |
| SPI | Serial Peripheral Interface |
| SSI | Serial Synchronous Interface |
| SysCReg | System Control Registers |

15. Revision history

Table 39: Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------------|--------------|--|---------------|-------------------|
| LPC3152_3154 v.0.12 | <tbd> | Preliminary data sheet | - | LPC3152_3154_0.11 |
| Modifications: | | <ul style="list-style-type: none"> Reset state of JTAG pins and GPIO0, GPIO1, and GPIO2 pins updated in Table 4. Document template updated. Digital I/O level for pin CLOCK_OUT corrected in Table 4. USB Hi-speed logo added. USB-IF TestID numbers added in Section 6.10. | | |
| LPC3152_3154_0.11 | <tbd> | Preliminary data sheet | - | - |

16. Legal information

16.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b)

whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

| | | | | | |
|----------|---|-----------|-----------|--|-----------|
| 1 | General description | 1 | 6.31 | System control registers | 39 |
| 2 | Features and benefits | 1 | 6.32 | Audio Subsystem (ADSS) | 39 |
| 2.1 | Key features | 1 | 6.32.1 | I ² S/O digital audio input/output | 40 |
| 3 | Ordering information | 2 | 7 | Functional description of the analog die blocks | 41 |
| 3.1 | Ordering options | 3 | 7.1 | Analog die | 41 |
| 4 | Block diagram | 4 | 7.2 | Audio codec | 42 |
| 5 | Pinning information | 5 | 7.2.1 | Stereo Digital-to-Analog Converter (SDAC) | 42 |
| 5.1 | Pinning | 5 | 7.2.2 | Class AB headphone amplifier | 43 |
| 6 | Functional description | 16 | 7.2.3 | Stereo Analog-to-Digital Converter (SADC) for Audio | 43 |
| 6.1 | ARM926EJ-S | 16 | 7.3 | Li-ion charger | 44 |
| 6.2 | Memory map | 17 | 7.4 | USB charge pump (host mode) | 45 |
| 6.2.1 | Analog die memory organization | 17 | 7.5 | Power Supply Unit (PSU) | 45 |
| 6.3 | JTAG | 18 | 7.6 | Real-Time Clock (RTC) | 47 |
| 6.4 | NAND flash controller | 18 | 8 | Limiting values | 48 |
| 6.5 | Multi-Port Memory Controller (MPMC) | 20 | 9 | Static characteristics | 48 |
| 6.6 | External Bus Interface (EBI) | 21 | 9.1 | Digital die | 48 |
| 6.7 | Internal ROM Memory | 21 | 9.2 | Analog die | 54 |
| 6.8 | Internal RAM memory | 22 | 9.2.1 | PSU | 54 |
| 6.9 | Memory Card Interface (MCI) | 23 | 9.2.1.1 | PSU_VOUT1 efficiency | 56 |
| 6.10 | Universal Serial Bus 2.0 High Speed On-The-Go (OTG) | 23 | 9.2.1.2 | PSU_VOUT2 efficiency | 57 |
| 6.11 | DMA controller | 24 | 9.2.2 | Li-ion charger | 59 |
| 6.12 | Interrupt controller | 25 | 10 | Dynamic characteristics | 60 |
| 6.13 | Multi-layer AHB | 25 | 10.1 | Digital die | 60 |
| 6.14 | APB bridge | 27 | 10.1.1 | LCD controller | 60 |
| 6.15 | Clock Generation Unit (CGU) | 27 | 10.1.1.1 | Intel 8080 mode | 60 |
| 6.16 | Watchdog Timer (WDT) | 29 | 10.1.1.2 | Motorola 6800 mode | 61 |
| 6.17 | Input/Output configuration module (IOCONFIG) | 30 | 10.1.1.3 | Serial mode | 62 |
| 6.18 | 10-bit Analog-to-Digital Converter (ADC10B) | 30 | 10.1.2 | SRAM controller | 63 |
| 6.19 | Event router | 31 | 10.1.3 | SDRAM controller | 65 |
| 6.20 | Random Number Generator (RNG) | 32 | 10.2 | NAND flash memory controller | 69 |
| 6.21 | AES decryption (LPC3154 only) | 32 | 10.2.1 | Crystal oscillator | 70 |
| 6.22 | Secure One-Time Programmable (OTP) memory | 32 | 10.2.2 | SPI | 70 |
| 6.23 | Serial Peripheral Interface (SPI) | 32 | 10.2.2.1 | Texas Instruments synchronous serial mode (SSP mode) | 72 |
| 6.24 | Universal Asynchronous Receiver Transmitter (UART) | 33 | 10.2.3 | I ² S-interface | 74 |
| 6.25 | Pulse Code Modulation (PCM) interface | 33 | 10.2.4 | I ² C-bus | 75 |
| 6.26 | LCD interface | 34 | 10.2.5 | USB interface | 77 |
| 6.27 | I ² C-bus master/slave interface | 34 | 10.2.6 | 10-bit ADC | 77 |
| 6.28 | LCD/NAND flash/SDRAM multiplexing | 35 | 10.3 | Analog die/audio system | 78 |
| 6.28.1 | Pin connections | 35 | 11 | Application information | 79 |
| 6.28.2 | Multiplexing between LCD and MPMC | 37 | 12 | Marking | 80 |
| 6.28.3 | Supply domains | 38 | 13 | Package outline | 81 |
| 6.29 | Timer module | 39 | 14 | Abbreviations | 82 |
| 6.30 | Pulse Width Modulation (PWM) module | 39 | 15 | Revision history | 84 |

continued >>

