XK-1 Hardware Manual

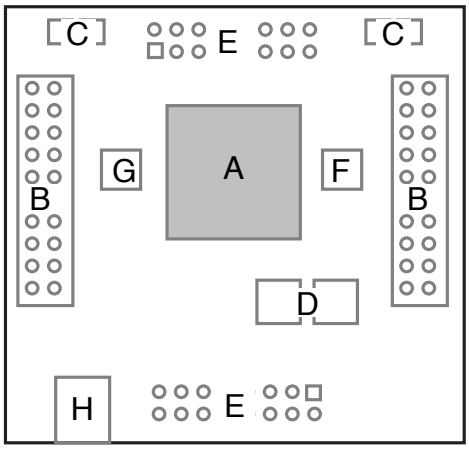
Version 1.2.2

XMOS

Publication Date: 2009/12/21

1 Introduction

The XK-1 is a low cost development board intended for exploring and designing event-driven processor designs. It comprises a single XS1-L1 device, 128KBytes SPI FLASH memory, four LEDs and two press-button switches. Two XMOS Links allow you to link multiple XK-1 boards together in a chain, two I/O expansion areas are provided for connecting additional components to the XK-1, and an XTAG-2 debug adapter can be connected to debug the XK-1 board with a PC. The diagram below shows the layout of these components on the card.



A	XS1-L1 Device	**E**	16-way Expansion Areas
B	XSYS IDC Headers	**F**	SPI Flash Memory
C	User LEDs	**G**	20MHz Crystal Oscillator
D	Push-Button Switches	**H**	5V PSU

An XK-1 board can be powered from the USB connection using an XTAG-2 debug adapter or by an external 5V power supply. Additional boards that have been chained together may be able to be powered by the XTAG-2 (depending on the length of the chain) or from an external 5V power supply.

The rest of this document provide a detailed description of these components.

2 XS1-L1 Device [A]

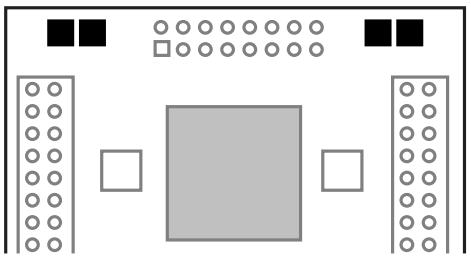
The XK-1 is based on a single XS1-L1 device in a 128TQFP package. The XS1-L1 consists of a single XCore, which comprises an event-driven multi-threaded processor with tightly integrated general purpose I/O pins and 64 KBytes of on-chip RAM. The pins are brought out of the package and connected to the card's components as follows:

- Four yellow LEDs
- Two push-button switches
- Two XSYS 20-way IDC headers (one male and one female)
- An SPI interface to FLASH memory
- 12 I/O pins to the expansion areas

The processor has ports that are directly connected to the I/O pins. Examples of how to write software that interfaces over these ports with the XK-1 components is provided in the document *Programming XC for XMOS Devices* available from the XMOS website.

3 User LEDs [C]

The XK-1 provides four user LEDs that can be driven by software. The layout of these LEDs is shown below.



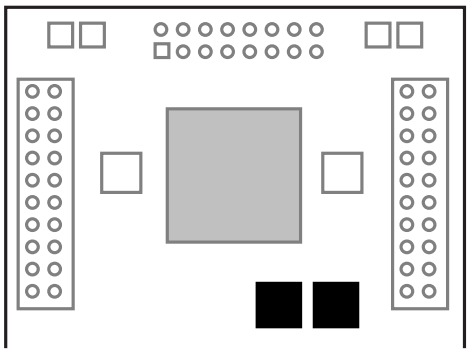
Each LED is connected to a different pin, all of which are mapped to ports as described in the table on the next page.

Pin	Port	Processor
XD28	P4F0	PORT_LED
XD29	P4F1	PORT_LED
XD30	P4F2	PORT_LED
XD31	P4F3	PORT_LED

The LED pins are active high.

4 Push-Button Switches [D]

The XK-1 provides two push-button switches whose states can be sampled at any time by software. The layout of these switches is shown below.



The switches are connected to two pins, which are mapped to ports as described in the table on the next page.

Pin	Port	Processor
XD34	P1K0	PORT_BUT_1
XD35	P1L0	PORT_BUT_2

The push-button switch pins are active low.

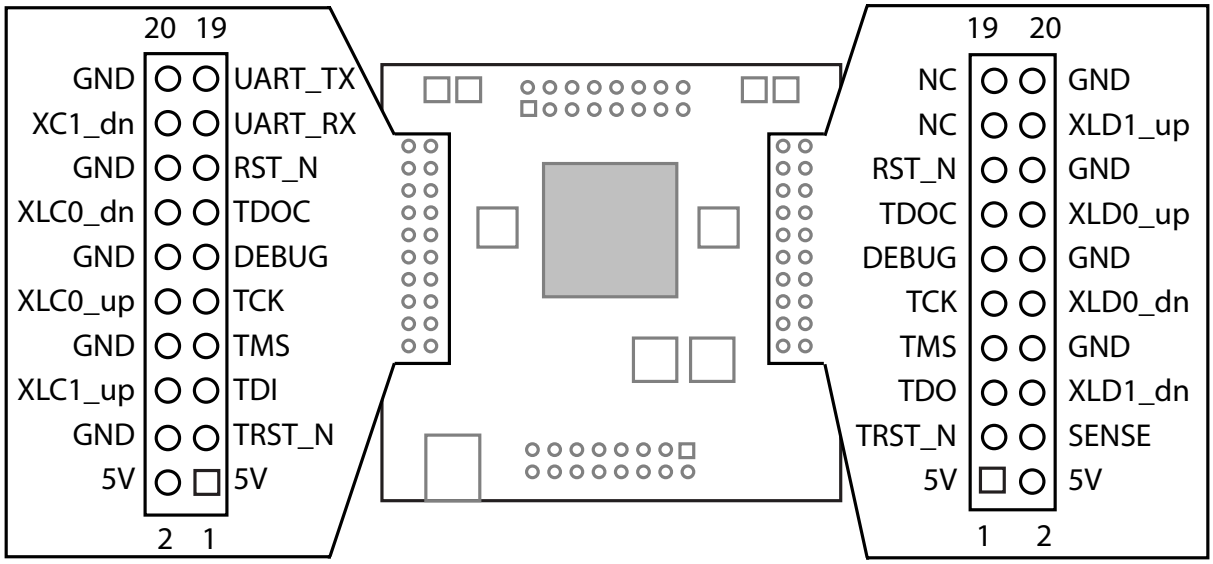
5 XSYS Connectors [B]

The XK-1 includes two XSYS 20-way IDC Headers, which can be used to link to an XTAG-2 debug adapter for debugging programs on the board, or to connect additional XK-1 boards together in a chain.

The XSYS connector provides pins for JTAG control, system reset, processor debug, two UART links and two XMOS Links.

Pin	Signal	Direction	Description
1	3V3	Target to Host	Power
2	3V3	Target to Host	Power
3	TRST_N	Host to Target	JTAG Test Reset - Active Low
4	SENSE	N/A	Ground on TARGET, pull up on HOST
5	TDI/TDO	Host to Target	JTAG Test Data
6	XLC1_out/XLD1_in	Target to Host	XMOS Link
7	TMS	Host to Target	JTAG Test Mode Select
8	GND	N/A	Ground
9	TCK	Host to Target	JTAG Test Clock
10	XLC0_out/XLD0_in	Target to Host	XMOS Link
11	DEBUG	Bidirectional	Debug
12	GND	N/A	Ground
13	TDOC	Target to Host	JTAG Test Data
14	XLC0_in/XLD0_out	Host to Target	XMOS Link
15	RST_N	Host to Target	System Reset - Active Low.
16	GND	N/A	Ground
17	UART_RX	Host to Target	Serial Port (Down)
18	XLC1_in/XLD1_out	Host to Target	XMOS Link
19	UART_TX	Target to Host	Serial Port (Up)
20	GND	N/A	Ground

The routing of these I/O pins along with the power pins is shown on the following page.



The XTAG-2 converts between XSYS and USB 2.0, allowing the XK-1 to be connected to most PCs. On power on, the XS1-L1 boots from the on-board flash memory. The XS1-L1 can then be put into JTAG mode by the PC, which then boots another program.

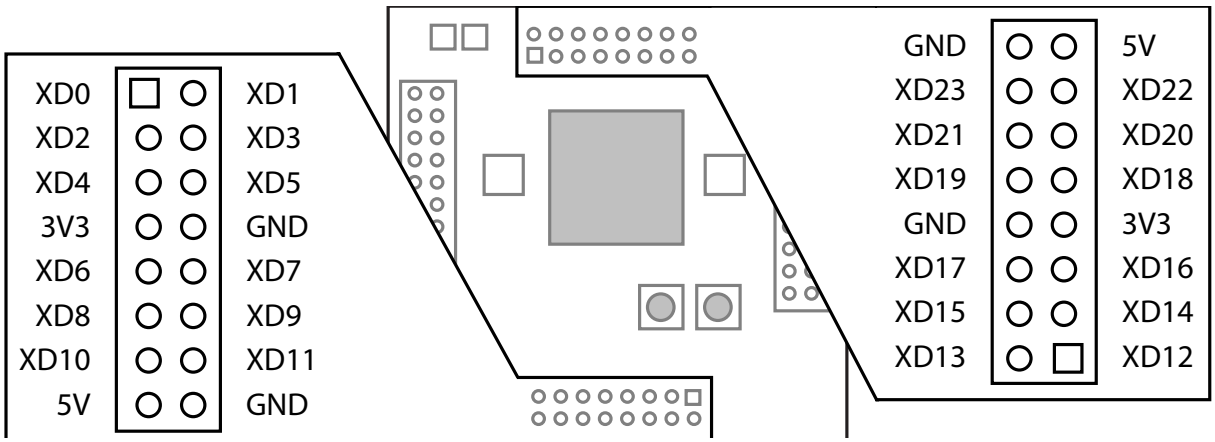
No UART hardware is provided. Instead, two UART pins are mapped to ports, as shown in the table below.

Pin	Port	Processor
XD24	P1I0	PORT_UART_RX
XD25	P1J0	PORT_UART_TX

If a UART is required, it can be implemented in software by sampling and driving these ports at the required rate. The XTAG-2 performs a UART-to-USB conversion on these pins, which is interfaced by a proprietary XMOS terminal emulator.

6 Expansion Areas [E]

The I/O pins of the processor are brought out to expansion areas on the top and bottom of the card. These areas have 0.1" pitch through-plated holes and are populated with 0.1" right-angle IDC male connectors. The routing of I/O and power pins in the headers is shown below.



Each expansion header provides a bank of 12 I/O pins, which are mapped to the ports as described in the table on the next page, and four power/ground pins.

Pin	Port			Processor
	1b	4b	8b	
XD0	P1A0			GPIO_A
XD1	P1B0			
XD2		P4A0	P8A0	
XD3		P4A1	P8A1	
XD4		P4B0	P8A2	
XD5		P4B1	P8A3	
XD6		P4B2	P8A4	
XD7		P4B3	P8A5	
XD8		P4A2	P8A6	
XD9		P4A3	P8A7	
XD10	P1C0			
XD11	P1D0			
XD12	P1E0			GPIO_B
XD13	P1F0			
XD14		P4C0	P8B0	
XD15		P4C1	P8B1	
XD16		P4D0	P8B2	
XD17		P4D1	P8B3	
XD18		P4D2	P8B4	
XD19		P4D3	P8B5	
XD20		P4C2	P8B6	
XD21		P4C3	P8B7	
XD22	P1G0			
XD23	P1H0			

Eight pins from each bank can be configured as either two 4-bit ports or a single 8-bit port. The A and B expansion headers can alternatively be used together as a single 16-bit port.

Narrower ports take priority over the pins where multiple ports are mapped to the same pins.

6.1 XMOS Link Configuration

Some of the I/O pins on the processor are configured as an additional 2-bit XMOS Link. The mapping of XMOS Links to the pins is shown in the table below.

Pin	XMOS Link
XD52	XLC1_in
XD53	XLC0_in
XD54	XLC0_out
XD55	XLC1_out
XD64	XLD1_in
XD65	XLD0_in
XD66	XLD0_out
XD67	XLD1_out

Some of the I/O pins on the expansion areas can also be configured as 2-bit XMOS Links. The mapping of XMOS Links to the headers is shown in the table below.

Pin	XMOS Link	Expansion Area
XD4	XLA1_out	GPIO_A
XD5	XLA0_out	
XD6	XLA0_in	
XD7	XLA1_in	
XD16	XLB1_out	GPIO_B
XD17	XLB0_out	
XD18	XLB0_in	
XD20	XLB1_in	

7 SPI Flash Memory [F]

The XK-1 provides 128KBytes of Serial Peripheral Interface (SPI) FLASH memory, which is interfaced by the four 1-bit connections described in the table below.

Pin	Port	Processor
XD36	P1M0	PORT_SPI_MISO
XD37	P1N0	PORT_SPI_SS
XD38	P1O0	PORT_SPI_CLK
XD39	P1P0	PORT_SPI_MOSI

The Tools include the XFLASH utility for programming compiled programs into the flash memory. XK-1 designs may also access the FLASH memory at run-time by interfacing with the above ports.

8 20MHz Crystal Oscillator [G]

The XS1-L1 is clocked at 20MHz by a crystal oscillator on the card. Each processor is clocked at 400MHz, the I/O ports at 100MHz, by an on-chip phase-locked loop (PLL).

9 Power Connector [H]

An XK-1 can be powered from the XTAG-2 debug adapter or an external 5V power supply. Additional boards that have been chained together may be able to be powered by the XTAG-2 (depending on the length of the chain) or from an external 5V power supply.

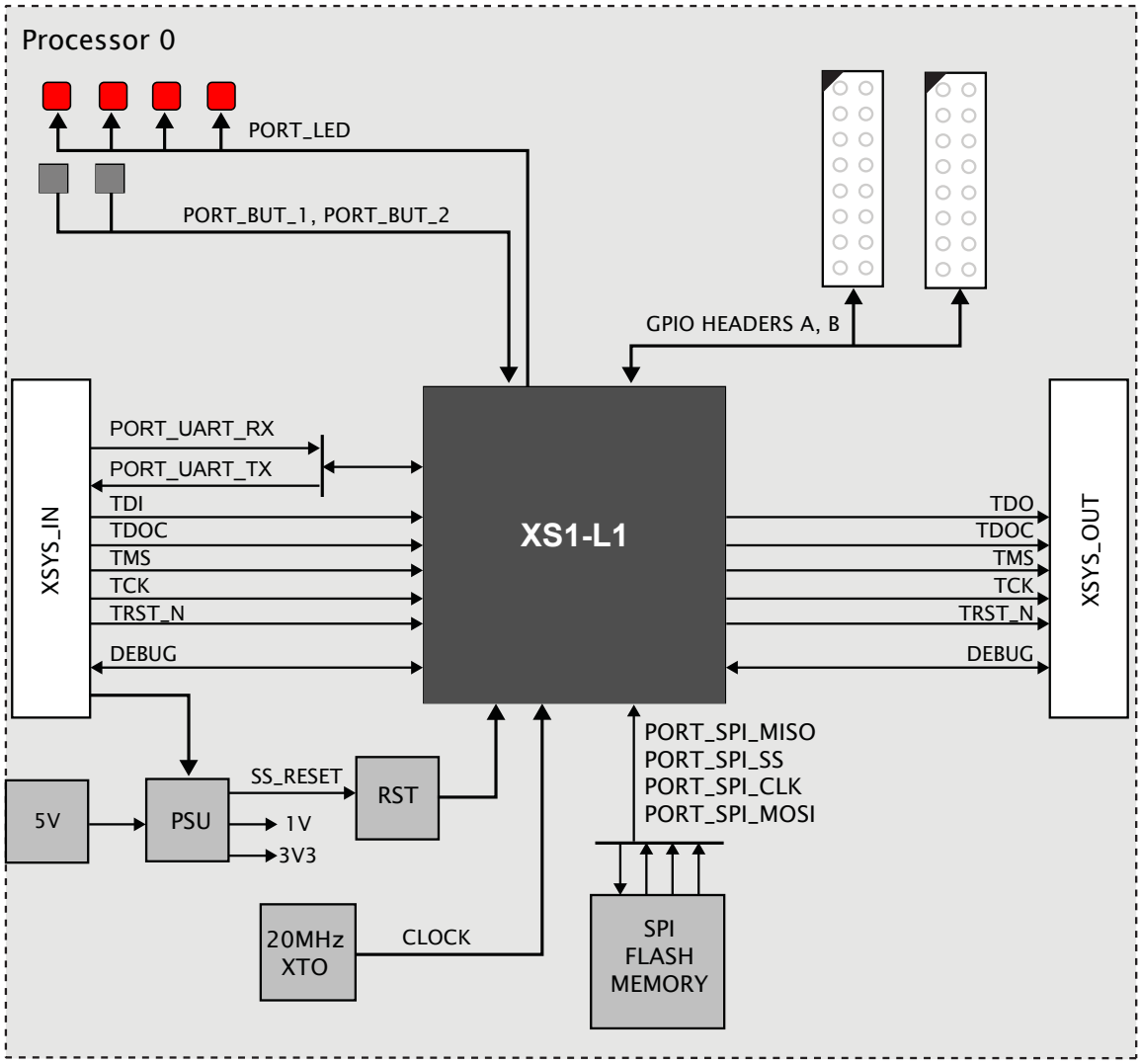
The voltage is converted by the on-board regulator to the 1V and 3V3 supplies used by the components.

10 Dimensions

The XK-1 dimensions are 50 x 50mm. The mounting holes are 3mm in diameter.

11 XK-1 Block Diagram

The diagram below shows how the XK-1 components are connected to the XS1-L1.



11.1 I/O Port-to-Pin Mapping

The table on the following page provides a full description of the port-to-pin mappings described throughout this document.

Pin	Port				Processor
	1b	4b	8b	16b	
XD0	P1A0				GPIO_A
XD1	P1B0				
XD2		P4A0	P8A0	P16A0	
XD3		P4A1	P8A1	P16A1	
XD4		P4B0	P8A2	P16A2	
XD5		P4B1	P8A3	P16A3	
XD6		P4B2	P8A4	P16A4	
XD7		P4B3	P8A5	P16A5	
XD8		P4A2	P8A6	P16A6	
XD9		P4A3	P8A7	P16A7	
XD10	P1C0				
XD11	P1D0				
XD12	P1E0				GPIO_B
XD13	P1F0				
XD14		P4C0	P8B0	P16A8	
XD15		P4C1	P8B1	P16A9	
XD16		P4D0	P8B2	P16A10	
XD17		P4D1	P8B3	P16A11	
XD18		P4D2	P8B4	P16A12	
XD19		P4D3	P8B5	P16A13	
XD20		P4C2	P8B6	P16A14	
XD21		P4C3	P8B7	P16A15	
XD22	P1G0				
XD23	P1H0				
XD24	P1I0				PORT_UART_RX
XD25	P1J0				PORT_UART_TX
XD26		P4E0	P8C0		
XD27		P4E1	P8C1		
XD28		P4F0	P8C2		PORT_LED
XD29		P4F1	P8C3		
XD30		P4F2	P8C4		
XD31		P4F3	P8C5		
XD32		P4E2	P8C6		
XD33		P4E3	P8C7		
XD34	P1K0				PORT_BUT_1
XD35	P1L0				PORT_BUT_2
XD36	P1M0		P8D0		PORT_SPI_MISO
XD37	P1N0		P8D1		PORT_SPI_SS
XD38	P1O0		P8D2		PORT_SPI_CLK
XD39	P1P0		P8D3		PORT_SPI_MOSI
XD40			P8D4		
XD41			P8D5		
XD42			P8D6		
XD43			P8D7		
XD52					XLC1_in
XD53					XLC0_in
XD54					XLC0_out
XD55					XLC1_out
XD64					XLD1_in
XD65					XLD0_in
XD66					XLD0_out
XD67					XLD1_out

12 XK-1 XN File

The XK-1 XN file is a platform specific file, similar to a `# define`. It defines the type of event-driven processor device on the board, and can be used to map the hardware features on the board to generic port identifiers, simplifying the process of writing projects and porting between platforms.

The following table lists the defined identifiers defined in the XMOS Tools version 9.9.1 for the XK-1:

Port Location	Generic Identifier
XS1_PORT_1I	PORT_UART_RX
XS1_PORT_1J	PORT_UART_TX
XS1_PORT_1K	PORT_BUT_1
XS1_PORT_1L	PORT_BUT_2
XS1_PORT_1M	PORT_SPI_MISO
XS1_PORT_1N	PORT_SPI_SS
XS1_PORT_1O	PORT_SPI_CLK
XS1_PORT_1P	PORT_SPI_MOSI
XS1_PORT_4F	PORT_LED

To provide backward compatibility with source code written using the version 9.9.0 XN file, add the following to your source:

```
#ifdef PORT\_BUT_1
    // 9.9.1 XN names found, add 9.9.0 XN names
    #define PORT_BUTTON_0 PORT_BUT_1
    #define PORT_BUTTON_1 PORT_BUT_2
#else
    // 9.9.0 XN names found, add 9.9.1 XN names
    #define PORT_BUT_1 PORT_BUTTON_0
    #define PORT_BUT_2 PORT_BUTTON_1
endif
```

13 Related Documents

The following documents (available from the XMOS website) provide more information on designing with the XK-1:

- *XK-1 Development Kit Tutorial*: provides an introduction to programming software on the XK-1 using the XC language.
- *XCore XS1 Architecture Tutorial*: provides an overview of the XS1 instruction set architecture.

The most up-to-date information on the XK-1, including board schematics and product datasheets, is available from:

- `http://www.xmos.com/xk1/`

14 Document History

Date	Release	Comment
2009-12-21	1.2.2	Page 6: Pin 14 right-hand connector XLD0_up

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