# XC-1A Hardware Manual

*Version* 1.2

XMOS

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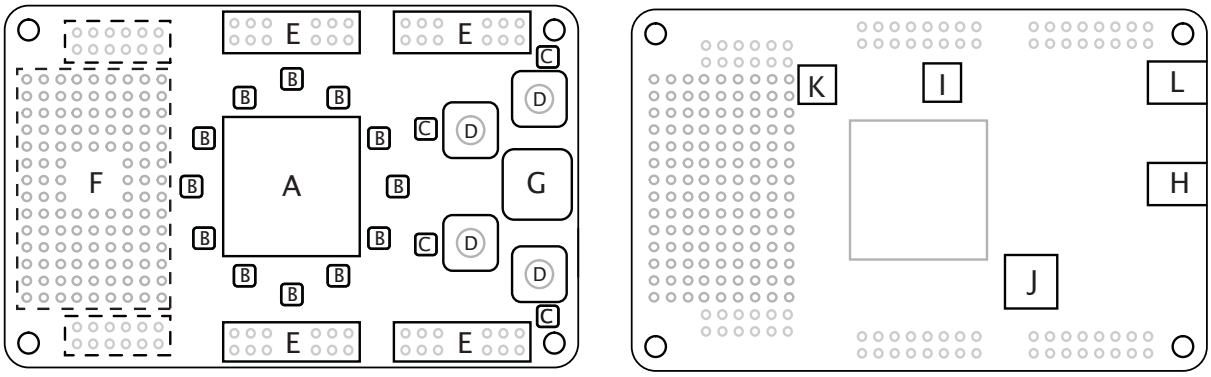
# 1 Introduction

The XC-1A is a card-sized development board based on the XMOS XS1-G4 event-driven processor device. It comprises a single XS1-G4, 16 user-configurable LEDs, four push-buttons, a speaker, JTAG and serial interfaces, four expansion areas suitable for IDC headers and a through-hole prototyping area for connecting external components.

The diagram below shows the layout of the main components on the card:




**A** XS1-G4 Device

**B** Twelve Red/Green User LEDs

**C** Four Green User LEDs

**D** Four Push-Button Switches

**E** Four I/O Expansion Areas

**F** Prototyping Area

**G** Speaker

**H** Mini USB-B Connector

**I** 20MHz Crystal Oscillator

**J** USB 2.0 to JTAG

**K** SPI FLASH

**L** External 5V Connector

The XC-1A Development Kit also includes a USB cable for powering and booting the device from a PC. The card is fitted with four plastic feet, which are useful for building bigger prototyping systems.

The following sections in this document provide a detailed description of these components.

# 2 XS1-G4 Device [A]

The XC-1A provides a single XS1-G4 device in a 512BGA package. The XS1-G4 device contains four multithreaded XCore™ processing components with tightly integrated support for communication, I/O and timing. The pins on XCore processors are brought out of the package and connected to the card's components as follows:

**Processor 0**

- Three red/green and four green LEDs
- Four push-button switches
- Speaker
- SPI FLASH memory
- Prototyping area
- One 16-way I/O expansion header (16 I/O bits)

**Processor 1, 2**

- Three red/green LEDs
- One 16-way I/O expansion header (16 I/O bits)

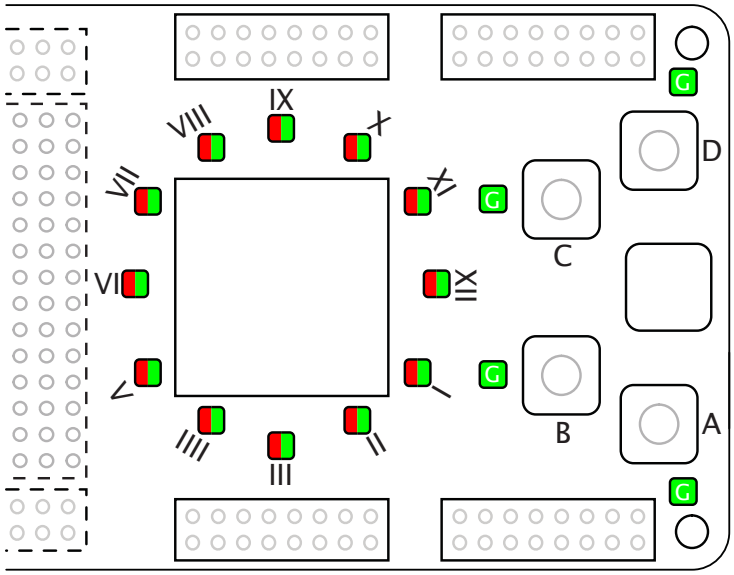
**Processor 3**

- Three red/green LEDs
- Two 16-way I/O expansion headers (16 I/O bits)

The processors have ports that are directly connected to the I/O pins. Examples of how to write software that interfaces over these ports with the XC-1A components is provided in a separate tutorial [1].

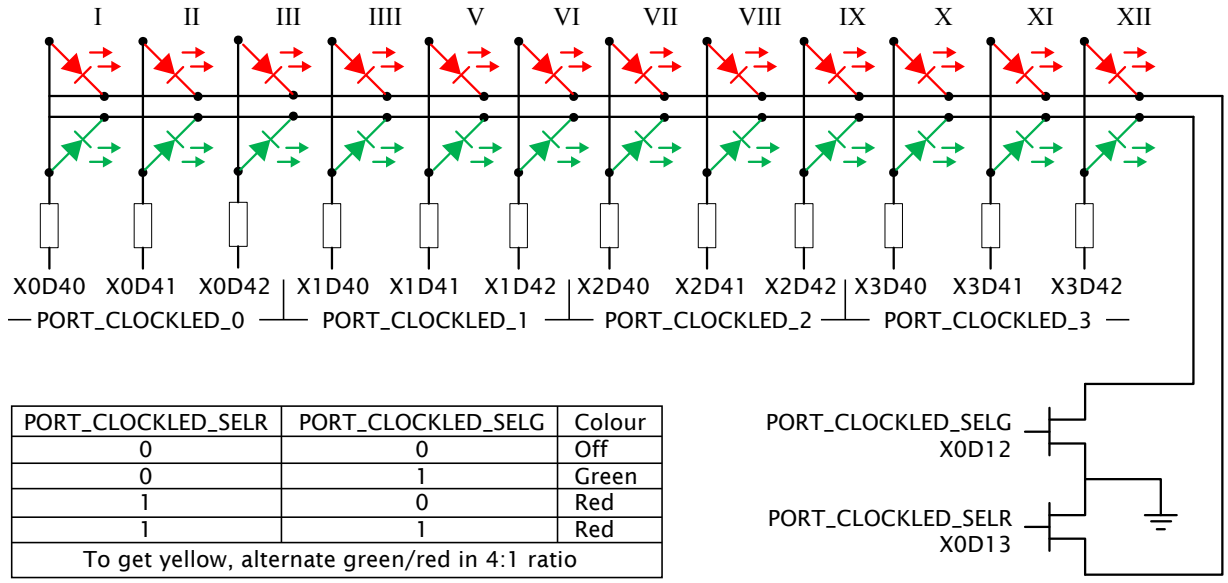
# 3 User-configurable LEDs [B and C]

The XC-1A has 16 user-configurable LEDs. Four LEDs are positioned next to the four push-buttons (collectively referred to as button-LEDs) and contain green diodes. The other 12 LEDs are positioned around the XS1-G4 in a circle (collectively referred to as clock-LEDs) and contain red/green diodes. A Roman numeral is printed next to each LED. The layout of the LEDs is shown on the following page.




To reduce the number of pins required for the 12 clock-LEDs, the LED anodes are connected to four 8-bit ports (8D) on processor 0, 1, 2 and 3 and the cathodes are connected to two 1-bit ports (1E for green, 1F for red) on processor 0.

The schematic for the clock-LEDs is shown below




| PORT_CLOCKLED_SELR | PORT_CLOCKLED_SELG | Colour |
|---|---|---|
| 0 | 0 | Off |
| 0 | 1 | Green |
| 1 | 0 | Red |
| 1 | 1 | Red |
| To get yellow, alternate green/red in 4:1 ratio | | |

The clock-LED pins are mapped to ports on the XS1-G4 as shown in the table below:

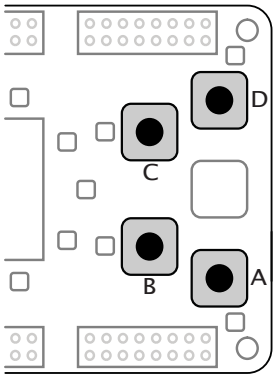
| Pin | Port | | Processor |
|---|---|---|---|
| | 1b | 8b | |
| XCore0 | | | |
| X0D40 | | P8D4 | PORT_CLOCKLED_0 [I] |
| X0D41 | | P8D5 | PORT_CLOCKLED_0 [II] |
| X0D42 | | P8D6 | PORT_CLOCKLED_0 [III] |
| X0D12 | P1E0 | | PORT_CLOCKLED_SELG |
| X0D13 | P1F0 | | PORT_CLOCKLED_SELR |
| XCore1 | | | |
| X1D40 | | P8D4 | PORT_CLOCKLED_1 [IV] |
| X1D41 | | P8D5 | PORT_CLOCKLED_1 [V] |
| X1D42 | | P8D6 | PORT_CLOCKLED_1 [VI] |
| XCore2 | | | |
| X2D40 | | P8D4 | PORT_CLOCKLED_2 [VII] |
| X2D41 | | P8D5 | PORT_CLOCKLED_2 [VIII] |
| X2D42 | | P8D6 | PORT_CLOCKLED_2 [IX] |
| XCore3 | | | |
| X3D40 | | P8D4 | PORT_CLOCKLED_3 [X] |
| X3D41 | | P8D5 | PORT_CLOCKLED_3 [XI] |
| X3D42 | | P8D6 | PORT_CLOCKLED_3 [XII] |

The button LED pins are mapped to ports on the XS1-G4 as described in the table below:

| Pin | Port | Processor |
|---|---|---|
| | 4b | 0 |
| X0D14 | P4C0 | PORT_BUTTONLED [A] |
| X0D15 | P4C1 | PORT_BUTTONLED [B] |
| X0D20 | P4C2 | PORT_BUTTONLED [C] |
| X0D21 | P4C3 | PORT_BUTTONLED [D] |

# 4 Push-Button Switches [D]

The XC-1A provides four push-button switches whose states can be sampled at any time by software. The layout of the push-buttons is shown below.



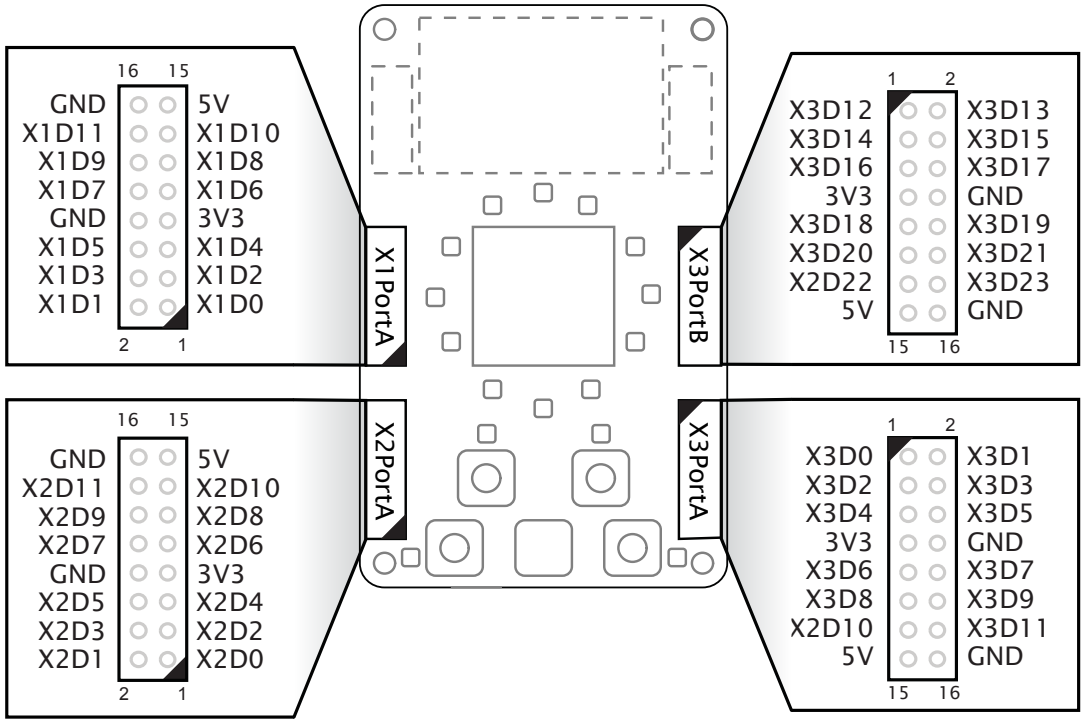

The push buttons are connected to four pins, which are mapped to ports as described in the table below.

| Pin | Port | | Processor |
|---|---|---|---|
| | 4b | 8b | 0 |
| X0D16 | P4D0 | P8B2 | PORT_BUTTON [A] |
| X0D17 | P4D1 | P8B3 | PORT_BUTTON [B] |
| X0D18 | P4D2 | P8B4 | PORT_BUTTON [C] |
| X0D19 | P4D3 | P8B5 | PORT_BUTTON [D] |

The default state of a pin is high, pushing the button drives its pin low. Each pin can be interfaced to a 4-bit port or an 8-bit port on the XS1-G4. The choice is defined by the port interface used in the software [2].

# 5 I/O Expansion Areas [E]

The I/O pins of XCore1, XCore2 and XCore3 are brought out to expansion areas on both sides of the card. These areas have 0.1" pitch plated through holes and are suitable for use with IDC headers. To provide maximum flexibility, no headers are fitted, allowing the most suitable type to be selected. The routing of the I/O and power pins in the expansion headers is shown below.




The expansion headers provide a bank of 12 I/O pins. The pins are mapped to the ports as shown in the table on the next page.

Eight pins from each bank can be configured as either two 4-bit ports or a single 8-bit port. Alternatively, two of the expansion headers can be used together as a single 16-bit port.

| Pin | Port | | | | Processor |
|---|---|---|---|---|---|
| | 1b | 4b | 8b | 16b | 1 |
| XCore1 | | | | | |
| X1D0 | P1A0 | | | | X1PortA |
| X1D1 | P1B0 | | | | |
| X1D2 | | P4A0 | P8A0 | P16A0 | |
| X1D3 | | P4A1 | P8A1 | P16A1 | |
| X1D4 | | P4B0 | P8A2 | P16A2 | |
| X1D5 | | P4B1 | P8A3 | P16A3 | |
| X1D6 | | P4B2 | P8A4 | P16A4 | |
| X1D7 | | P4B3 | P8A5 | P16A5 | |
| X1D8 | | P4A2 | P8A6 | P16A6 | |
| X1D9 | | P4A3 | P8A7 | P16A7 | |
| X1D10 | P1C0 | | | | |
| X1D11 | P1D0 | | | | |
| XCore2 | | | | | |
| X2D0 | P1A0 | | | | X2PortA |
| X2D1 | P1B0 | | | | |
| X2D2 | | P4A0 | P8A0 | P16A0 | |
| X2D3 | | P4A1 | P8A1 | P16A1 | |
| X2D4 | | P4B0 | P8A2 | P16A2 | |
| X2D5 | | P4B1 | P8A3 | P16A3 | |
| X2D6 | | P4B2 | P8A4 | P16A4 | |
| X2D7 | | P4B3 | P8A5 | P16A5 | |
| X2D8 | | P4A2 | P8A6 | P16A6 | |
| X2D9 | | P4A3 | P8A7 | P16A7 | |
| X2D10 | P1C0 | | | | |
| X2D11 | P1D0 | | | | |
| XCore3 | | | | | |
| X3D0 | P1A0 | | | | X3PortA |
| X3D1 | P1B0 | | | | |
| X3D2 | | P4A0 | P8A0 | P16A0 | |
| X3D3 | | P4A1 | P8A1 | P16A1 | |
| X3D4 | | P4B0 | P8A2 | P16A2 | |
| X3D5 | | P4B1 | P8A3 | P16A3 | |
| X3D6 | | P4B2 | P8A4 | P16A4 | |
| X3D7 | | P4B3 | P8A5 | P16A5 | |
| X3D8 | | P4A2 | P8A6 | P16A6 | |
| X3D9 | | P4A3 | P8A7 | P16A7 | |
| X3D10 | P1C0 | | | | |
| X3D11 | P1D0 | | | | |
| X3D12 | P1E0 | | | | X3PortB |
| X3D13 | P1F0 | | | | |
| X3D14 | | P4C0 | P8B0 | P16A8 | |
| X3D15 | | P4C1 | P8B1 | P16A9 | |
| X3D16 | | P4D0 | P8B2 | P16A10 | |
| X3D17 | | P4D1 | P8B3 | P16A11 | |
| X3D18 | | P4D2 | P8B4 | P16A12 | |
| X3D19 | | P4D3 | P8B5 | P16A13 | |
| X3D20 | | P4C2 | P8B6 | P16A14 | |
| X3D21 | | P4C3 | P8B7 | P16A15 | |
| X3D22 | P1G0 | | | | |
| X3D23 | P1H0 | | | | |

## 5.1 XMOS Link Configuration

Some of the I/O pins on the expansion header can be configured as XMOS Links. The mapping of XMOS Links to the headers is shown in the table below.

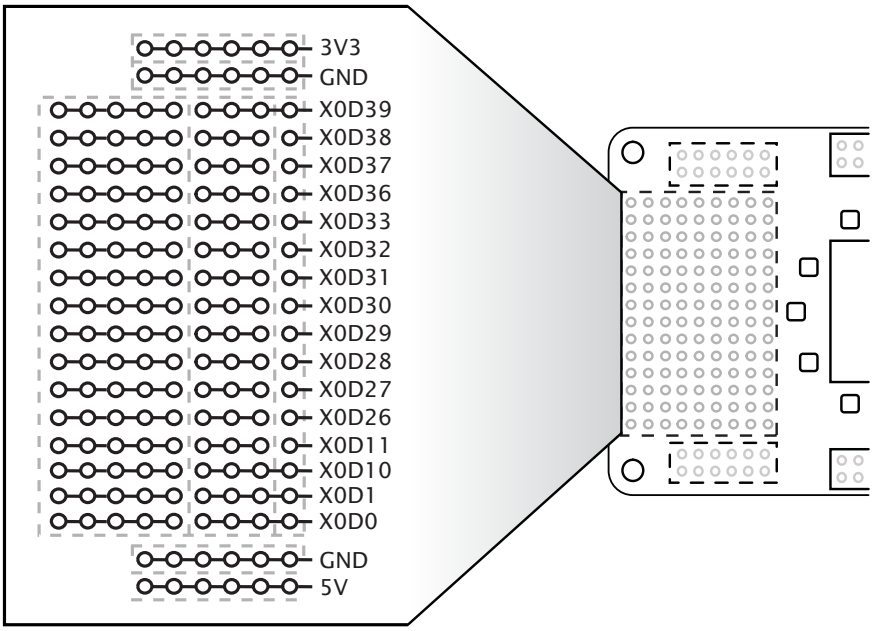
| Pin | Processor 1 | | Processor 2 | | Processor 3 | |
|---|---|---|---|---|---|---|
| | Header A | | Header A | | Header A | |
| | 2 bit | 5 bit | 2 bit | 5 bit | 2 bit | 5 bit |
| XnD1 | | XLA4 I | | XLA4 O | | XLA4 I |
| XnD2 | | XLA3 I | | XLA3 O | | XLA3 I |
| XnD3 | | XLA2 I | | XLA2 O | | XLA2 I |
| XnD4 | XLA1 I | XLA1 I | XLA1 I | XLA1 O | XLA1 I | XLA1 I |
| XnD5 | XLA0 I | XLA0 I | XLA0 I | XLA0 O | XLA0 I | XLA0 I |
| XnD6 | XLA0 O | XLA0 O | XLA0 O | XLA0 I | XLA0 O | XLA0 O |
| XnD7 | XLA1 O | XLA1 O | XLA1 O | XLA1 I | XLA1 O | XLA1 O |
| XnD8 | | XLA2 O | | XLA2 I | | XLA2 O |
| XnD9 | | XLA3 O | | XLA3 I | | XLA3 O |
| XnD10 | | XLA4 O | | XLA4 I | | XLA4 O |

| | | Header B | |
|---|---|---|---|
| XnD13 | | | XLB4 I |
| XnD14 | | | XLB3 I |
| XnD15 | | | XLB2 I |
| XnD16 | | XLB1 I | XLB1 I |
| XnD17 | | XLB0 I | XLB0 I |
| XnD18 | | XLB0 O | XLB0 O |
| XnD19 | | XLB1 O | XLB1 O |
| XnD20 | | | XLB2 O |
| XnD21 | | | XLB3 O |
| XnD22 | | | XLB4 O |

# 6 Prototyping Area [F]

The XC-1A provides a 0.1” pitch plated through hole area for adding components to the card.

The routing of I/O and power pins in the prototyping area is shown below.

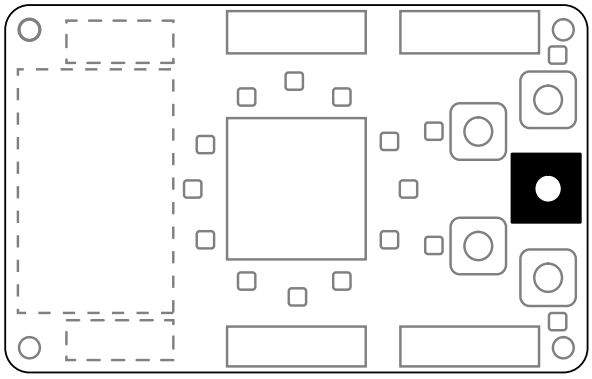



The prototyping area provides a bank of 16 I/O pins, which are mapped to the ports on processor 0 as described in the table below.

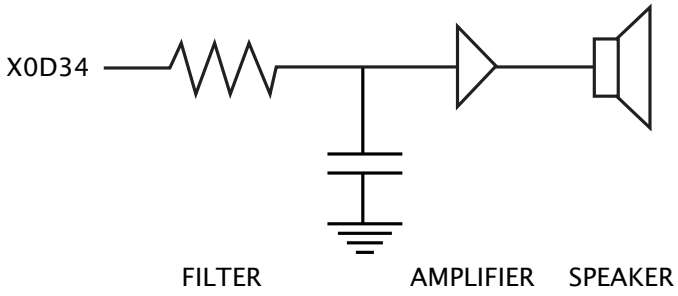
| Pin | Port | | | Processor |
|---|---|---|---|---|
| | 1b | 4b | 8b | 0 |
| X0D26 | | P4E0 | P8C0 | Prototyping Area |
| X0D27 | | P4E1 | P8C1 | |
| X0D28 | | P4F0 | P8C2 | |
| X0D29 | | P4F1 | P8C3 | |
| X0D30 | | P4F2 | P8C4 | |
| X0D31 | | P4F3 | P8C5 | |
| X0D32 | | P4E2 | P8C6 | |
| X0D33 | | P4E3 | P8C7 | |
| X0D36 | P1M0 | | | |
| X0D37 | P1N0 | | | |
| X0D38 | P1O0 | | | |
| X0D39 | P1P0 | | | |

# 7 Speaker [G]

The XC-1A has a speaker. The layout of the speaker is shown below.



Audio signals are generated by filtering pulse width modulated (PWM) digital signals to form an analogue waveform, which is amplified and sent to the speaker, as shown below:



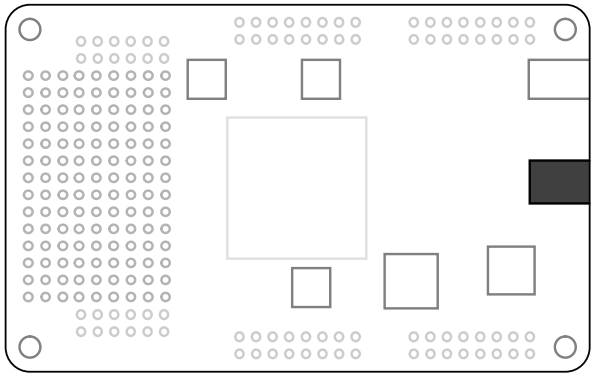

The speaker pin is mapped to a port on processor 0, as shown in the table below.

| Pin | Port | Processor |
|---|---|---|
| | 1b | 0 |
| X0D34 | P1K0 | PORT_SPEAKER |

# 8 USB Connector [H and J]

The XC-1A can be powered directly from a host PC using a USB connector. The 5V voltage is converted by the on-board regulator to the 1V and 3V3 supplies used by the components.

The USB connector can also be used to load and debug code on all of the XS1-G4's processors. The USB connector provides JTAG control, system reset, processor debug, and two UART links. The layout of the USB connector is shown below.



On power on, the XS1-G4 boots from the on-board flash memory. The XS1-G4 can then be put into JTAG mode by the PC, which then boots another program.

No UART hardware is provided. Instead, two UART pins are mapped to ports, as shown in the table below.

| Pin | Port | Processor |
|---|---|---|
| | 1b | 0 |
| X0D23 | P1H0 | PORT_UART_TX |
| X0D24 | P1I0 | PORT_UART_RX |

If a UART is required, it can be implemented in software by sampling and driving these ports at the required rate. The connector performs a UART-to-USB conversion on these pins, presenting a virtual COM port to the PC that can be interfaced via a terminal emulator.

# 9 20MHz Crystal Oscillator [I]

The XS1-G4 is clocked at 20MHz by a crystal oscillator on the card. Each processor is clocked at 400MHz, the I/O ports at 100MHz, by an on-chip phase-locked loop (PLL).

# 10 SPI FLASH Memory [J]

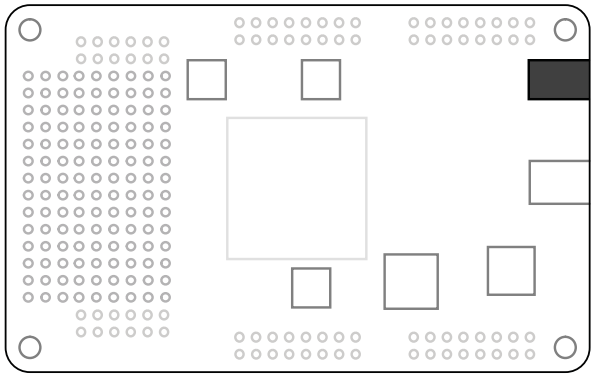
The XC-1A provides 4Mbit of Serial Peripheral Interface (SPI) FLASH memory, which is interfaced by the four 1-bit connections described in the table on page 16.

| Pin | Port | Processor |
|---|---|---|
| | 1b | 0 |
| X0D0 | P1A0 | PORT_SPI_MISO |
| X0D1 | P1B0 | PORT_SPI_SS |
| X0D10 | P1C0 | PORT_SPI_CLK |
| X0D11 | P1D0 | PORT_SPI_MOSI |

The Tools include the XFLASH utility for programming compiled programs into the flash memory. XC-1A designs may also access the flash memory at run-time by interfacing with the above ports.

# 11 Power Connector [L]

The XC-1A includes an external 5V power supply connector. The voltage is converted by the on-board regulator to the 1V and 3V3 supplies used by the components. The layout of the connector is shown below.

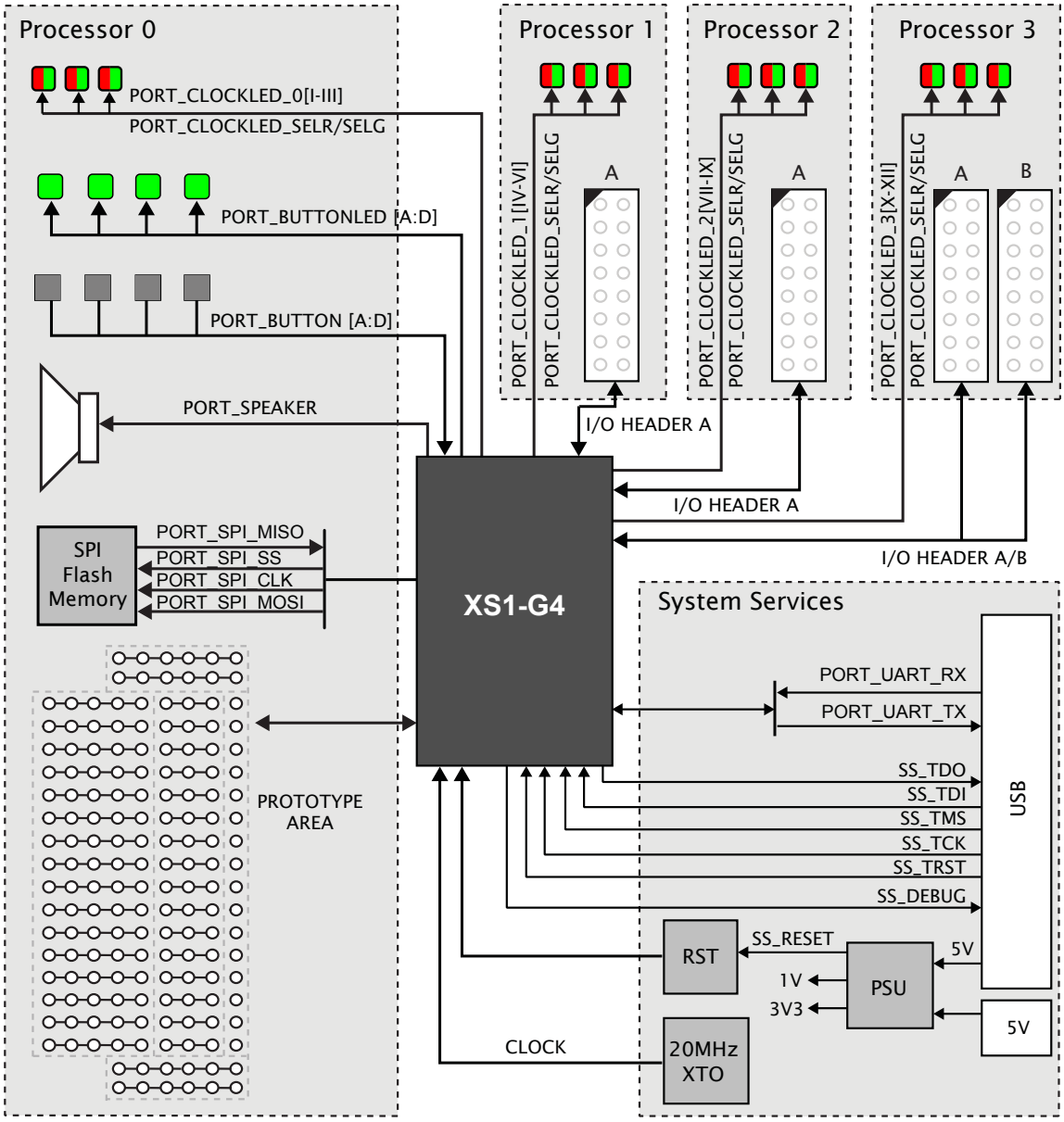


# 12 Dimensions

The XC-1A dimensions are 86 x 54mm. The mounting holes are 3mm in diameter.

# 13 XC-1A Block Diagram

The diagram below shows how the XC-1A components are connected to the XS1-G4.




## 13.1 I/O Port-to-Pin Mapping

The table on the next page provides a full description of the port-to-pin mappings described throughout this document.

| Pin | Port | | | | Processor | | | |
|---|---|---|---|---|---|---|---|---|
| | 1b | 4b | 8b | 16b | 0 | 1 | 2 | 3 |
| X*n*D0 | P1A0 | | | | PORT_SPI_MISO | X1PortA Header | X2PortA Header | X3PortA Header |
| X*n*D1 | P1B0 | | | | PORT_SPI_SS | | | |
| X*n*D2 | | P4A0 | P8A0 | P16A0 | | | | |
| X*n*D3 | | P4A1 | P8A1 | P16A1 | | | | |
| X*n*D4 | | P4B0 | P8A2 | P16A2 | | | | |
| X*n*D5 | | P4B1 | P8A3 | P16A3 | | | | |
| X*n*D6 | | P4B2 | P8A4 | P16A4 | | | | |
| X*n*D7 | | P4B3 | P8A5 | P16A5 | | | | |
| X*n*D8 | | P4A2 | P8A6 | P16A6 | | | | |
| X*n*D9 | | P4A3 | P8A7 | P16A7 | | | | |
| X*n*D10 | P1C0 | | | | SPI_CLK | | | |
| X*n*D11 | P1D0 | | | | SPI_MOSI | | | |
| X*n*D12 | P1E0 | | | | CLOCKLED_SELG | | | X3PortB Header |
| X*n*D13 | P1F0 | | | | CLOCKLED_SELR | | | |
| X*n*D14 | | P4C0 | P8B0 | P16A8 | BUTTONLED [A] | | | |
| X*n*D15 | | P4C1 | P8B1 | P16A9 | BUTTONLED [B] | | | |
| X*n*D16 | | P4D0 | P8B2 | P16A10 | BUTTON [A] | | | |
| X*n*D17 | | P4D1 | P8B3 | P16A11 | BUTTON [B] | | | |
| X*n*D18 | | P4D2 | P8B4 | P16A12 | BUTTON [C] | | | |
| X*n*D19 | | P4D3 | P8B5 | P16A13 | BUTTON [D] | | | |
| X*n*D20 | | P4C2 | P8B6 | P16A14 | BUTTONLED [C] | | | |
| X*n*D21 | | P4C3 | P8B7 | P16A15 | BUTTONLED [D] | | | |
| X*n*D22 | P1G0 | | | | TESTPOINT | | | |
| X*n*D23 | P1H0 | | | | UART_TX | | | |
| X*n*D24 | P1I0 | | | | UART_RX | | | |
| X*n*D25 | P1J0 | | | | TESTPOINT | | | |
| X*n*D26 | | P4E0 | P8C0 | P16B0 | PROTO_AREA_4 | | | |
| X*n*D27 | | P4E1 | P8C1 | P16B1 | PROTO_AREA_5 | | | |
| X*n*D28 | | P4F0 | P8C2 | P16B2 | PROTO_AREA_6 | | | |
| X*n*D29 | | P4F1 | P8C3 | P16B3 | PROTO_AREA_7 | | | |
| X*n*D30 | | P4F2 | P8C4 | P16B4 | PROTO_AREA_8 | | | |
| X*n*D31 | | P4F3 | P8C5 | P16B5 | PROTO_AREA_9 | | | |
| X*n*D32 | | P4E2 | P8C6 | P16B6 | PROTO_AREA_10 | | | |
| X*n*D33 | | P4E3 | P8C7 | P16B7 | PROTO_AREA_11 | | | |
| X*n*D34 | P1K0 | | | | SPEAKER | | | |
| X*n*D35 | P1L0 | | | | TESTPOINT | | | |
| X*n*D36 | P1M0 | | P8D0 | P16B8 | PROTO_AREA_12 | | | |
| X*n*D37 | P1N0 | | P8D1 | P16B9 | PROTO_AREA_13 | | | |
| X*n*D38 | P1O0 | | P8D2 | P16B10 | PROTO_AREA_14 | | | |
| X*n*D39 | P1P0 | | P8D3 | P16B11 | PROTO_AREA_15 | | | |
| X*n*D40 | | | P8D4 | P16B12 | CLOCKLED_0 [I] | CLOCKLED_1 [IV] | CLOCKLED_2 [VII] | CLOCKLED_3 [X] |
| X*n*D41 | | | P8D5 | P16B13 | CLOCKLED_0 [II] | CLOCKLED_1 [V] | CLOCKLED_2 [VIII] | CLOCKLED_3 [XI] |
| X*n*D42 | | | P8D6 | P16B14 | CLOCKLED_0 [III] | CLOCKLED_1 [VI] | CLOCKLED_2 [IX] | CLOCKLED_3 [XII] |
| X*n*D43 | | | P8D7 | P16B15 | | | | |

# 14 XC-1A XN File

The XCore ports linked to the hardware features on the XC-1A are mapped to generic port identifiers as part of a platform specific XN file, which simplifies the process of porting a project between platforms.

The following table lists the defined identifiers for all processors:

| Processor | Port Location | Generic Identifier |
|---|---|---|
| 0 | XS1_PORT_1A | PORT_SPI_MISO |
| | XS1_PORT_1B | PORT_SPI_SS |
| | XS1_PORT_1C | PORT_SPI_CLK |
| | XS1_PORT_1D | PORT_SPI_MOSI |
| | XS1_PORT_1E | PORT_CLOCKLED_SELG |
| | XS1_PORT_1F | PORT_CLOCKLED_SELR |
| | XS1_PORT_1H | PORT_UART_TX |
| | XS1_PORT_1I | PORT_UART_RX |
| | XS1_PORT_1K | PORT_SPEAKER |
| | XS1_PORT_4C | PORT_BUTTONLED |
| | XS1_PORT_4D | PORT_BUTTON |
| | XS1_PORT_8D | PORT_CLOCKLED_0 |
| 1 | XS1_PORT_8D | PORT_CLOCKLED_1 |
| 2 | XS1_PORT_8D | PORT_CLOCKLED_2 |
| 3 | XS1_PORT_8D | PORT_CLOCKLED_3 |

# 15 Related Documents

The following documents provide more information on designing with the XC-1A:

- *XCard-1A Tutorial* [1]: provides an introduction to programming software on the XC-1A using the XC language.
- *The XMOS XS1 Architecture* [3]: provides an overview of the XS1 instruction set architecture.

The most up-to-date information on the XC-1A, including board schematics and product datasheets, is available from:

- **http://www.xmos.com/xc1a**

# 16 Document History

| Date | Release | Comment |
|---|---|---|
| 2010-01-08 | 1.1 | Section 13: Arrows to SPI wrong direction<br>Added document history. |
| 2010-04-27 | 1.2 | Section 13.1: CLOCKLEDs linked to P8D4/5/6 |

## Bibliography

[1] XC-1A Development Kit Tutorial. Website, 2009. http://www.xmos.com/published/xc1atut.

[2] Douglas Watt. *Programming XC on XMOS Devices*. XMOS Limited, Sep 2009. http://www.xmos.com/published/xc_en.

[3] David May. *The XMOS XS1 Architecture*. XMOS Limited, 2009. http://www.xmos.com/published/xs1_en.

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