P2020DS

Integrated media and communications processor development system

Overview

The P2020/P2010 Development System (P2020DS) is ideal for hardware and software development for embedded applications. It leverages Freescale's highly integrated QorIQ™ P2020 processor and leading-edge external components.

The high level of integration in the P2020E processor helps to lower system costs, improve performance and simplify board design. The P2020E processor supports:

Dual e500 cores, built on Power Architecture® technology

- 800–1200 MHz
- 512 KB frontside L2 cache w/ECC, hardware cache coherent
- 36-bit physical addressing, DP-FPU

System Unit

- 64-/32-bit DDR2/DDR3 with ECC
- Integrated SEC 3.1 Security Engine
- Open-PIC Interrupt controller, performance monitor, 2x I²C, timers, 16 GPIOs, DUART
- 16-bit enhanced local bus supports booting from NAND flash memory
- One USB 2.0 host controller with ULPI interface
- SPI controller supports booting from SPI serial flash memory
- SD/MMC card controller supports booting from flash cards
- Three 10/100/1000 Ethernet controllers (eTSEC) w/ Jumbo Frame support, SGMII interface
- Enhanced features: Parser/filer, QOS, IP-checksum offload, lossless flow control
- IEEE® 1588 v2 support
- Two Serial RapidIO® controllers with integrated message unit operating up to 3.125 GHz
- Three PCI Express® 1.0a controllers

The P2010E is a single-core version of the P2020E. The P2020E processor also integrates an optional hardware encryption block that supports different algorithms for high-performance data that is critical for supporting secure communications. Devices marked with an E include this security engine.

A board support package (BSP) is pre-installed on the P2020DS. This BSP consists of a boot loader (u-boot) and a generic Power Architecture technology system based on the Linux® kernel. The u-boot binary and the Linux kernel reside in the on-board flash memory with a file system pre-installed on the hard disk shipped in the P2020DS development system.

The P2020DS BSP generation takes advantage of the Linux Target Image Builder (LTIB), a suite of tools that leverages existing open source configuration scripts and source code packages, packing them all into a single BSP generation bundle. The source code packages include boot loader and Linux kernel sources as well as many user-space source code packages to build a complete BSP. The LTIB also provides compiler packages, required to build the BSP. Freescale developers use the LTIB to create BSPs for a multitude of Freescale development markets. The LTIB leverages as many BSP elements as possible for the Freescale markets supported, while offering the flexibility necessary to customize components that require platform-specific modifications.

Many third-party applications are available for the P2020DS. They are typically built on top of the BSP delivered by Freescale and can be installed on the hard disk. To see demonstrations or to acquire details of Freescale's third-party applications for this platform, please contact your local Freescale sales office.

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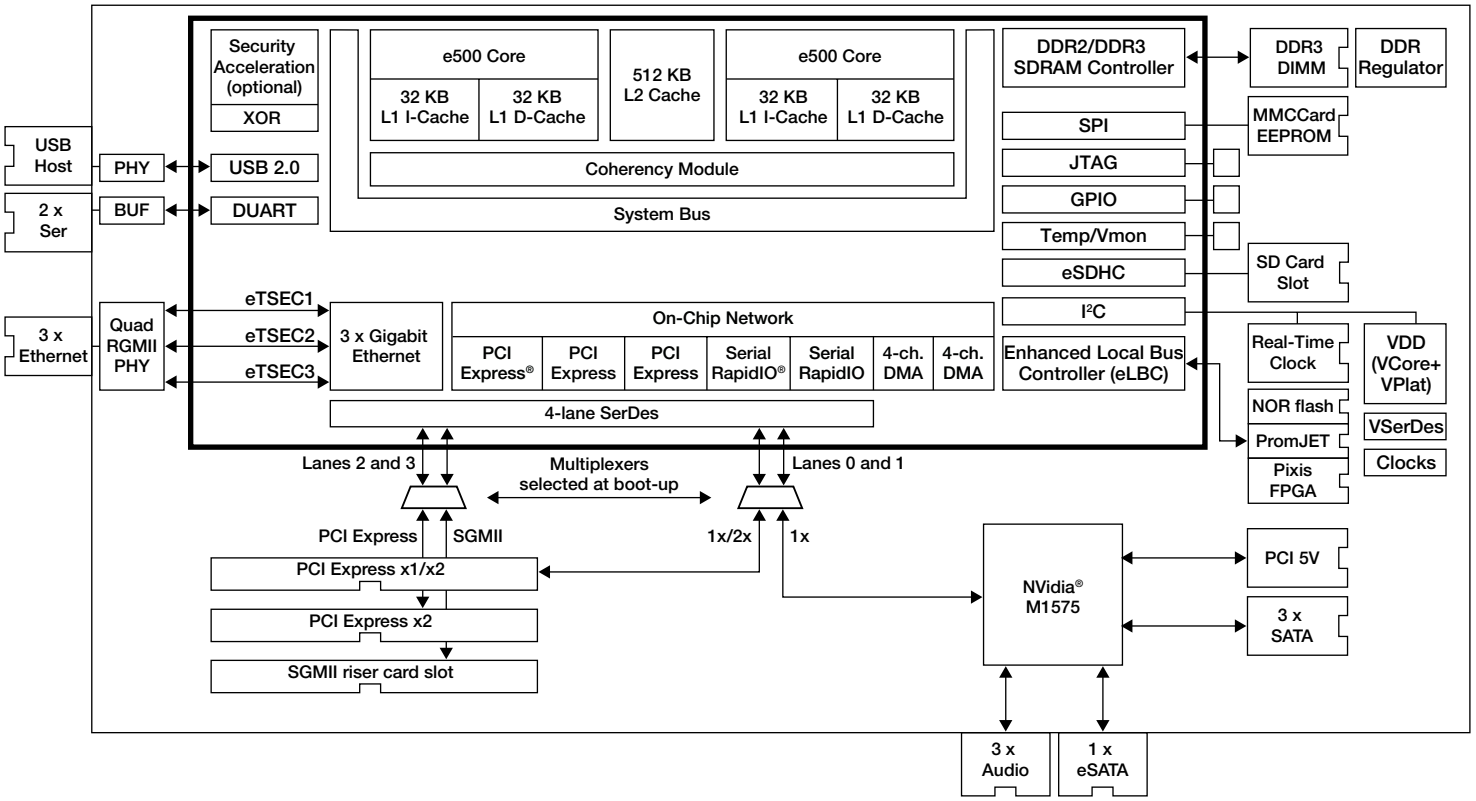
P2020DS Block Diagram



P2020E Development System

- P2020E QorIQ™ multicore communications processor, built on Power Architecture technology
- Memory
  - 2 GB DDR3 DIMM
  - 128 MB NOR flash memory
  - 16 MB SPI ROM
  - 256B NVRAM
- PCI Express: dual x2 slot
- Ethernet
  - eTSEC1: RGMII
  - eTSEC2: RGMII or SGMII
  - eTSEC3: RGMII or SGMII
- IEEE® 1588
  - Clock input from precision oscillator
  - Accessible via test header
- Dual I²C
- SD/MMC card slot
- USB Type A connector
- UARTs: Two DB9 connectors
- SATA2
- GPIO: 16
- Three 10/100/1000 Ethernet connectors
- SGMII riser card slot
- System logic (Pixis FPGA)
  - Manages system reset sequencing
  - Manages system bus and PCI clock speed selections
  - Implements registers for system control and monitoring
- System clock
  - SYSCLK switch can be set to one of eight common settings in the interval 33 MHz–166 MHz
- DDR clock
  - DDRCLK switch can be set to one of eight common settings in the interval 33 MHz–166 MHz
- Power supplies
  - Combined regulator for VDD and VDD_PLAT (nominally 1.05V)
- Documentation
  - Reference manual
  - Schematics
  - Bill of materials
  - Board errata
  - Configuration guide
- Software tools
  - Linux 2.6.x kernel
  - Cross compile and native GNU tool chain
  - CodeWarrior™ USB TAP

Learn More: For current information about Freescale products and documentation, please visit **www.freescale.com/QorIQ**.

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