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User's Manual

Renesas Starter Kit for H8S/2215R

User's Manual

RENESAS SINGLE-CHIP MICROCOMPUTER
H8S FAMILY

Renesas Electronics
www.renesas.com

Rev.1.00 2008.01

Table of Contents

Chapter 1. Preface

Cautions

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Glossary

ADC	Analog to Digital Converter	USB	Universal Serial Bus
CPU	Central Processing Unit	DAC	Digital to Analog Converter
DMA	Direct Memory Access	E10A	E10A for Starter Kits debug module
FDT	Flash Development Tool	RSK	Renesas Starter Kit
LED	Light Emitting Diode	LCD	Liquid Crystal Display

Chapter 2. Purpose

This RSK is an evaluation tool for Renesas microcontrollers.

Features include:

- Renesas Microcontroller Programming.
- User Code Debugging.
- User Circuitry such as switches, LEDs and potentiometer(s).
- Sample Application.
- Sample peripheral device initialisation code.

The CPU board contains all the circuitry required for microcontroller operation.

This manual describes the technical details of the RSK hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

Chapter 3. Power Supply

3.1. Requirements

This CPU board operates from a 5V power supply.

A diode provides reverse polarity protection only if a current limiting power supply is used.

The CPU board is supplied with an E10A debugger. This product is NOT able to power the CPU board.

When the CPU board is connected to another system, that system should supply power to the CPU board.

All CPU boards have a centre positive supply connector using a 2.0mm barrel power jack and are supplied with a suitable universal power supply. The user should select the correct mains connector for their country of use.

Warning

The CPU board is neither under not over voltage protected. Always use a centre positive supply for this board.

3.2. Power – Up Behaviour

When the RSK is purchased the CPU board has the ‘Release’ or stand alone code from the example tutorial code pre-programmed into the Renesas microcontroller. On powering up the board the user LEDs will start to flash. Pressing switch 2 will cause the LEDs to flash at a rate controlled by the potentiometer.

Chapter 4. Board Layout

4.1. Component Layout

The following diagram shows top layer component layout of the board.

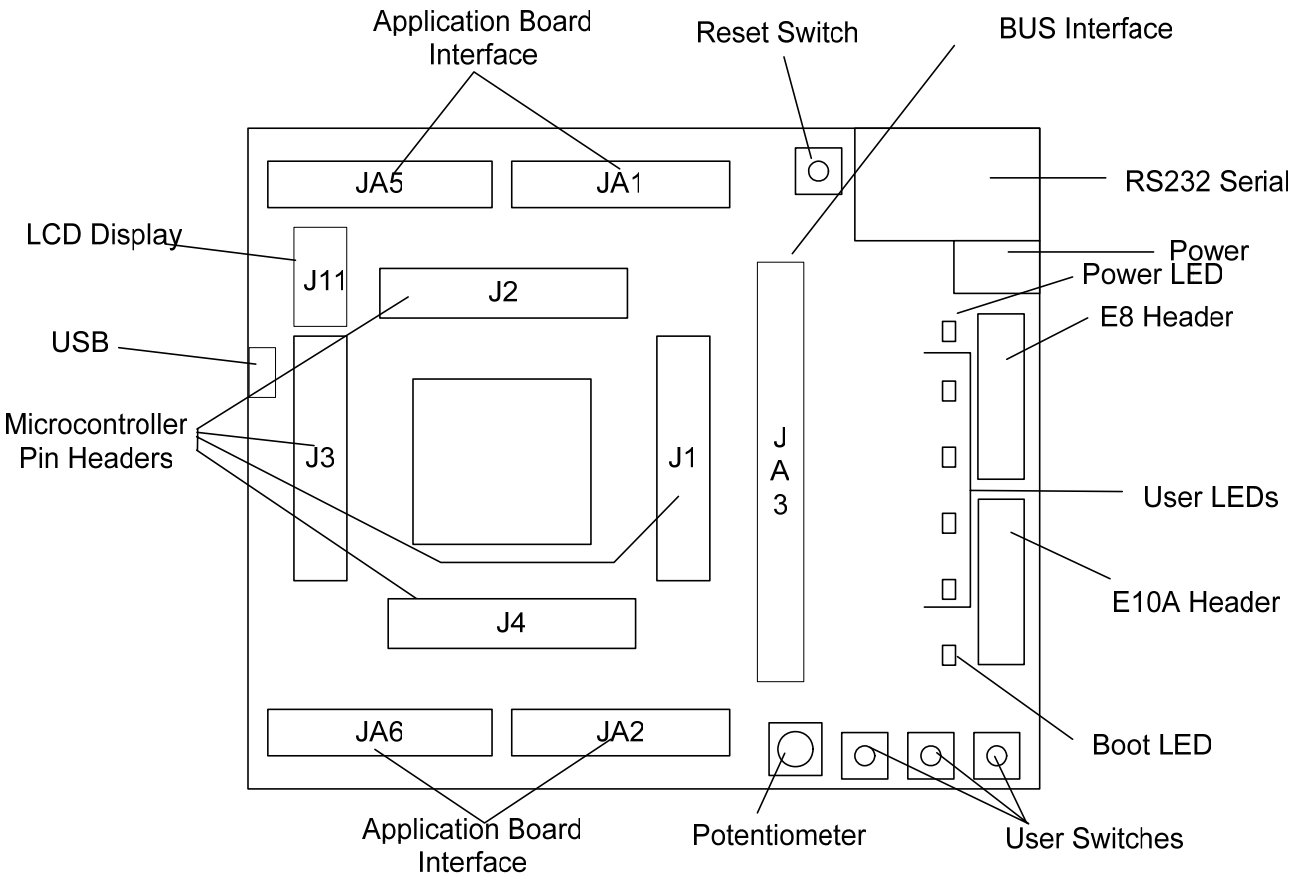

Figure 4.1: Board Layout

4.2. Board Dimensions

The following diagram gives the board dimensions and connector positions. All through hole connectors are on a common 0.1" grid for easy interfacing.

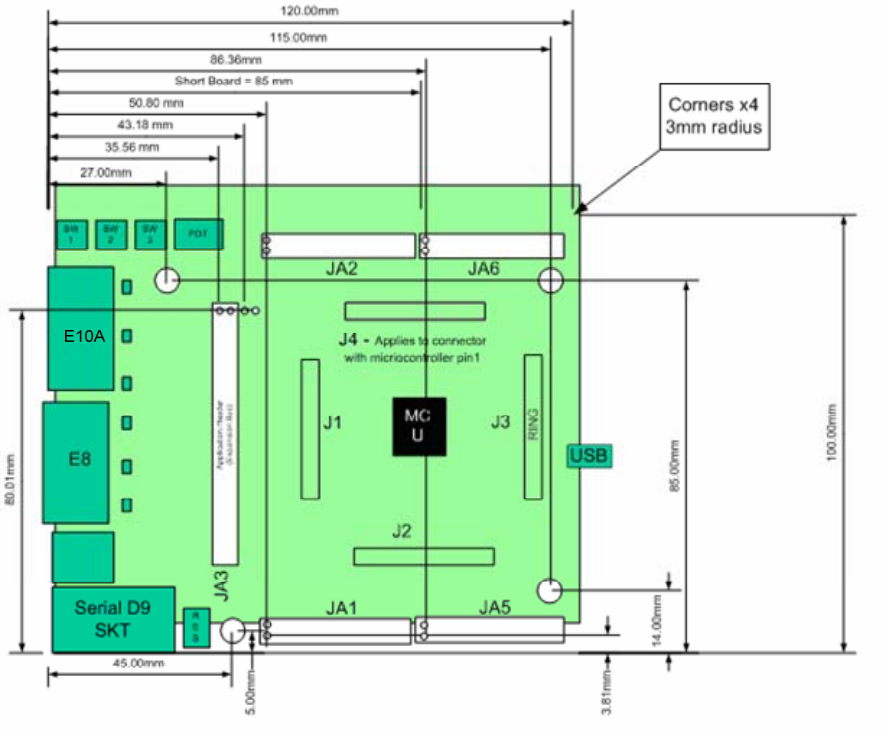

Figure 4.2 : Board Dimensions

Chapter 5. Block Diagram

Figure 5.1 shows the CPU board components and their connectivity.

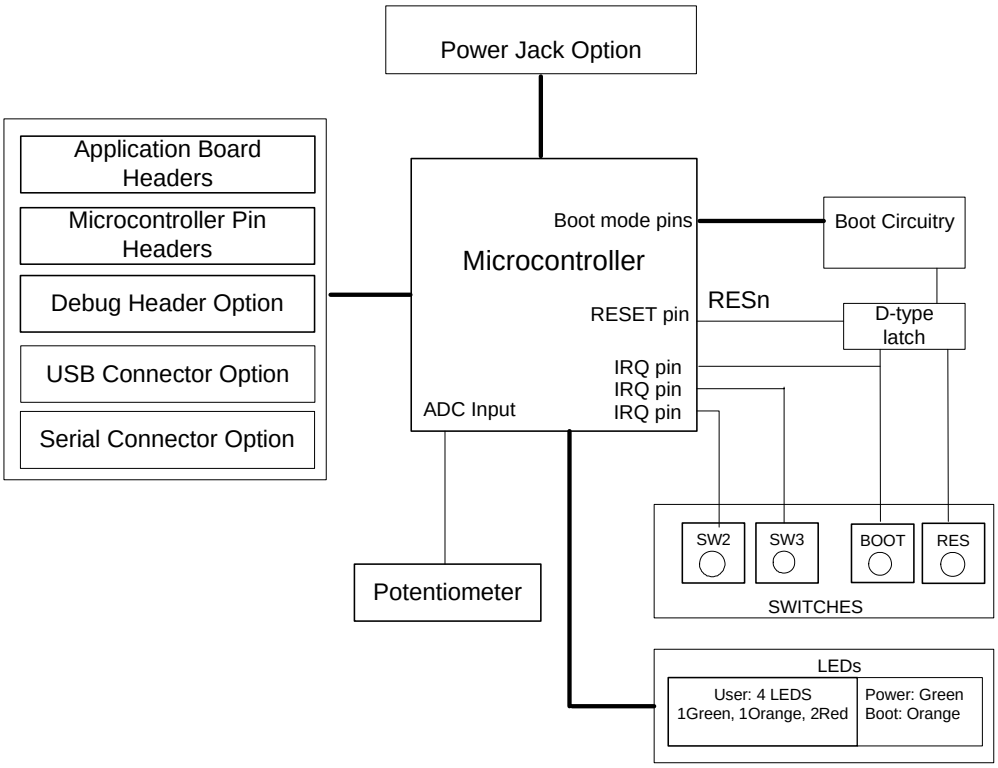

Figure 5.1: Block Diagram

Figure 5.2 shows the connections to the RSK.

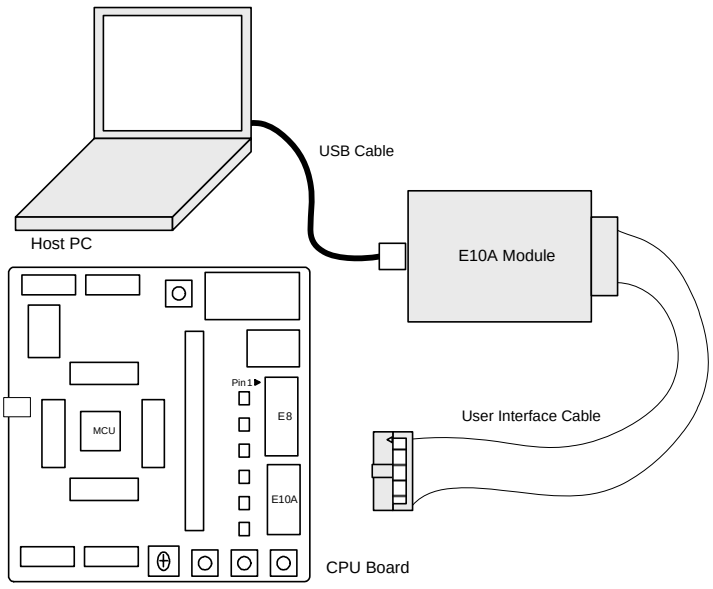

Figure 5.2 : RSK Connctions

Chapter 6. User Circuitry

6.1. Switches

There are four switches located on the CPU board. The function of each switch and its connection are shown in Table 6-1.

Switch	Function	Microcontroller
RES	When pressed; the CPU board microcontroller is reset.	RESn
SW1/BOOT*	Connects to an IRQ input for user controls.	IRQ0n, Pin 39 (Port 1, pin 4)
SW2*	Connects to an IRQ line for user controls.	IRQ2n , Pin 87 (Port F, pin 0)
SW3*	Connects to the ADC trigger/ IRQ3 input via option 0R link R105.	IRQ3n, Pin 83 (Port F, pin 3)

Table 6-1: Switch Functions

*Refer to schematic for detailed connectivity information.

6.2. LEDs

There are six LEDs on the CPU board. The green 'POWER' LED lights when the board is powered. The orange BOOT LED indicates the device is in BOOT mode when lit. The four user LEDs are connected to an IO port and will light when their corresponding port pin is set low.

Table 6-2, below, shows the LED pin references and their corresponding microcontroller port pin connections.

LED Reference (As shown on silkscreen)	Microcontroller Port Pin function	Microcontroller Pin Number	Polarity
LED0	Port F1	86	Active Low
LED1	Port F2	85	Active Low
LED2*	Port A0	30 via R133	Active Low
LED3	Port G0	101	Active Low

Table 6-2: LED Port

*Refer to schematic for detailed connectivity information.

6.3. Potentiometer

A single turn potentiometer is connected to AN0 of the microcontroller via R42. This may be used to vary the input analog voltage value to this pin between AVCC and Ground.

6.4. Serial port

The microcontroller programming serial port (SCI2) is connected to the 'E8' connector by default. SCI0 is connected to the 9-way D-type connector labelled J8 via a RS232 transceiver.

Programming via	SCI 2	SCI 0	Fit	Remove
E8a	E8a	RS232	R6, R7, R28, R29	R37, R38
Serial	RS232	Disconnected	R37, R38	R6, R7, R28, R29

Table 6-3 - Serial Option Links

The board is designed to accept a straight through RS232 cable. A secondary microcontroller serial port is available and connected to the application headers. Please refer to the schematic diagram for more details on the available connections.

6.5. LCD Module

A LCD module can be fitted to the LCD connector. Any module that conforms to the pin connections and has a KS0066u compatible controller can be used with the tutorial code. The LCD module uses a 4bit interface to reduce the pin allocation. No contrast control is provided; this must be set on the display module.

Table 6-4 shows the pin allocation and signal names used on this connector.

The module supplied with the CPU board only supports 5V operation.

LCD					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	Ground	-	2	5V Only	-
3	No Connection	-	4	D0_DLCDRS	111
5	R/W (Wired to Write only)	-	6	D1_DLCDE	113
7	No Connection	-	8	No connection	-
9	No Connection	-	10	No connection	-
11	D4_DLCDD4	117	12	D5_DLCDD5	118
13	D6_DLCDD6	119	14	D7_DLCDD7	120

Table 6-4 LCD Module Connections

6.6. Option Links

Table 6-5 below describes the function of the option links associated with serial configuration. The default configuration is indicated by BOLD text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R6	Serial Port Configuration	**Connects programming port (Rx) to E8 connector.**	Disconnects programming port (Rx) from E8 connector.	R7, R37, R38
R7	Serial Port Configuration	**Connects programming port (Tx) to E8 connector.**	Disconnects programming port (Tx) from E8 connector.	R6, R37, R38
R19	RS232 Serial	Disables RS232 Serial Transceiver	**Enables RS232 Serial Transceiver**	
R28	Serial Port Configuration	**Connects serial port RXD0 to SERIAL D-type connector.**	Disconnects serial port RXD0 from SERIAL D-type connector.	R29
R29	Serial Port Configuration	**Connects serial port TXD0 to SERIAL D-type connector.**	Disconnects serial port TXD0 from SERIAL D-type connector.	R28
R30	Serial Port Configuration	Routes RS232 serial port Rx to application connector (JA6)	**Disconnects RS232 serial port Rx from application connector (JA6)**	R31
R31	Serial Port Configuration	Routes RS232 serial port Tx to application connector (JA6)	**Disconnects RS232 serial port Tx from application connector (JA6)**	R30
R32	Serial Port Configuration	Connects serial port 1(Tx) to SERIAL D-type (J8).	**Disconnects serial port 1 (Tx) from SERIAL D-type.**	R16, R26, R33
R33	Serial Port Configuration	Connects serial port 1 (Rx) to D-type (J8).	**Disconnects serial port 1 (Rx) from SERIAL D-type.**	R16, R26, R32
R37	Serial Port Configuration	Connects programming port (Rx) to external connectors (not E8).	**Disconnects programming port (Rx) to external connectors (not E8).**	R6, R7, R38
R38	Serial Port Configuration	Connects programming port (Tx) to external connectors (not E8).	**Disconnects programming port (Tx) to external connectors (not E8).**	R6, R7, R37

Table 6-5: Serial configuration links

Table 6-6 below describes the function of the option links associated with Power configuration. The default configuration is indicated by BOLD text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R4	Power Source	**Board can be powered from PWR connector**	Disable external power connector	R14, R21, R82
R14	Power Source	Board is powered from VBUS	**Board is powered by another source**	R4, R21, R82
R17	Power Source	Connects external 3.3V power source to Board_VCC	**Disconnects external 3.3V power source from Board_VCC**	R41
R21	Power Source	**Board can be powered from E8a**	Disable E8a power source	R4, R14, R82
R23	Microcontroller Power Supply	**Supply power to Microcontroller**	Fit Low ohm resistor to measure current.	
R41	Power Source	**Connects regulated 3.3V voltage source to Board_VCC**	Disconnects regulated 3.3V voltage source from Board_VCC	R41
R76	LCD Power Source	LCD powered from External 5V source PWR.	**LCD Powered from a different source.**	R79, R81
R78	CON 5V connection	CON 5V connected to External power source PWR.	**CON 5V connected to a different place.**	R80, R82
R79	LCD Power Source	LCD powered from VBUS 5V source.	**LCD powered from a different source.**	R76, R81
R80	CON 5V connection	CON 5V connected to VBUS 5V source	**CON 5V connected to a different place.**	R78, R82
R81	LCD Power Source	**LCD powered from Microprocessor 5V Source.**	LCD powered from a different source.	R76, R79
R82	CON 5V connection	**CON 5V connected to Microprocessor 5V Source**	CON 5V connected to a different place.	R4, R14, R21, R78, R80

Table 6-6: Power configuration links

Table 6-7 below describes the function of the option links associated with Analog configuration. The default configuration is indicated by BOLD text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R34	Analog Input	AN0 channel connected to JA1	**AN0 channel disconnected from JA1**	R42
R42	Analog Input	**AN0 channel connected to POT**	AN0 channel disconnected from POT	R34
R43	Voltage Reference Source	**Voltage Reference set to AVcc signal**	Voltage Reference taken from external connector (JA1-7).	R99
R85	Analog Voltage Source	Analog Voltage Source from external connector.	**Analog voltage source from Board_Vcc.**	R86, R131
R86	Analog Voltage Source	**Links analog ground to digital ground.**	Isolates analog ground from digital ground.	R85,R131
R99	Voltage Reference Source	Voltage Reference set to AVcc signal	**Voltage Reference taken from external connector (J4).**	R43
R131	Analog Voltage Source	**Analog voltage source from on board Vcc.**	Analog Voltage Source from external connector.	R85,R86

Table 6-7: Analog configuration links

Table 6-8 below describes the function of the option links associated with Pin function configuration. The default configuration is indicated by BOLD text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R47	Pin function select	PIN 28 connected to A14 on JA3	**PIN 28 disconnected from A14**	R48
R48	Pin function select	**PIN 28 connected to IO6 on JA1**	PIN 28 disconnected from IO6	R47
R49	Pin function select	PIN 83 connected to LWRn on JA3	**PIN 83 disconnected from JA3**	R105
R50	Pin function select	**PIN 31 connected to PTTX**	PIN 31 disconnected from PTTX	R61
R51	Pin function select	**PIN 20 connected to IO0 on JA1**	PIN 20 disconnected from IO0	R52
R52	Pin function select	PIN 20 connected to A8 on JA3	**PIN 20 disconnected from A8**	R51
R53	Pin function select	**PIN 21 connected to IO1 on JA1**	PIN 21 disconnected from IO1	R54
R54	Pin function select	PIN 21 connected to A9 on JA3	**PIN 21 disconnected from A9**	R53
R55	Pin function select	**PIN 23 connected to IO2 on JA1**	PIN 23 disconnected from IO2	R56
R56	Pin function select	PIN 23 connected to A10 on JA3	**PIN 23 disconnected from A10**	R55
R57	Pin function select	**PIN 25 connected to IO3 on JA1**	PIN 25 disconnected from IO3	R58
R58	Pin function select	PIN 25 connected to A11 on JA3	**PIN 25 disconnected from A11**	R57
R59	Pin function select	PIN 27 connected to A13 on JA3	**PIN 27 disconnected from A13**	R60
R60	Pin function select	**PIN 27 connected to IO5 on JA1**	PIN 27 disconnected from IO5	R59
R61	Pin function select	PIN 31 connected to A17 on JA3	**PIN 31 disconnected from A17**	R50
R62	Pin function select	PIN 26 connected to A12 on JA3	**PIN 26 disconnected from A12**	R63
R63	Pin function select	**PIN 26 connected to IO4 on JA1**	PIN 26 disconnected from IO4	R62
R64	Pin function select	PIN 29 connected to A15 on JA3	**PIN 29 disconnected from A15**	R65
R65	Pin function select	**PIN 29 connected to IO7 on JA1**	PIN 29 disconnected from IO7	R64
R66	Pin function select	**PIN 32 connected to PTRX**	PIN 32 disconnected from PTRX	R67
R67	Pin function select	PIN 32 connected to A18 on JA3	**PIN 32 disconnected from A18**	R66
R68	Pin function select	**PIN 33 connected to SCK2**	PIN 33 disconnected from SCK2	R69
R69	Pin function select	PIN 33 connected to A19 on JA3	**PIN 33 disconnected from A19**	R68
R70	Pin function select	**PIN 36 connected to Un on JA2**	PIN 36 disconnected from Un	R71
R71	Pin function select	PIN 36 connected to A21 on JA3	**PIN 36 disconnected from A21**	R70
R72	Pin function select	**PIN 35 connected to Up on JA2**	PIN 35 disconnected from Up	R73
R73	Pin function select	PIN 35 connected to A20 on JA3	**PIN 35 disconnected from A20**	R72
R74	Pin function select	**PIN 37 connected to Vp on JA2**	PIN 37 disconnected from Vp	R75
R75	Pin function select	PIN 37 connected to A22 on JA3	**PIN 37 disconnected from A22**	R74
R91	Pin function select	**PIN 45 connected to DA0 on JA1**	PIN 45 disconnected from DA0	R113
R93	Pin function select	**PIN 44 connected to DA1 on JA1**	PIN 44 disconnected from DA1	R111
R105	Pin function select	**PIN 83 connected to SW3**	PIN 83 disconnected from SW3	R49
R111	Pin function select	PIN 44 connected to AN15 on JA5	**PIN 44 disconnected from AN15**	R93

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R113	Pin function select	PIN 45 connected to AN14 on JA5	**PIN 45 disconnected from AN14**	R91
R133	Pin function select	**PIN 30 connected to LED2**	PIN 30 disconnected from LED2	R130
R130	Pin function select	PIN 30 connected to A16 on JA3	**PIN 30 disconnected from A16**	R133

Table 6-8: Pin function configuration links

Table 6-9 below describes the function of the option links associated with Clock configuration. The default configuration is indicated by BOLD text.

Option Link Settings				
Reference	Function	Fitted	Alternative (Removed)	Related To
R107	Main OscillatorCrystal	Parallel resistor for crystal	**Not fitted**	
R109	48MHz USB Crystal Oscillator	Parallel resistor for crystal	**Not fitted**	
R110	Main Oscillator Source	Connects on board clock to MCU	External Clock Source	R112,R121
R112	Main Oscillator Source	Connects external clock to MCU	**Disconnects external clock connection to MCU**	R110,R121
R114	48MHz USB Crystal Oscillator	Connected to Ring Connector	**Disconnected from Ring Connector**	R117, R118
R117	48MHz USB Crystal Oscillator	**Force clock Input low. USB uses main oscillator**	USB Uses 48MHz Oscillator	R114,R118
R118	48MHz USB Crystal Oscillator	Connected to Ring Connector	**Disconnected from Ring Connector**	R114,R117
R121	Main Oscillator Source	Connects external clock to MCU	**Disconnects external clock connection to MCU**	R110,R112
R129	Crystal Selection	Fit if 16MHz Crystal Fitted	**24MHz Crystal Fitted**	R132
R132	Crystal Selection	**Fit if 24MHz Crystal Fitted**	16MHz Crystal Fitted	R129

Table 6-9: Clock configuration links

6.7. Oscillator Sources

A crystal oscillator is fitted on the CPU board and used to supply the main clock input to the Renesas microcontroller. Another crystal oscillator is provided to drive the USB clock. Table 6-10 details the oscillators that are fitted and alternative footprints provided on this CPU board:

Component		
Crystal (X1)	Not Fitted	48MHz (HC49/4H package)
Crystal (X2)	Fitted	24MHz (HC49/4H package)

Table 6-10: Oscillators / Resonators

Warning: When replacing the default oscillator with that of another frequency, the debugging monitor will not function unless the following are corrected:

- FDT programming kernels supplied are rebuilt for the new frequency

The user is responsible for code written to support operating speeds other than the default.

6.8. Reset Circuit

The CPU Board includes a simple latch circuit that links the mode selection and reset circuit. This provides an easy method for swapping the device between Boot Mode, User Boot Mode and User mode. This circuit is not required on customer's boards as it is intended for providing easy evaluation of the operating modes of the device on the RSK. Please refer to the Hardware Manual for more information on the requirements of the reset circuit.

The reset circuit operates by latching the state of the boot switch on pressing the reset button. This control is subsequently used to modify the mode pin states as required.

The mode pins should change state only while the reset signal is active to avoid possible device damage.

The reset is held in the active state for a fixed period by a pair of resistors and a capacitor. Please check the reset requirements carefully to ensure the reset circuit on the user's board meets all the reset timing requirements.

6.9. USB Port

This RSK has a Full-speed (12 Mbps) USB port compliant to USB 2.0 specification. It is available as USB port on the RSK. This port allows Boot mode programming using USB Direct connection and FDT. For more details please refer to *H8S/2215 Group Hardware Manual.*

Chapter 7. Modes

The CPU board can be configured in User mode and Boot mode. User mode may be used to run and debug user code, while Boot mode may only be used to program the Renesas microcontroller with program code via the USB interface. Further details of programming the flash are available in the H8S/2215 Group hardware manual.

Note: Please note that, jumper 'J13' needs to be fitted in order to use the E10A debugger.

The CPU board provides the capability of changing between User and Boot / User Boot modes using a simple latch circuit. This is only to provide a simple mode control on this board when the E10A debugger is not in use.

To manually enter boot mode, press and hold the SW1/BOOT. The mode pins are held in their boot states while reset is pressed and released. Release the boot button. The BOOT LED will be illuminated to indicate that the microcontroller is in boot mode.

More information on the operating modes can be found in the device hardware manual.

7.1.1. Boot mode

The boot mode settings for this CPU board are shown in Table 7-1 below:

MD2	MD1	**MD0**	**LSI State after Reset End**
1	0	1	Boot Mode

Table 7-1: Mode pin settings

7.1.2. User Mode

The H8S/2215R supports four user modes. The memory map in all of these modes is 16Mbyte in size. The default user mode for CPU board supporting H8S2215R is mode 7.

MD2	MD1	**MD0**	**LSI State after Reset End**
1	1	1	User Mode

Table 7-2: Mode pin settings

Chapter 8. Programming Methods

The board is intended for use with HEW and the supplied E10A debugger. This board can also be programmed using the H8S/2215 on-chip USB port. Refer to *H8S/2215 Group Hardware Manual* for details of programming the microcontroller without using E10A debugger.

Note: Please note that, jumper 'J13' needs to be fitted in order to use the E10A debugger.

Chapter 9.Headers

9.1. Microcontroller Headers

Table 9-1 to Table 9-4 show the microcontroller pin headers and their corresponding microcontroller connections. The header pins connect directly to the microcontroller pin unless otherwise stated.

J1					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	EMLEn	1	2	D8	2
3	D9	3	4	D10	4
5	D11	5	6	D12	6
7	D13	7	8	D14	8
9	D15	9	10	Board_VCC	10
11	A0	11	12	GROUND	12
13	A1	13	14	A2	14
15	A3	15	16	A4	16
17	A5	17	18	A6	18
19	A7	19	20	A8_IO0	20
21	A9_IO1	21	22	No connection	22
23	A10_IO2	23	24	No connection	24
25	A11_IO3	25	26	A12_IO4	26
27	A13_IO5	27	28	A14_IO6	28
29	A15_IO7	29	30	A16_LED2	30

Table 9-1: J1

J2					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	A17_PTTX	31	2	A18_PTRX	32
3	A19_SCK2	33	4	No connection	34
5	A20_Up	35	6	A21_Un	36
7	A22_Vp	37	8	Vn	38
9	IRQ0n	39	10	Wp	40
11	Wn	41	12	TRIGb	42
13	CON_AVSS	43	14	AN15_DA1	44
15	AN14_DA0	45	16	AN3	46
17	AN2	47	18	AN1	48
19	AN0_ADPOT	49	20	CON_VREF	50
21	CON_AVCC	51	22	No connection	52
23	USPND	53	24	No connection	54
25	VBUS_DET	55	26	UBPMn	56
27	Board_VCC (DRVCC)	57	28	No connection (USD-)	58
29	No connection (USD+)	59	30	GROUND (DRVSS)	60

Table 9-2: J2

J3					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	GROUND	61	2	GROUND (DRVSS)	62
3	No connection (PLLCAP)	63	4	CON_PLLVCC	64
5	CON_XTAL48	65	6	CON_EXTAL48	66
7	MD0	67	8	MD1	68
9	FWE	69	10	NMI	70
11	STBYn	71	12	RESn	72
13	GROUND	73	14	CON_XTAL	74
15	Board_VCC	75	16	CON_EXTAL	76
17	MD2	77	18	PHI	78
19	ASn	79	20	RDn	80
21	HWRn	81	22	No connection	82
23	LWRn_ADTRG_IRQ3n	83	24	No connection	84
25	LED1	85	26	LED0	86
27	IRQ2n	87	28	TxD0	88
29	TxD0	89	30	SCK0	90

Table 9-3: J3

J4					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	TxD1	91	2	RxD1	92
3	SCK1	93	4	PUD+	94
5	No connection	95	6	TRISTn	96
7	TMR1	97	8	TMR0	98
9	UD	99	10	TRIGa	100
11	LED3	101	12	IRQ7n	102
13	CS2n	103	14	CS1n	104
15	CS0n	105	16	TDO	106
17	TCK	107	18	TMS	108
19	TRISTn	109	20	TDI	110
21	D0_DLCDRS	111	22	No connection	112
23	D1_DLCDE	113	24	No connection	114
25	D2	115	26	D3	116
27	D4_DLCDD4	117	28	D5_DLCDD5	118
29	D6_DLCDD6	119	30	D7_DLCDD7	120

Table 9-4: J4

9.2. Application Headers

Table 9-5 and Table 9-9 below show the standard application header connections.

JA1							
Pin	Generic Header Name	CPU board Signal Name	Device Pin	Pin	Generic Header Name	CPU board Signal Name	Device Pin
1	Regulated Supply (5V)	---	---	2	Regulated Supply 1 (Gnd)	---	---
3	Regulated Supply (3V3)	---	---	4	Regulated Supply 2 (Gnd)	---	---
5	Analog Supply	AVcc*	51	6	Analog Supply	AVss	43
7	Analog Reference	AVref*	50	8	ADTRG	ADTRG_IRQ3n*	83
9	AD0	AN0*	49	10	AD1	AN1	48
11	AD2	AN2	47	12	AD3	AN3	46
13	DAC0	DAC0*	45	14	DAC1	DA1*	44
15	IOPort	IO0*	20	16	IOPort	IO1*	21
17	IOPort	IO2*	23	18	IOPort	IO3*	25
19	IOPort	IO4*	26	20	IOPort	IO5*	27
21	IOPort	IO6*	28	22	IOPort	IO7*	29
23	Open drain IRQ3n	ADTRG_IRQ3n*	83	24	IIC_EX	---	---
25	IIC_SDA	---	---	26	IIC_SCL	---	---

Table 9-5: JA1 Standard Generic Header

JA2							
Pin	Generic Header Name	CPU board Signal Name	Device Pin	Pin	Generic Header Name	CPU board Signal Name	Device Pin
1	Open drain	RESn	72	2	External Clock Input	CON_EXTAL*	76
3	Open drain	NMI	70	4	Regulated Supply (Vss)	---	---
5	Open drain output	---	---	6	Serial Port	TxD0*	88
7	Open drain WUP	IRQ0	39	8	Serial Port	RxD0*	89
9	Open drain	IRQ2	87	10	Serial Port	SCK0*	90
11	Up/down	UD	99	12	Serial Port Handshake	---	---
13	Motor control	Up*	35	14	Motor control	Un*	36
15	Motor control	Vp*	37	16	Motor control	Vn	38
17	Motor control	Wp*	40	18	Motor control	Wn	41
19	Output	TMR0	98	20	Output	TMR1	97
21	Input	TRIGa	100	22	Input	TRIGb	42
23	Open drain	ADTRG_IRQ3n*	83	24	Tristate Control	TRISTn	96
25	Reserved	---	---	26	Reserved	---	---

Table 9-6: JA2 Standard Generic Header

JA3							
Pin	Generic Header Name	CPU board Signal Name	Device Pin	Pin	Generic Header Name	CPU board Signal Name	Device Pin
1	Address Bus	A0	11	2	Address Bus	A1	13
3	Address Bus	A2	14	4	Address Bus	A3	15
5	Address Bus	A4	16	6	Address Bus	A5	17
7	Address Bus	A6	18	8	Address Bus	A7	19
9	Address Bus	A8*	20	10	Address Bus	A9*	21
11	Address Bus	A10*	23	12	Address Bus	A11*	25
13	Address Bus	A12*	26	14	Address Bus	A13*	27
15	Address Bus	A14*	28	16	Address Bus	A15*	29
17	Data Bus	D0_DLCDRS	111	18	Data Bus	D1_DLCDE	113
19	Data Bus	D2	115	20	Data Bus	D3	116
21	Data Bus	D4_DLCD4	117	22	Data Bus	D5_DLCD5	118
23	Data Bus	D6_DLCD6	119	24	Data Bus	D7_DLCD7	120
25	Read/Write Control	RDn	80	26	Read/Write Control	LWRn*	83
27	Memory Select	CS0n	105	28	Memory Select	CS1n	104
29	Data Bus	D8	2	30	Data Bus	D9	3
31	Data Bus	D10	4	32	Data Bus	D11	5
33	Data Bus	D12	6	34	Data Bus	D13	7
35	Data Bus	D14	8	36	Data Bus	D15	9
37	Address Bus	A16*	30	38	Address Bus	A17*	31
39	Address Bus	A18*	32	40	Address Bus	A19*	33
41	Address Bus	A20*	35	42	Address Bus	A21*	36
43	Address Bus	A22*	37	44	External Device Clock	PHI	78
45	Memory Select	CS2n	103	46	Bus Control	ASn	79
47	Data Bus Strobe	HWRn	81	48	Data Bus Strobe	LWRn*	83
49	Reserved			50	Reserved		

Table 9-7: JA3 Expansion bus Header

JA5							
Pin	Generic Header Name	CPU board Signal Name	Device Pin	Pin	Generic Header Name	CPU board Signal Name	Device Pin
1	AD4	AN14*	45	2	AD5	AN15*	44
3	AD6	---	---	4	AD7	---	---
5	CAN1TX	---	---	6	CAN1RX	---	---
7	CAN2TX	---	---	8	CAN2RX	---	---
9	AD8	---	---	10	AD9	---	---
11	AD10	---	---	12	AD11	---	---
13	TIOC0A	---	---	14	TIOC0B	---	---
15	TIOC0C	---	---	16	M2_TRISTn	---	---
17	TCLKC	---	---	18	TCLKD	---	---
19	M2_Up	---	---	20	M2_Un	---	---
21	M2_Vp	---	---	22	M2_Vn	---	---
23	M2_Wp	---	---	24	M2_Wn	---	---

Table 9-8: JA5 Optional Generic Header

JA6								
Pin	Generic Header Name		CPU board Signal Name	Device Pin	Pin	Generic Header Name	CPU board Signal Name	Device Pin
1	DMA		---	---	2	DMA	---	---
3	DMA		---	---	4	Standby (Open drain)	STBYn	71
5	Host Serial		RS232TX*	---	6	Host Serial	RS232RX*	---
7	Serial Port		RxD1	92	8	Serial Port	TxD1	91
9	Serial Port	Synchronous	PTTX*	31	10	Serial Port	SCK1	93
11	Serial Port	Synchronous	SCK2*	33	12	Serial Port Synchronous	PTRX*	32
13	Reserved				14	Reserved		
15	Reserved				16	Reserved		
17	Reserved				18	Reserved		
19	Reserved				20	Reserved		
21	Reserved				22	Reserved		
23	Reserved				24	Reserved		
25	Reserved				26	Reserved		

Table 9-9: JA6 Optional Generic Header

* Marked pins are affected by option links (see 6.6).

Chapter 10. Code Development

10.1. Overview

Note: For all code debugging using Renesas software tools, the CPU board must either be connected to a PC serial port via a serial cable or a PC USB port via an E10A. An E10A is supplied with the RSK product.

Due to the continuous process of improvements undertaken by Renesas the user is recommended to review the information provided on the Renesas website at www.renesas.com to check for the latest updates to the Compiler and Debugger manuals.

10.2. Compiler Restrictions

The compiler supplied with this RSK is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 64k code and data. To use the compiler with programs greater than this size you will need to purchase the full tools from your distributor.

Warning: The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

10.3. Breakpoint Support

This RSK is supplied with E10A emulator which supports breakpoints in ROM. For more details on breakpoints & E10A functions please refer to 'H8S, H8SX Family E10A-USB Emulator User's Manual'.

10.4. Memory Map

The memory map shown in this section visually describes the locations of the each memory areas when operating the RSK in the default mode (Mode 7).

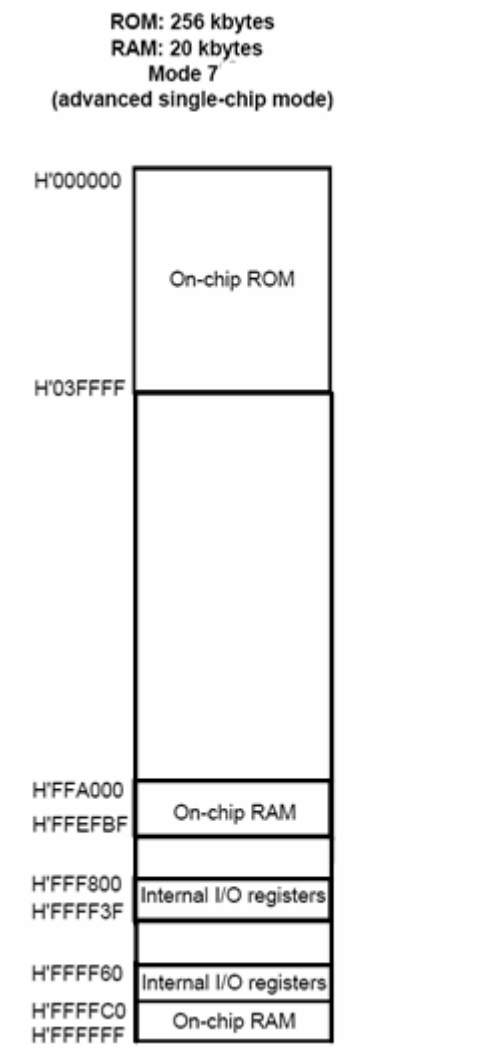

Figure 10-1: Memory Map

Chapter 11. Component Placement

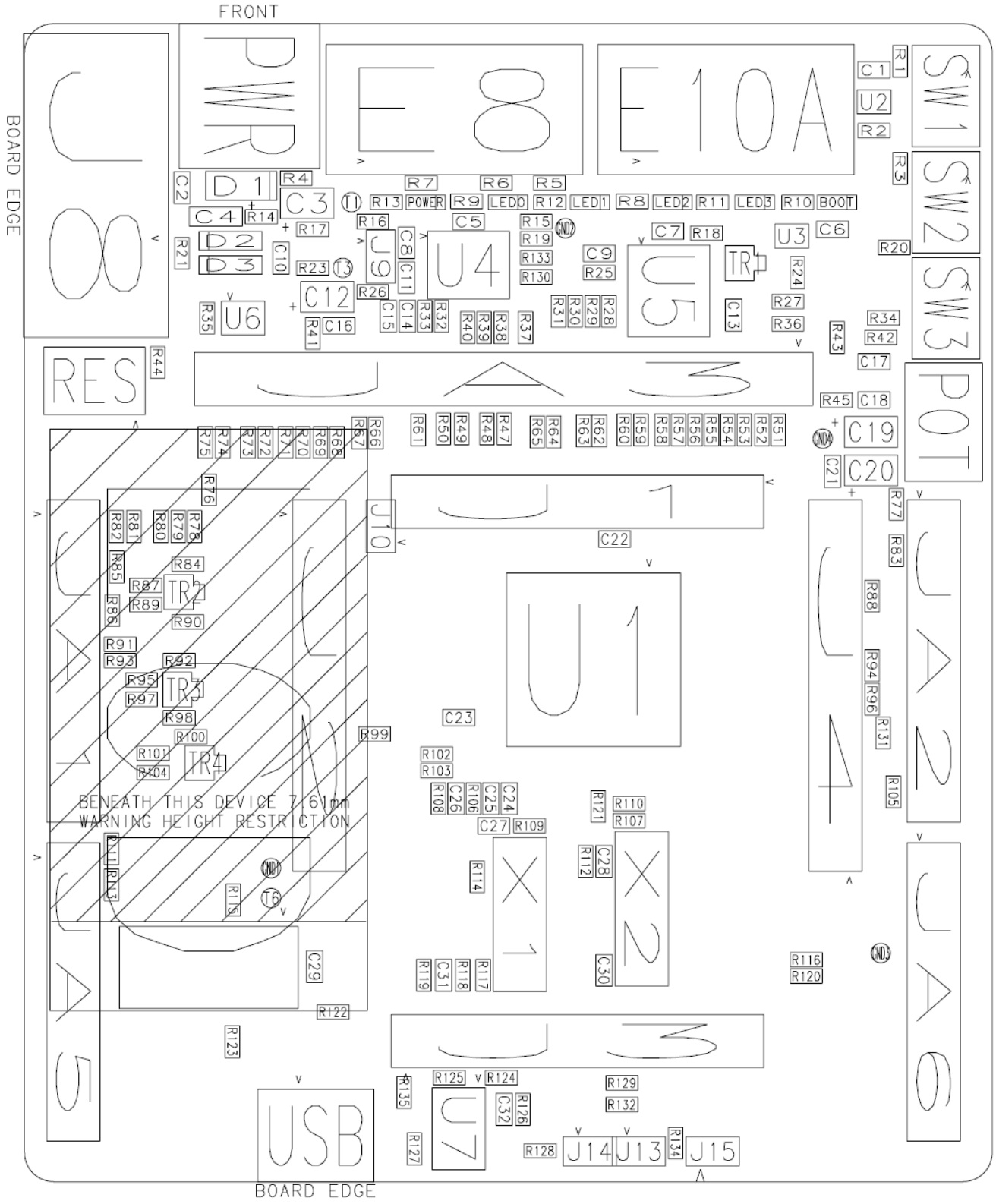

Figure 11-1: Component Placement

Chapter 12. Additional Information

For details on how to use High-performance Embedded Workshop (HEW), refer to the HEW manual available on the CD or installed in the Manual Navigator.

For information about the H8S/2215R series microcontrollers please refer to the *H8S/2215 Group Hardware Manual*

For information about the H8S/2215R assembly language, please refer to the *H8S Series Programming Manual*

For information about the E10A Emulator, please refer to the *H8S, H8SX Family E10A-USB Emulator User's Manual*

Further information available for this product can be found on the Renesas website at:

http://www.renesas.com/renesas_starter_kits

General information on Renesas Microcontrollers can be found on the following website.

Global: http://www.renesas.com/

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Renesas Electronics Corporation
1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan

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