

# **ARM9** Microcontroller

**Graphic Solution for Embedded Applications** 



- > Powerful Graphic Controller with Accelerator
- > Various Operating Systems
- > Rich Set of On-Chip Peripherals
- > Industrial Temperature Range
- > Class B Compliant (IEC60730)



# Introduction

### A new Microcontroller combines a 32-bit ARM processor with graphics control and processing functionality to simplify display applications

The TMPA9x family brings together a high-performance 32-bit core, with comprehensive graphics control and processing functionality, and a variety of on-board connectivity and peripheral options. These new devices considerably reduce the development time and component count.

The new low power products feature an ARM926EJ-CPU™ core, LCD controller with image process accelerator, touch screen interface, CMOS image sensor input, USB Device and Host, SD Host Controller and further comprehensive connectivity options.

### TMPA900CMXBG / TMPA901CMXBG

#### Key Features:

Core Operating voltage Max. operating freq. Internal memory Debug circuit Power saving operation

#### **Built-in functions:**

SD Host Controller LCD Ctrl. LCDA

USB Device USB Host 10 bit A/DC Touch screen I/F 16 bit timer 1/0 RTC CMOS-Camera I/F

Serial interfaces

Memory I/F

DMA OFD PMC Package

ARM926EJ-S, 16kB I\$ and 16kB D\$ I/O=1.7~3.9V, 3,0V ~3,6V 200MHz @ 0~70°C, 150MHz @ -20~+85°C Boot-ROM: 16kB, RAM: 32kB JTAG Interface Clock gear (f/2, f/4 or f/8) Standby mode (NORMAL/Power Cut Mode)

Hi-speed, 50MHz, High Capacity, 32GB Mono, STN Color, 16/24bit TFT Color Display Data Accelerator supports Scaling, Blending and Rotation High speed (480Mbps) Full speed (12Mbps) 8ch (3.0-3.6V), 1.39µs 1ch 6ch (2ch PWM output) 91 (43 @TMPA901) 1ch (CMSI) Up to 1,3Mpixel, YUV-to-RGB conversion (only TMPA900) SSP(SPI) x 2ch (1ch @TMPA901) UART x 3ch (2ch @TMPA901) I<sup>2</sup>C x 2ch (1ch @TMPA901) I<sup>2</sup>S x 2ch (1ch @TMPA901) 16/32bit SDR SDRAM 16/32bit DDR SDRAM NAND Flash 8bit bus (SLC/4LC) 8ch Oscillation Frequency Detector (IEC60730) Power Management Circuit TMPA900: FBGA289 (15mmx15mm 0.8mm ball pitch) TMPA901: FBGA177 (13mmx13mm 0.8mm ball pitch) LCD Accelerator



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### Blending

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### ARM9 Microcontroller TMPA900CMXBG

# > Multi-Layer Bus System

A 7-Layer multi bus system has been implemented in order to increase the overall performance drastically. Even MPEG4 or H.264 videos can be handled while scaling is supported by the LCD accelerator.

Following bus masters can operate individually:

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Bus Master 1:	CPU data
Bus Master 2:	CPU instruction
Bus Master 3:	LCD controller
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- Bus Master 4: LCD data process accelerator
- Bus Master 5: DMA controller 1
- Bus Master 6: DMA controller 2
- Bus Master 7: USB device controller



### Oscillation Frequency Detector (OFD)

OFD is the required H/W implementation to comply with the "*Standard for safety of Electrical Equipment*" in accordance with IEC60730 (Class B). It generates a Reset when the high oscillation frequency ( $f_{OSC}$ ) falls or rises outside of the normal frequency range specified by the lower and higher detection frequency setting registers.

An abnormal frequency condition can be detected via the external  $\mathsf{OFD}_{\mathsf{OUTn}}$  pin. The high-frequency clock ( $f_{\mathsf{OSC}}$ ) is used as a detection clock, and the low-frequency clock ( $f_{s:}$  32KHz) is used as a reference clock. If the 32 KHz reference clock stops due to an external cause, the OFD detects an abnormal condition and resets the internal circuitry as well.



### Overview Toshiba ARM Display Microcontroller



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# ARM9 Microcontroller TMPA900CMXBG

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Product No.	Core	CPU Clock (MHz.)	ROM (kB)	RAM (kB)	Package	LCD Controller	LCD Accelerator	USB Host/Device	SPI Ch.	UART/SIO Ch.	I2C/SIO Ch.	Memory Controller	ADC 10-bit Ch.	16-bit Timer	RTC / WDT	I/O Ports	Supply Voltage	Special Features
TMPA900CMXBG <sup>2)</sup>	ARM926EJ-S	200*	-	32	FBGA 289	$\checkmark$	$\checkmark$	H/D	2	3	2	1	8	6	$\checkmark$	91	1.7~3.6	SD Host, Touch I/F, CMOS- Camera I/F, OFD**
TMPA901CMXBG <sup>2)</sup>	ARM926EJ-S	200*	-	32	FBGA 177	$\checkmark$	$\checkmark$	H/D	1	2	1	1	4	6		43	1.7~3.6	Touch I/F; OFD
TMPA910CRAXBG <sup>1)</sup>	ARM926EJ-S	200*	-	56	FBGA 361	$\checkmark$	$\checkmark$	D	2	2	2	1	6	6	$\checkmark$	114	1.7~3.6	SD Host, Touch I/F, CMOS- Camera I/F
TMPA911CRAXBG <sup>1)</sup>	ARM926EJ-S	200*	-	56	FBGA 361			D	2	2	2	1	6	6		114	1.7~3.6	Touch I/F, CMOS-Camera I/F
TMPA912CMAXBG <sup>1)</sup>	ARM926EJ-S	200*	-	32	FBGA 361			D	2	2	2	1	6	6		114	1.7~3.6	Touch I/F, CMOS-Camera I/F
TMPA913CRHXBG <sup>1)</sup>	ARM926EJ-S	200*	-	16	FBGA 361			D	2	2	2	1	6	6		114	1.7~3.6	
* 200MHz @ 0°C to 70°C,	150MHz @ -20°C to +85°C 1) Starter Kit Order No.: BMKSTOPASA910(DCE)																	

\*\* OFD = Oscillation Frequency Detector

2) Starter Kit Order No.: BMKSTOPASA910(DCE)
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## > Reference Board/Starter Kit

### Compact size (11cm x 15cm)

### Supported MCUs

> TMPA900CMXBG, TMPA901CMXBG,

#### Features

- > Includes a 3.5" Display with Touch Screen
- > J-Link Interface
- > Ethernet Connection
- > USB Device & Host, RS232
- > Excellent Sound Input & Output (Audio DAC via I<sup>2</sup>S)
- > 2 x SD-Card Sockets (via SD-Host Controller & SPI)
- > JTAG Interface
- > Memory:
- > 64MB SDRAM, 32MB NOR Flash, 256MB NAND Flash
  > Extensive Software Support
  - > Segger for emWin, emOS, etc.
  - (www.Segger.de)
  - > Linux from Bplan
  - (www.bplan-gmbh.de)
  - > Windows CE
  - > Many Software examples available
- > Plug & Play! Excellent Tool for fast Prototyping
- > Schematics and Layout Data provided by Toshiba

# Linux Support

### BSP for the STK incl. Kernel, Device Drivers, etc.

- Dedicated Linux Distribution running under VMware on a standard PC
  - > For initial evaluation no dedicted Linux PC is required
  - > Tool Chain (GNU cross compiler, Editor, etc.)

#### Many S/W Examples

- > "Hello World", Slideshow, Video using MPLAYER
- > Advanced Tutorial including Set-up of the Board and the S/W







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#### Please visit our Web-Pages for more information: http://www.toshiba-components.com/microcontroller

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