EDK2215

USER MANUAL

FOR H8S/2215
ON-CHIP FLASH MICROCONTROLLER

Preface

Cautions

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Europe: http://www.hmse.com/

1. TABLE OF CONTENTS

2. START-UP INSTRUCTIONS

2.1. INSTALLING THE EVALUATION DEVELOPMENT KIT (EDK)

Please refer to the quick start guide provided for initial installation of the EDK.

A copy of the quick start guide and other information relating to this EDK at:

http://www.hmse.com/products/support.htm

Installing the EDK requires power and COM1serial connection to a host computer.

2.2. SERIAL CONNECTION

The serial communications cable for connecting the EDK to a host computer is supplied. The serial cable has 1:1 connectivity.

Figure 2-1 shows how to connect the EDK to a PC or notebook computer equipped with a nine pin D connector.

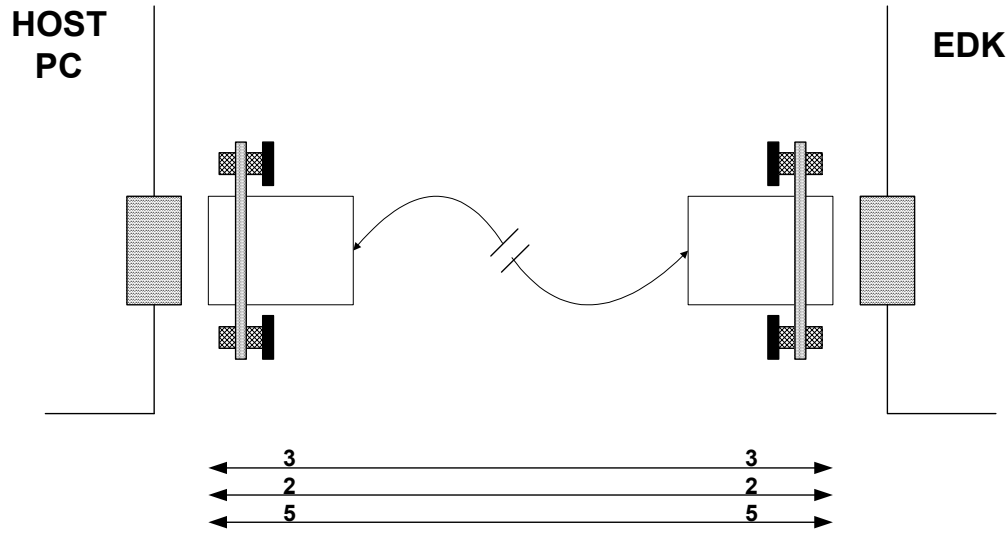


FIGURE 2-1: SERIAL CONNECTION TO PC/NOTEBOOK WITH DB-9 CONNECTOR (SUPPLIED)

2.3. POWER SUPPLY

The EDK hardware requires a power supply of +5V. Since total power consumption can vary widely due to external connections, port states, and memory configuration, use a power supply capable of providing at least 500mA at +5V DC ± 5%.

The design is specified for evaluation of the microcontroller and so does not include circuitry for supply filtering/noise reduction, under voltage protection, over current protection or reversed polarity protection. Caution should be used when selecting and using a power supply.

The power connector on the EDK is a 2.5mm Barrel connector. The center pin is the positive connection.

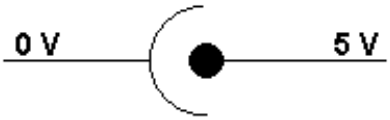


FIGURE 2-2: POWER SUPPLY CONNECTION

Caution: Existing customers using E6000 products note that the polarity of this board is opposite to that for the E6000. Use of the E6000 power supply with this board will damage both board and power supply.

3. EDK BOARD LAYOUT

The diagram shows a general layout of the EDK board.

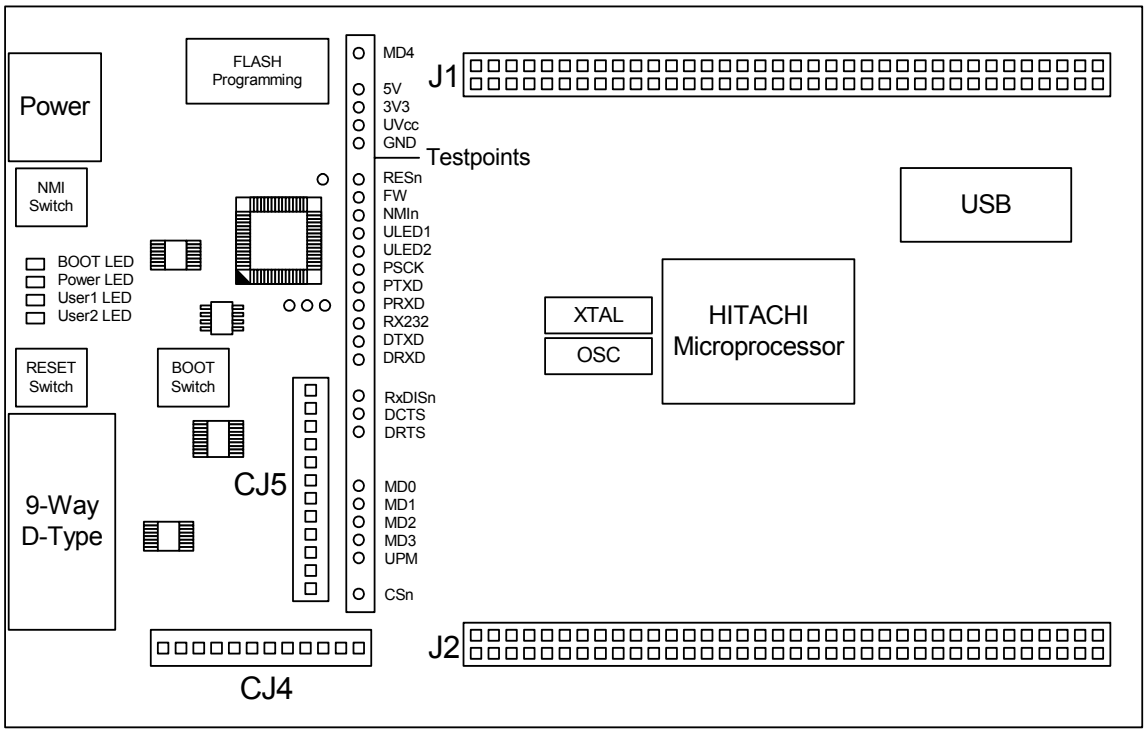


FIGURE 3-1: EDK BOARD LAYOUT

3.1. EDK BLOCK DIAGRAM

The diagram shows the connectivity of the components on the EDK board.

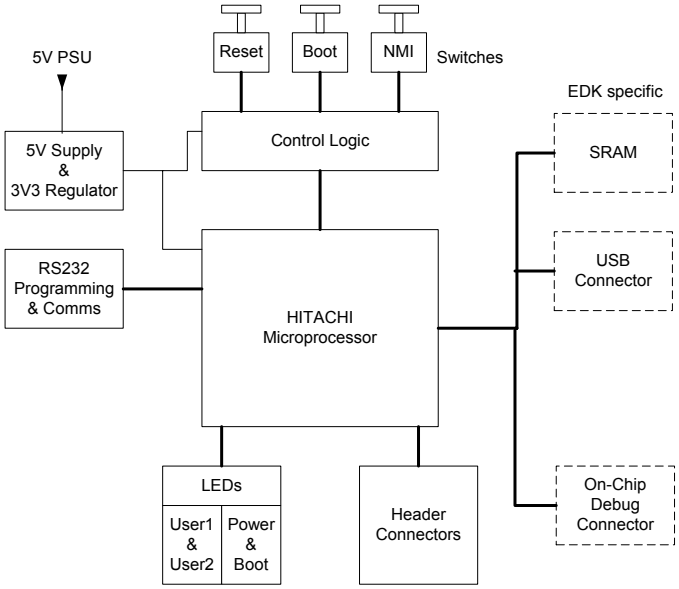


FIGURE 3-2: EDK BLOCK DIAGRAM

4. EDK OPERATION

4.1. USER INTERFACE

The EDK provides three buttons for influencing the operation of the board. The purpose of each button is clearly marked next to it. Refer to the board layout for positions (Section 3)

1. Reset Switch

This button provides the microcontroller with a timed reset pulse of at least 250mS.

2. Boot Switch

This button toggles the operating mode of the microcontroller. A complete description of this function is given in section 5.7.

3. NMI Switch

This button provides a de-bounced signal to the microcontroller for each operation of the button. There is no minimum or maximum activation time for this button.

4.2. SERIAL INTERFACE

The serial interface on the EDK board has several functions. The serial port on the microcontroller directly supports three wire serial interfaces. Options are provided on the board for the user to write handshaking routines using standard port pins. Other board option links allow users to control the entry and exit from boot mode using the same handshaking signals. Refer to section 5 for details on setting serial interface options.

4.2.1. CONNECTOR PIN DEFINITIONS

The EDK RS232 interface conforms to Data Communication Equipment (DCE) format allowing the use of 1-1 cables when connected to Data Terminal Equipment (DTE) such as an IBM PC. The cable used to connect to the EDK will affect the available board options. A fully wired cable can allow handshaking between the microcontroller and the host PC, subject to setting the board options and the availability of suitable host software. Handshaking is not supported as standard on the microcontroller so for normal use a minimal three-wire cable can be used. The minimum connections are unshaded in the following table.

EDK DB9 Connector Pin	Signal	Host DB9 Connector Pin
1	No Connection	1
2	EDK Tx Host Rx	2
3	EDK Rx Host Tx	3
4	No Connection	4
5	Ground	5
6	No Connection	6
7	* EDK CTS Host RTS	7
8	* EDK RTS Host CTS	8
9	No Connection	9

TABLE 4-1: RS232 INTERFACE CONNECTIONS

* These are not connected on the EDK by default. See section 5.4 for more details.

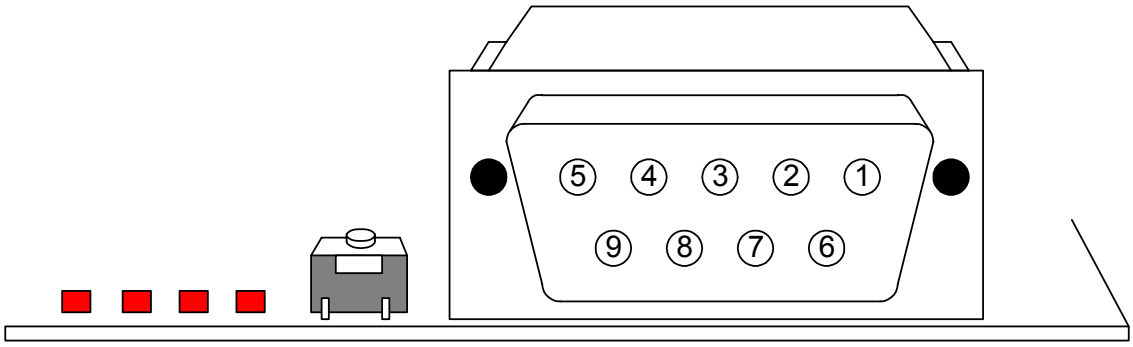


FIGURE 4-1: EDK SERIAL PORT PIN NUMBERING

4.2.2. CRYSTAL CHOICE

The operating crystal frequency has been chosen to support the fastest operation with the fastest serial operating speeds. The value of the crystal is 14.7456MHz.

The following table shows the baud rates and Baud Rate Register (BRR) setting required for each communication rate using the above default operating speed. It also confirms the resultant baud rate and the bit error rate that can be expected.

Baud Rate Register Settings for Serial Communication Rates												
SMR Setting:	**0**			**1**			**2**			**3**		
Comm. Baud	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**
110	invalid	invalid	Invalid	invalid	invalid	invalid	invalid	invalid	invalid	81	109.76	-0.22
300	invalid	invalid	Invalid	invalid	invalid	invalid	119	300	0.00	29	300	0.00
1200	invalid	invalid	Invalid	119	1200	0.00	29	1200	0.00	7	1125	-6.25
2400	239	2400	0.00	59	2400	0.00	14	2400	0.00	3	2250	-6.25
4800	119	4800	0.00	29	4800	0.00	7	4500	-6.25	1	4500	-6.25
9600	59	9600	0.00	14	9600	0.00	3	9000	-6.25	invalid	invalid	invalid
19200	29	19200	0.00	7	18000	-6.25	1	18000	-6.25	invalid	invalid	invalid
38400	11	38400	0.00	3	36000	-6.25	invalid	invalid	invalid	invalid	invalid	invalid
57600	9	57600	0.00	2	48000	-16.67	invalid	invalid	invalid	invalid	invalid	invalid
115200	3	115200	0.00	0	144000	25.00	invalid	invalid	invalid	invalid	invalid	invalid
230400*	2	192000	-16.67	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid
460800*	0	576000	25.00	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid

TABLE 4-2 CRYSTAL FREQUENCIES FOR RS232 COMMUNICATION

** Note: The device used to convert the RS232 serial information to logic signals for the microcontroller is limited to 120kBaud. The rates above this level can only be utilised if the user provides direct logic level communications.*

The default communication rate for the EDK is indicated by the shaded selection.

The user may replace the HC49/U surface mounted AT cut crystal with another of similar type within the operating frequency of the microcontroller device. Please refer to the hardware manual for the microcontroller for the valid operating range.

Alternatively the user may fit an oscillator module – or provide an external clock source. When providing an oscillator module or external source it is highly recommended that the load capacitors for the AT crystal are removed from the PCB. These are physically placed within the PCB outline of the oscillator module for easy location and to ensure they are removed when using this option.

When changing the crystal frequency the pre-loaded debugging monitor will not function. In this situation the user is responsible for providing code to evaluate the device away from the default operating speed.

4.2.3. REMOVABLE COMPONENT INFORMATION.

This information is provided to allow the replacement of components removed from the board as described in section 4.2.2.

Component	Cct. Ref	Value	Rating	Manufacturer
Load Resistor (X1)	R25	1MΩ	0805 1%	Welwyn WCR Series
Load capacitors (X1)	C18,C19	22pF	0603 10% 25V	AVX 0603 3 A 220 KAT

TABLE 4-3: REMOVABLE COMPONENT INFORMATION

Care must be taken not to damage the tracking around these components. Only use soldering equipment designed for surface mount assembly and rework.

4.3. SRAM

The SRAM device fitted to the board is a 4Mbit device allowing 256K x 16bit operation.

The SRAM is mapped to area 2 via CS2n (Port PG2), with a usable address range of H'400000 – H'43FFFF using address signals A1 to A18..

Glue logic provides the required SRAM control signals from the micon.

4.4. MEMORY MAP

Table 4-4 illustrates the EDK memory map for mode 6.

Section Start Section End	Section Allocation
H'0000 0000 H'0003 FFFF	On-Chip ROM
H'0040 0000 H'0043 FFFF	External RAM
H'0044 0000 H'00BFFFFF	External Address Space
H'00C00000 H'00DFFFFF	On-Chip USB Registers
H'00E00000 H'00FF8FFF	External Address Space
H'00FF9000 H'00FFAFFF	Reserved
H'00FF B000 H'00FF EFBF	On-Chip RAM
H'00FF EFC0 H'00FF F7FF	RESERVED
H'00FF F800 H'00FF FF3F	Internal I/O Registers
H'00FF FF40 H'00FF FF5F	RESERVED
H'00FF FF60 H'00FF FFBF	Internal I/O Registers
H'00FF FFC0 H'FFFFFFFF	On-Chip RAM

TABLE 4-4: MEMORY MAP (DEFAULT MODE 6)

4.5. SRAM ACCESS TIMING

External access timing is defined by several registers, allowing different types of devices to be addressed. The registers for the selection of wait states and signal extensions are given below with recommended values for the EDK.

Register	Address	Recommended Setting for EDK	Function
ABWCR	H'FED0	0x00	8bit R/W access. Bus Width Control Register. All areas set to 16 bit access
WCR	H'FED2	0xFF	16bit R/W access. Wait State Control Register – area 2 set to 3 wait states
PADDR	H'FE39	0x01	8bit R/W access. Port A data direction register. Address Bus (A16)
PBDDR	H'FE3A	0xFF	8bit R/W access. Port B data direction register. Address Bus (A15:8)
PCDDR	H'FE3B	0xFF	8bit R/W access. Port C data direction register. Address bus (A7:0)
PFDDR	H'FE3E	0x09	8bit R/W access. Port F data direction register. RAM control (HWRn/LWRn)
PGDDR	H'FE3F	0x02	8bit R/W access. Port G data direction register. Chip Select 2.

Please refer to the hardware manual of the microcontroller for further information on these register settings.

4.6. LEDS

The EDK has four red LEDs. The function of each LED is clearly marked on the silk screen of the PCB. Please refer to the board layout diagram for position information (Section 3).

When the board is connected to a power source the Power (PWR) led will illuminate. The Boot mode indication LED will illuminate when the microcontroller has been placed into Boot mode. Please see section 5.5 for more details of this function.

There are two LEDs dedicated for user control these are marked USR1 and USR2. Each LED will illuminate when the port pin is in a logical high state.

The user LEDs are connected to the following ports:

LED Identifier	Port Pin	Microcontroller Pin	Pin Functions on Port Pin
ULED1	P15	40	P15/TIOCB1/TCLKC/FSE0
ULED2	P16	41	P16/TIOCA2/IRQ1

TABLE 4-5: LED PORT CONNECTIONS

4.7 USB INTERFACE

Pin	Pin Function	Microcontroller Pin	Pin Function
1	VBUS	2	D-
3	D+	4	GND

The VBUS pin of this USB module must be connected to the USB's connector VBUS pin via a level shifter. This is because the USB module has a circuit that operates by detecting USB cable connection or disconnection.

Even if the power of the device incorporating the USB module is turned off, 5V power is applied to the USB connector's VBUS pin while the USB cable is connected to the device set. To protect the LSI from destruction a level shifter must be used. The part used in this design is a SN74LVC125APW from Texas Instruments. This allows voltage application to the pin even when the power is off.

5. BOARD OPTIONS

The EDK has a number of configuration settings set by jumpers CJ4 (A, B, C, D) CJ5 (A, B, C, D) and zero-ohm links. Common EDK functions can be set using the jumpers as described in sections 5.3 and 5.2. The additional zero-ohm links provide additional features that may be required to interface with other systems.

All the Jumper link settings are three pin options. There are four sets of options on each header.

The headers are numbered from 1 to 12 with pin 1 marked on the PCB by an arrow pointing to the pin. The diagram below shows the numbering of these jumper links and indicates jumpers fitted 1-2 for each three-pin jumper.

5.1. JUMPER LINKS

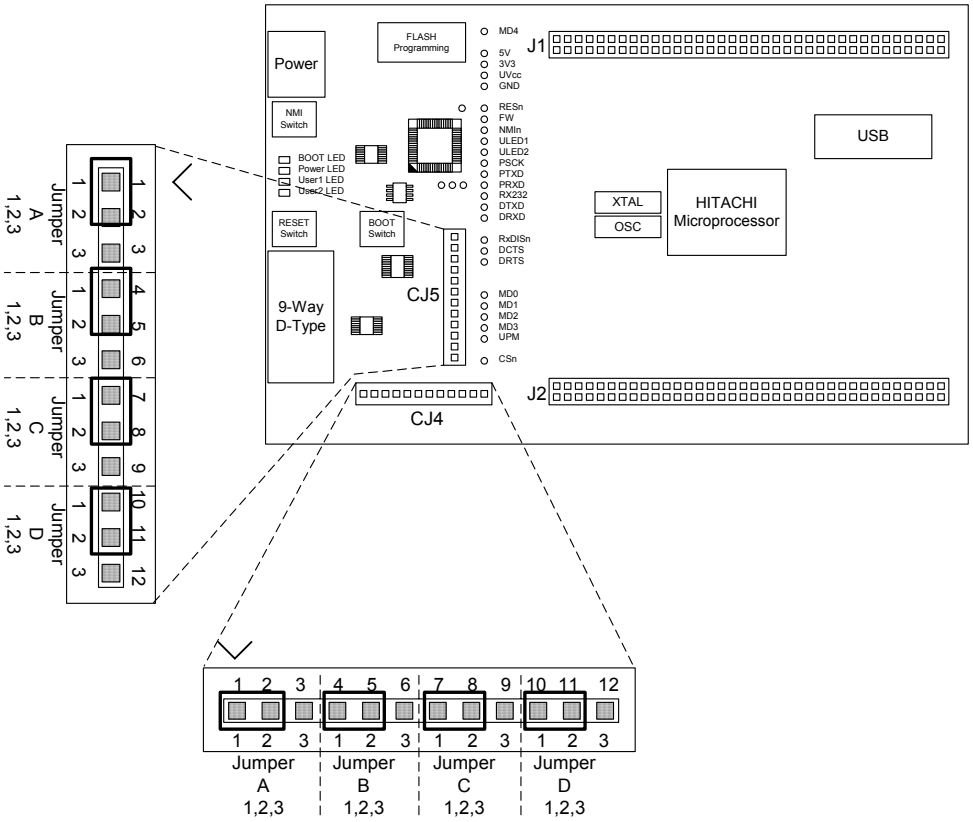


FIGURE 5-1: JUMPER CONFIGURATION

The following tables define each jumper and its settings.

5.2. USER MODE SETTINGS – CJ5

CJ5 is used to set the operating mode of the microcontroller.

These jumpers must be fitted at all times to ensure correct operation of the EDK.

Jumper	Function	Setting 1-2	Setting 2-3
CJ 5-A Default 2-3	User Mode Setting Bit 0	MD0 pulled High	**MD0 pulled Low**
CJ 5-B Default 1-2	User Mode Setting Bit 1	**MD1 pulled High**	MD1 pulled Low
CJ 5-C Default 1-2	User Mode Setting Bit 2	**MD2 pulled High**	MD2 pulled Low
CJ 5-D Default 2-3	User Mode Setting Bit 3	MD3 pulled High	**MD3 pulled Low**

TABLE 5-1: USER MODE: JUMPER SETTINGS (DEFAULT SETTINGS IN BOLD)

The default settings indicated in bold text place the microcontroller into Mode 6.

5.3. EDK OPTIONS – CJ4

The EDK options provide access to commonly used features of the EDK range.

These jumpers must be fitted at all times to ensure correct operation of the EDK.

Jumper	Function	Setting 1-2	Setting 2-3
CJ 4-A Default 2-3	Serial Receive Source	Disables the RS232 receive signal to enable the use of the Flash Programming Header	**Enables the RS232 receive signal. The Flash Programming Header* must not be used in this state.**
CJ 4-B Default 2-3	User Programming Mode	Disables the Flash write hardware protection. The flash can be overwritten in User Mode.	**Enables the Flash write hardware protection. The flash can not be overwritten in User Mode.**
CJ 4-C Default 2-3	CSn	**SRAM enabled**	SRAM disabled
CJ 4-D Default 1-2	UBPM	**Self-powered mode setting for USB**	Bus powered mode setting for USB

TABLE 5-2: BOARD OPTION: JUMPER SETTINGS (DEFAULT SETTINGS IN BOLD)

*See section 5.5

The following table lists the connections to each jumper pin.

Pin	Net Name	Description
1	UVCC	Microcontroller Supply Voltage
2	RXDISn	Disable Flash Header functions. Pulled low. (Enables RX232)
3	No Connection	No Connection
4	UVCC	Microcontroller Supply Voltage
5	UPM	CPLD Controlled option to set Flash Write (FW). Pulled low.
6	No Connection	No Connection
7	No Connection	No Connection
8	No Connection	No Connection
9	No Connection	No Connection
10	No Connection	No Connection
11	No Connection	No Connection
12	No Connection	No Connection

5.4. SERIAL PORT SELECTION

The programming serial port is connected to the RS232 connector by default. This allows direct programming of the EDK using the supplied software tools. A secondary serial port is available on the microcontroller and can be connected to the RS232 connector by changing some board option links. The additional port option allows the user to write messages or connect to other devices via the serial port while programming support is provided by the Flash programming header.

The following surface mount, zero-ohm link settings are fitted by default and connect the RS232 header to the programming serial port of the microcontroller.

Zero-ohm Link ID	Default	Function	Microcontroller Port Pin
CR20	Fitted	Transmit data from EDK	PA9
CR23	Fitted	Receive data to EDK	PA8
CR19	Not Fitted	Alternate Transmit data from EDK	PB3
CR22	Not Fitted	Alternate Receive data to EDK	PB2

TABLE 5-3: OPTION LINKS – DEFAULT SETTINGS

To enable the use of this alternate port the user must change the settings to those in the following table.

Zero-ohm Link ID	Default	Function	Microcontroller Port Pin
CR20	Not Fitted	Transmit data from EDK	PA9
CR23	Not Fitted	Receive data to EDK	PA8
CR19	Fitted	Alternate Transmit data from EDK	PB3
CR22	Fitted	Alternate Receive data to EDK	PB2

TABLE 5-4: OPTION LINKS – ALTERNATE SERIAL PORT

The user may implement a handshaking protocol on the EDK. This is not supported with the software tools supplied. To support this option two spare port pins have been allocated on the microcontroller. Using these port pins the CTS and RTS lines of the host serial interface can be controlled.

The user may also control the operation of the board via the same handshaking lines. This is not supported with the software tools supplied but may be written by the user. Using the CTS line the user may simulate pressing the boot button, see section:5.7. This will cause the EDK to swap into and out of Boot mode on each low-level activation of CTS. Feedback of the current mode is provided on the RTS line. A high level indicates boot mode and a low level indicates user mode.

The following settings are made by default, and ensure that there are no conflicts on unnecessary microcontroller pins.

Zero-ohm Link ID	Default	Function	Microcontroller Port Pin
CR12	Not Fitted	Mode State out from EDK	N/A (From CPLD*)
CR7	Not Fitted	Change Mode request to EDK	N/A (From CPLD*)
CR16	Not Fitted	Alternate RTS232 – Ready to send – from EDK	PF4
CR13	Not Fitted	Alternate CTS232 – Clear to send – to EDK	PF0

TABLE 5-5: OPTION LINKS – SERIAL PORT CONTROL

* See section 5.7

Note: These setting pairs are exclusive:
If CR12 and CR7 are fitted; CR16 and CR13 must not be fitted.
If CR16 and CR13 are fitted; CR12 and CR7 must not be fitted.

5.5. FLASH PROGRAMMING HEADER

The Flash Programming header is used with the Hitachi Flash Debug Board (FDB). The FDB is a USB based programming tool for control and programming of Hitachi microcontrollers, available separately from Hitachi. This header provides direct access for the FDB to control the EDK microcontroller.

To utilise this header the user must make the following changes to the board configuration.

1. Disable the RX232 signal from the RS232 transceiver.
   Jumper link CJ4-A is provided for this purpose. Please refer to section5.3.
2. Disable User Program Mode using jumper CJ4-B. Please refer to section5.3.

Caution: Do not operate the board with the user mode jumpers removed and the FDB disconnected as the microcontroller mode pins will float to an indeterminate state. This may damage the microcontroller device.

5.6. E10A HEADER

E10A/E10T is not supported on the EDK2215

5.7. BOOT CONTROL

The method for placing the microcontroller device in to Boot mode for reprogramming has been incorporated into a complex programmable logic device (CPLD). This is not necessary for most user designs but allows a measure of increased flexibility for the EDK designs. Mode transitions including boot mode transitions only require the reset to be held active while the mode settings are presented. On releasing reset the microcontroller will be in the required mode.

The logic design detects a power up event and provides a timed reset pulse to guarantee the reset of the device. At the end of the rest pulse the processor will be placed in user mode and any code in the device will execute.

During user mode the NMI button can be pressed at any time. This will provide a single de-bounced NMI interrupt to the device.

Pressing the boot button will cause the boot mode controller to reset the device and, during the reset period, present the required mode settings to start the device in boot mode. At the end of the reset period the boot mode settings will have been latched into the device which will then be ready to accept a boot mode connection via the RS232 interface or the flash programming header. Pressing the boot button during a normal reset will not cause the EDK to enter boot mode.

The boot mode settings are fixed at mode 0. The required mode settings are made using a tri-state capable buffer.

Note: The boot control device is programmed to support all possible EDK products.
For this reason the reset pulse is over 500ms. Repetitive activation of either the Boot or Reset buttons will restart the reset timer and extend the reset period. Pressing the boot button within the 500mS period of a reset will not cause the board to enter boot mode.

5.7.1. CPLD CODE

The code is based upon a four state machine providing a guaranteed reset period which can be extended by holding the relevant control input in the active state. When released the timer will extend the reset for approximately 500mS.

The states are split into two functions, one for User mode and one for Boot mode. The first state of each is used to hold the reset line active. When the timer expires then the second state is used to hold the device in the selected mode and wait for an external control signal to either move back into the user reset state or into the boot reset state.

5.7.2. STATE DIAGRAM

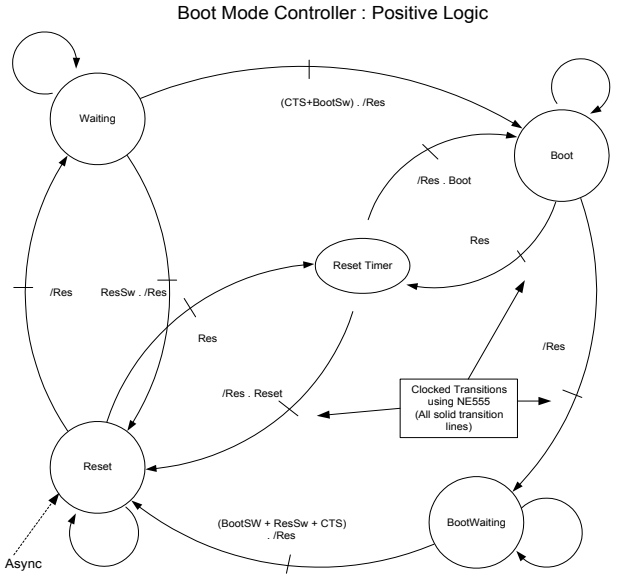


FIGURE 5-2: CPLD STATE DIAGRAM

6. MICROCONTROLLER HEADER CONNECTIONS

The following table lists the connections to each or the headers on the board.

6.1. HEADER J1

J1							
Pin No	**Function**	**EDK Symbol**	**Device pin**	**Pin No**	**Function**	**EDK Symbol**	**Device pin**
1	PC5, A5	PC5	17	2	PC4, A4	PC4	16
3	PC3, A3	PC3	15	4	PC2, A2	PC2	14
5	PC1, A1	PC1	13	6	VSS	Ground	6
7	PC0, A0	PC0	11	8	VCC	Uvcc	8
9	PD7, D15	PD7	9	10	PD6, D14	PD6	10
11	PD5, D13	PD5	7	12	PD4, D12	PD4	12
13	PD3, D11	PD3	5	14	PD2, D10	PD2	4
15	PD1, D9	PD1	3	16	PD0, D8	PD0	2
17	RESERVE	NC1	1	18	PE7, D7	PE7	120
19	PE6, D6	PE6	119	20	PE5, D5	PE5	118
21	PE4, D4	PE4	117	22	PE3, D3	PE3	116
23	PE2, D2	PE2	115	24	RESERVE	NC114	114
25	PE1, D1	PE1	113	26	RESERVE	NC112	112
27	PE0, D0	PE0	111	28	TDI	TDI	110
29	TRSTn	TRSTn	109	30	TMS	TMS	108
31	TCK	TCK	107	32	TDO	TDO	106
33	PG4, CS0n	PG4	105	34	PG3, CS1n	PG3	104
35	PG2, CS2n	CS2n	103	36	PG1, CS3n, IRQ7n	PG1	102
37	PG0	PG0	101	38	P70, TMRI01, TMCI01, CS4n	P70	10
39	P71, CS5n	P71	99	40	P72, TMO0, CS6n	P72	98
41	P73, TMO1, CS7n	P73	97	42	P74, MRESn	P74	96
43	RESERVE	NC95	95	44	P36	P36	94
45	P35, SCK1, IRQ5n	P35	93	46	P34, RxD1	P34	92
47	P33, TxD1	P33	91	48	P32, CSK0, IRQ4n	P32	90
49	P32, RxD0	DRXD	89	50	P30, TxD0	DTXD	88
51	PF0, BREQn, IRQ2n	PF0	87	52	PF1, BACKn	PF1	86
53	PF2, WAITn	PF2	85	54	RESERVE	NC84	84
55	PF3, LWRn, ADTRGn, IRQ3n	PF3	83	56	RESERVE	NC82	82
57	PF4, HWRn	PF4	81	58	PF5, RDn	PF5	80
59	PF6, Asn	PF6	79	60	PF7,	PF7	78

6.2. HEADER J2

J2							
Pin No	**Function**	**EDK Symbol**	**Device pin**	**Pin No**	**Function**	**EDK Symbol**	**Device pin**
1	PC6, A6	PC6	18	2	PC7, A7	PC7	19
3	PB0, A8	PB0	20	4	PB1, A9	PB1	21
5	RESERVE	NC22	22	6	PB2, A10	PB2	23
7	RESERVE	NC24	24	8	PB3, A11	PB3	25
9	PB4, A12	PB4	26	10	PB5, A13	PB5	27
11	PB6, A14	PB6	28	12	PB7, A15	PB7	29
13	PA0, A16	PA0	30	14	PA1, A17, TxD2	PTXD	31
15	PA2, A18, RxD2	PRXD	32	16	PA3, A19, SCK2, SUSPND	PSCK	33
17	RESERVE	NC34	34	18	P10, TIOCA0, A20, VM	P10	35
19	P11, TIOCB0, A21, VP	P11	36	20	P12, TIOCC0, TCLKA, A22, RCV	P12	37
21	P13, TIOCD0, TCLKB, A23, VPO	P13	38	22	P14, TIOCA1, IRQ0n	DCTS	39
23	P15, TOCB1, TCLKC, FSE0	ULED1	40	24	P16, TIOCA2, IRQ1n	ULED2	41
25	P17, TIOCB2, TCLKD, OEn	DRTS	42	26	AVSS	CON_AVSS	43
27	P97, AN15, DA1	P97	44	28	P96, AN14, DA0	P96	45
29	P43, AN3	P43	46	30	P42, AN2	P42	47
31	P41, AN1	P41	48	32	P40, AN0	P40	49
33	Vref	CON_VREF	50	34	AVCC	CON_AVCC	51
35	RESERVE	NC52	52	36	USPND	USPND	53
37	RESERVE	NC54	54	38	VBUS	VBUS	55
39	UBPMn	UBPMn	56	40	DrVCC	UVCC	57
41	USD+	USD_POS	58	42	USD-	USD_NEG	59
43	DrVSS	GROUND	60	44	VSS	GROUND	61
45	PLLVSS	NC62	62	46	PLLCAP	NC63	63
47	PLLVCC	NC64	64	48	XTAL48	CON_XTAL48	65
49	EXTAL48	CON_EXTAL48	66	50	MD0	MD0	67
51	MD1	MD1	68	52	FWE	FW	69
53	NMI	NMIn	70	54	STBYn	STBYn	71
55	RESn	RESn	72	56	VSS	GROUND	73
57	XTAL	CON_XTAL	74	58	VCC	UVCC	75
59	EXTAL	CON_EXTAL	76	60	MD2	MD2	77

7. CODE DEVELOPMENT

7.1. HMON

7.1.1. MODE SUPPORT

The HMON library is built to support modes 4, 5, 6, and 7. The library is also built with the number of parameter registers set to 3 (Default = 2). This provides more efficient code for Advanced Mode. This option is selectable in the Toolchain options for the CPU, and can be selectable in the standard projects generator (Not the EDK project generator as this is already set).

7.1.2. BREAKPOINT SUPPORT

H8S/2215 has no break controller, therefore no breakpoints can be set in FLASH. Code located in RAM may have multiple breakpoints, and is limited only by the size of the On-Chip RAM.

7.1.2.1. CODE LOCATED IN ROM

The H8S/2215 does not have a PC break controller. Breakpoints are limited to compiled in Trap instructions. HEW Will not allow breakpoints to be set in the ROM/FLASH area.

7.1.2.2. CODE LOCATED IN RAM

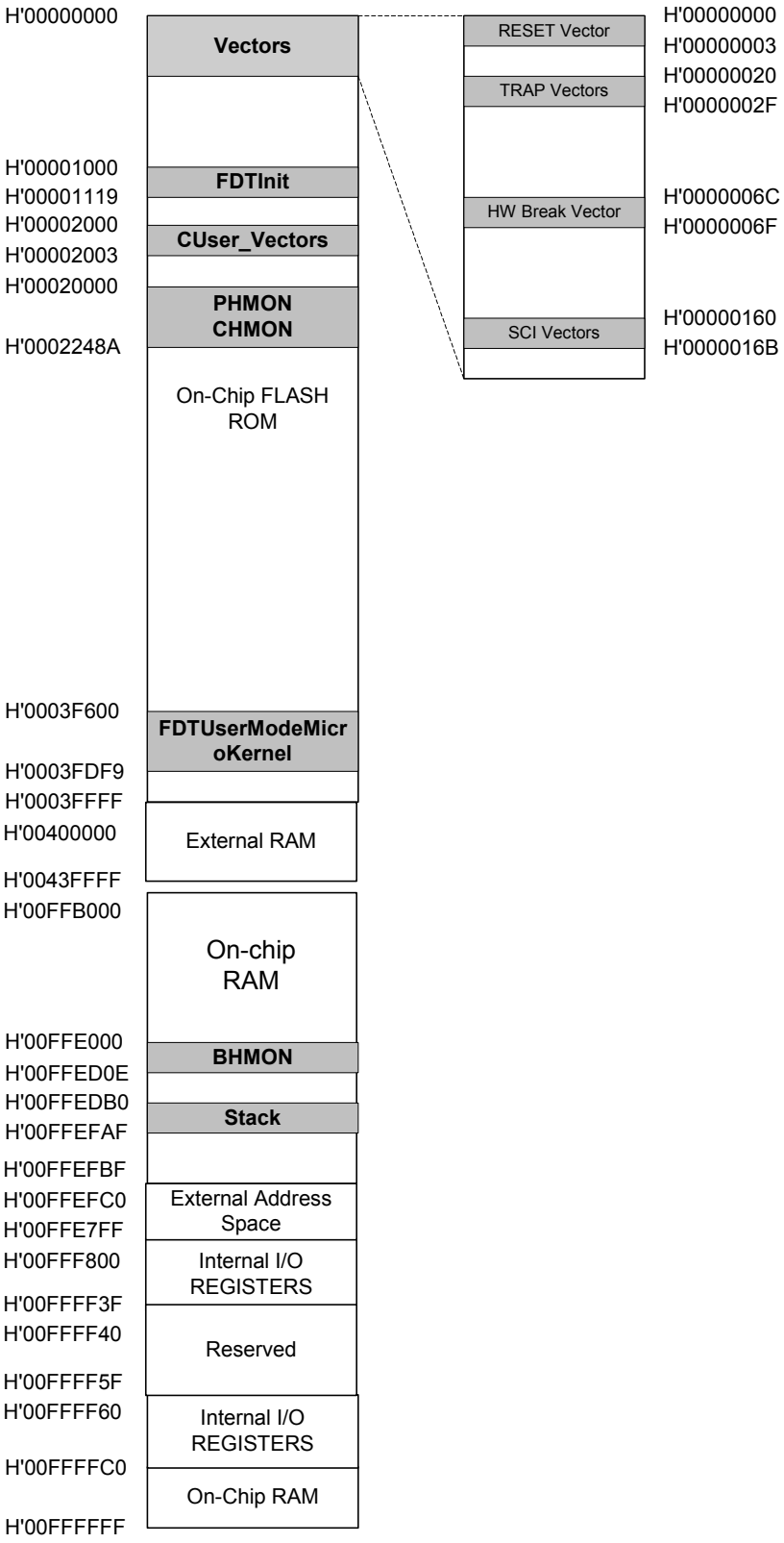
Double clicking in the breakpoint column in the code sets the breakpoint. Breakpoints will remain unless they are double clicked to remove them.

7.1.3. HMON CODE SIZE

HMON is built along with the debug code. Certain elements of the HMON code must remain at a fixed locationin memory. The following table details the HMON components and their size and location in memory. For more information, refer to the map file when building code.

Section	Description	Start Location	Size (H'bytes)
RESET_VECTOR	HMON Reset Vector (Vector 0) Required for Startup of HMON	H' 000000000	4
TRAP_VECTORS	Trap Vectors (Vector 8, 9, 10, 11) Required by HMON to create Trap Breakpoints in RAM	H' 00000020	10
HW_BREAK_VECTORS	HMON Break Controller (Vector 27) Required by HMON to create Breakpoints in ROM	H' 0000006C	4
SCI_VECTORS	HMON Serial Port Vectors (Vector 80, 81, 82, 83) Used by HMON when EDK is configured to connect to the default serial port.	H' 00000160	C
PHMON	HMON Code	H' 00020000	248A
CHMON	HMON Constant Data	H' 0002248A	148
BHMON	HMON Uninitialised data	H' 00FFE000	20F
FDTInit	FDT User Mode Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H' 00001000	11A
FDTUserModeMicroKernel	FDT User Mode Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H' 0003F600	7FA
CUser_Vectors	Pointer used by HMON to point to the start of user code. This is at a fixed location and must not be moved for the Reset CPU, and Go Reset commands to function.	H' 00002000	4

7.1.4. MEMORY MAP



7.1.5. BAUD RATE SETTING

HMON has initially set to connect at 115200Baud. Should the user wish to change this, the value for the BRR in HMONserialconfiguser.c will need to be changed and the project re-built. Please refer to the HMON User Manual for further information.

7.1.6. INTERRUPT MASK SECTIONS

HMON has an interrupt priority of 6. The serial port has an interrupt priority of 6. Modules using interrupts should be set to lower than this value, so that serial communications and debugging capability is maintained.

7.2. ADDITIONAL INFORMATION

For details on how to use Hitachi Embedded Workshop (HEW), with HMON, `refer to the HEW manual available on the CD or from the web site.

For information about the series microcontrollers refer to the *Series Hardware Manual*

For information about the assembly language, refer to the *Series Programming Manual*

Further information available for this product can be found on the HMSE web site at:

http://www.hmse.com/products/support.htm

General information on Hitachi Microcontrollers can be found at the following URLs.

Global: http://www.hitachisemiconductor.com

Europe: http://www.hmse.com