Z16F2800100ZCOG

ZNEO™ Series of Microcontrollers Development Kit

User Manual

UM020203-0606

ZiLOG Worldwide Headquarters • 532 Race Street • San Jose, CA 95126
Telephone: 408.558.8500 • Fax: 408.558.8300 • www.ZiLOG.com

ZNEO™ Development Kit
User Manual

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters
532 Race Street
San Jose, CA 95126
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

Document Disclaimer

UM020203-0606

Revision History

Each instance in Table 1 reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

Table 1. Revision History of this Document

Date	Revision Level	Section	Description	Page #
June 2006	3	ZNEO™ Series Development Board	Added note on the ZNEO development board 16-bit bus and programming external Flash memory.	5
May 2006	2	Schematics	Updated all schematics.	17
Jan. 2006	1		Original Issue	

Safeguards

The following precautions must be observed when working with the devices described in this document.

Caution: Always use a grounding strap to prevent damage resulting from electrostatic discharge (ESD).

Table of Contents

Revision History iii
Safeguards iv
Table of Contents v
List of Figures. vii
Introduction 1
Installation 3
ZNEO™ Series
Development Board 5
Introduction 5
Features 6
Development Kit Block Diagram 6
ZNEO MEMORY LAYOUT 8
MCU 11
UART with IrDA Endec 13
Switches and LEDs 13
Jumper Settings 14
External Interface Headers JP1, JP2, and JP4 15
Schematic 17

List of Figures

Figure 1. ZNEO™ Series Development Board 5
Figure 2. ZNEO Series Development Kit Block Diagram 7
Figure 3. ZNEO Physical Memory Layout 9

Introduction

The ZNEO™ Series MCU is part of the line of ZiLOG microcontroller products.

The ZNEO™ Series MCU Development Kit (Z16F2800100ZCOG) enables users to become familiar with the hardware and software tools available with this product. This kit consists of the 128KB version of the ZNEO™ Development board that supports and presents the features of the ZNEO™ Series. This kit allows users to begin writing application software and contains all supporting documents.

This manual acquaints users with the ZNEO™ Series MCU Development Kit, and gives instructions on setting up and using the tools to start building designs and applications.

Installation

Follow the directions in the Quick Start Guide for software installation and setup of the ZNEO™ Series Development kit.

ZNEO™ Series Development Board

Introduction

The ZNEO™ Series Development board is a development and prototyping board for the ZNEO™ Series MCU. The board provides customers with a tool to evaluate features of ZNEO™ Series MCU, and to start developing an application before building the hardware.

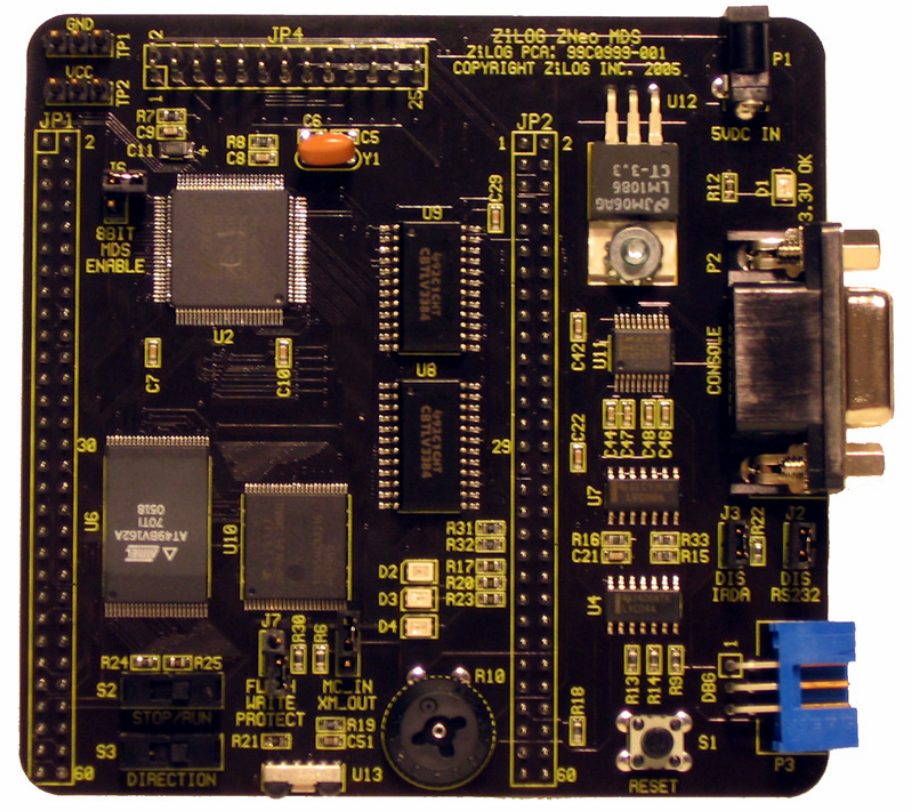


Figure 1. ZNEO™ Series Development Board

Features

- ZNEO™ MCU (100-pin LQFP package)
- 1M x 16 External Flash memory
- 256K x 16 External RAM
- 3 LEDs
- RS-232 interface
- On-Chip Debugger interface
- IrDA transceiver
- Electrical and mechanical compatibility with ZiLOG MDS architecture
- One RESET pushbutton (S1)
- Two SPST switches (S2, STOP/RUN and S3, DIRECTION)
- 5 VDC power connector
- 20 MHz Ceramic Oscillator (Y1)
- Header for ADC input
- External interface connectors JP1, JP2, and JP4
- 2.7–3.6 V operating voltage with 5V-tolerant inputs

Development Kit Block Diagram

A block diagram of the ZNEO Series Development Kit is provided in Figure 2.

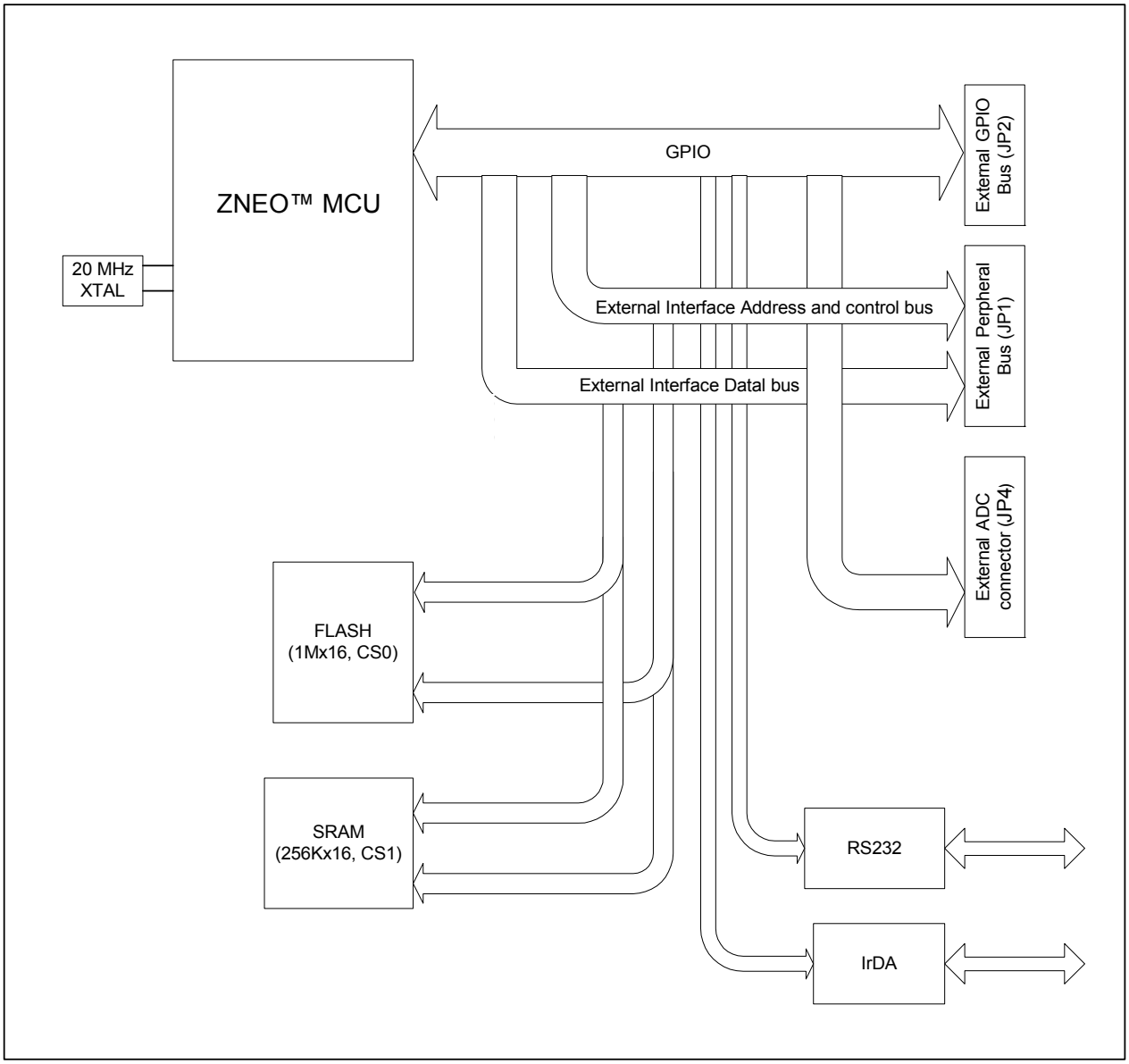


Figure 2. ZNEO Series Development Kit Block Diagram

ZNEO MEMORY LAYOUT

The ZNEO CPU has a unique memory architecture with a unified 24-bit physical address space, which is partitioned into several distinct memory areas. In terms of physical memory spaces, the overall address space can include the following:

- Internal nonvolatile memory
- Internal RAM
- Internal I/O memory and special-function registers (SFRs)
- External memory and memory mapped peripherals.

The internal spaces listed above are always present in ZNEO devices, while the external space is optional. Every address space is defined as a specific range of addresses located at a given place in the framework of the unified 24-bit address space, and the address ranges of the different spaces do not overlap. To promote code efficiency, the ZNEO CPU supports shorter 16-bit addressing for the memory located in the address ranges 00_0000H-00_7FFFH and FF_8000H-FF_FFFFH. Figure 3 shows the physical layout of memory spaces available in the ZNEO architecture.

Note: The external Flash memory on the ZNEO development kit board has a 16-bit bus. All writes to Flash memory must be 16 bits at even addresses only. Attempts to write 1 byte will result in the byte being replicated on both the upper and lower bytes of the 16-bit bus.

Memory	Address	Chip Selects
Internal I/O Memory & SFRs	FF_FFFFH FF_E000H	
External Memory Mapped Peripherals (optional)	FF_DFFFH FF_C800H	CS3 – CS5
External Memory at CS2 (optional)	FF_C7FFH FF_C000H	CS2
Internal RAM	FF_BFFFH FF_8000H	
External Memory at CS2 (optional)	F0_0000H	CS2
External Memory at CS1 (optional)	80_0000H	CS1
External Memory at CS0 (optional)	02_0000H	CS0
Internal Nonvolatile Memory	01_FFFFH 00_0000H	

Figure 3. ZNEO Physical Memory Layout

Each of the internal memory spaces has a distinct purpose. Internal nonvolatile memory typically contains executable program code and constant data. ZNEO-CPU-based devices have internal nonvolatile memory starting at address 00_0000H. For example, a device equipped with 128K of Flash has internal nonvolatile memory starting at address 00_0000H and ending at address 01_FFFFH.

Internal RAM typically contains nonconstant data and the stack. Executable program code can also reside in internal RAM, if desired. ZNEO-CPU-based devices have internal RAM ending at address FF_BFFFH, while the beginning address (and hence the total extent of this space) is device dependent. For example, a device equipped with 4K of RAM has internal RAM starting at address FF_B000H and ending at address FF_BFFFH. Because it is intended to be accessed using 16-bit addressing, the lowest possible starting address for internal RAM on any device is FF_8000H.

ZNEO-CPU-based devices support 8K of internal I/O memory located at addresses FF_E000H-FF_FFFFH. This memory contains CPU control registers and other SFRs, onchip peripherals, and memory-mapped I/O ports.

Finally, ZNEO-CPU-based devices also provide an external interface that allows seamless connection to external memory and/or peripherals. External memory can be nonvolatile memory such as Flash, or RAM, or both. External nonvolatile memory can be used to store program code and, at the user's option, constant data, while external RAM is available primarily as a location for nonconstant data.

The external interface supports multiple chip select signals (CSx), which are asserted by the CPU when an access to external memory is requested. These signals can be used to access distinct ranges and devices in external memory. The boundaries between memory ranges selected by the chip select signals are at fixed addresses, and, in some cases, the ranges covered by chip selects might overlap. For example, there might be some addresses in the range of both the CS0 and CS1 signals. In this case, the

ZNEO CPU uses a chip select priority scheme. It asserts only the single chip select with the highest priority among those that contain the address to be accessed, with CS0 having the lowest priority and CS5 the highest. Also, the chip selects can be individually enabled or disabled. On-chip memory always has the priority over external memory. CS0 starts at address 00_0000H, and CS1 starts at address 80_0000H. CS2 to CS5 start at addresses F0_0000H and beyond. Refer to the *ZNEO CPU User Manual* and the individual device product specification for more information.

MCU

The ZNEO Z16F Series Flash microcontrollers are based on ZiLOG's advanced ZNEO 16-bit CPU core. The ZNEO Z16F Series MCU family of devices sets a new standard of performance and efficiency with a 24-bit address bus and 16-bit data bus.

The ZNEO Z16F Series External Interface allows seamless connection to external memory and peripherals. A 24-bit address bus and selectable 8-bit or 16-bit data bus allows parallel access up to 16 MB.

The Development board contains circuitry to support and present all the features of the ZNEO™ Series. The main features of the ZNEO Series are:

- 20 MHz ZiLOG ZNEO CPU Core
- Up to 128 KB internal Flash program memory with 16-bit access and in-circuit programming capability
- Up to 4 KB internal RAM with 16-bit access
- External Interface allows seamless connection to external data memory and peripherals with:
  - 6 chip selects with programmable Wait states
  - 24-bit address bus supports up to 16 MB

  - Selectable 8-bit or 16-bit data bus widths
  - Programmable Chip Select signal polarity
  - ISA-compatible mode
- Up to twelve channels 10-bit analog-to-digital converter (ADC)
- Operational Amplifier
- Analog Comparator
- 4-channel DMA controller supports internal or external DMA requests
- Two full-duplex 9-bit UARTS with support for LIN and IrDA
- Internal Precision Oscillator
- I^2C master-slave controller
- Enhanced Serial Peripheral Interface (ESPI) controller
- 12-bit PWM module with three complementary pairs or six independent PWM outputs with dead-band generation and fault trip input
- Three standard 16-bit timers with capture, compare, and PWM capability
- Watch-Dog Timer (WDT) with internal RC oscillator
- Up to 76 I/O pins
- Up to 24 interrupts with programmable priority
- Single-pin on-chip debugger
- Power-On Reset (POR)
- Voltage Brown-Out Protection (VBO)
- 2.7 V to 3.6 V operating voltage with 5 V-tolerant inputs
- 0°C to +70°C standard temperature, -40°C to +105°C extended temperature, and -40°C to +125°C automotive operating ranges

For further information on the ZNEO™ family of devices, consult the product specification, P/N PS0220, available for download from www.zilog.com.

UART with IrDA Endec

The ZNEO Series contains a fully-functional, high-performance UART with Infrared Encoder/Decoder (ENDEC). The Infrared Endec is integrated with an on-chip UART (component U13) allowing easy communication between the ZNEO Series and IrDA transceivers. Infrared communication provides secure, reliable, low-cost, point-to-point communication between PCs, PDAs, cell phones, printers and other infrared enabled devices.

Switches and LEDs

The ZNEO development board contains the following LEDs and switches:

- Green LED D1, which when illuminated indicates the presence of 3.3VDC on the board's VCC_3V power bus
- Red LED D2, connected to chip port PA0_T0IN
- Yellow LED D3, connected to chip port PA1_T0OUT
- Green LED D4, connected to chip port PA2_DE0
- Reset switch S1, connected to chip port $\overline{\text{RESET}}$
- SPST switch S2, connected to chip port PA7_SDA
- SPST switch S3, connected to chip port PC0_T1IN

Potentiometer R10 is reserved for future use.

Jumper Settings

Table 1 provides information on the shunt status, functions, and defaults of jumpers on the ZNEO Series development board.

Table 1. ZNEO Jumper Settings

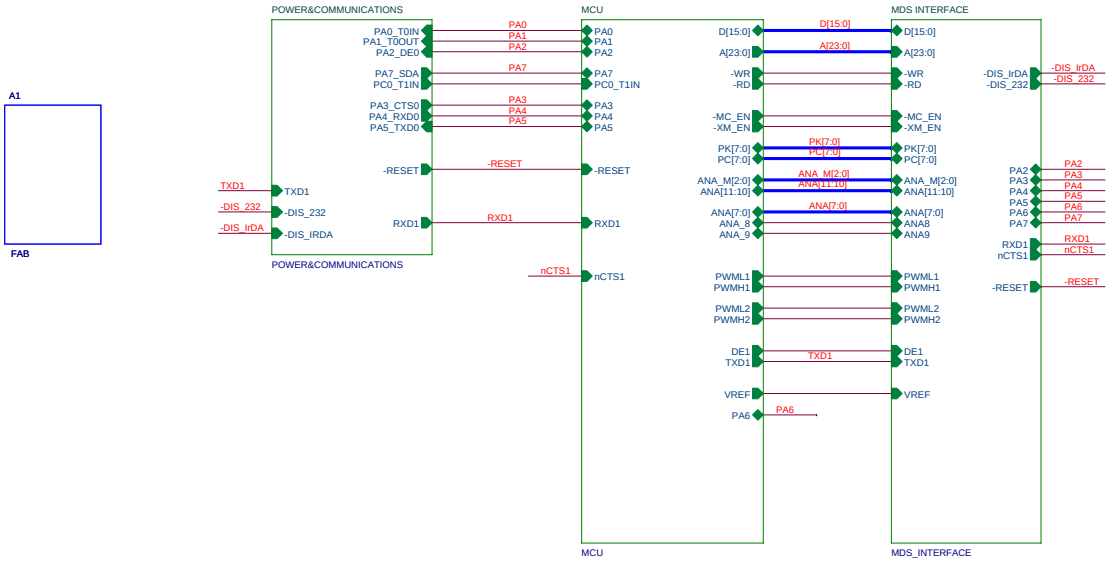
Jumper	Status	Function	Default
J1	OUT (not installed)	Enables ZNEO MCU access to external 16-bit memory bus on development board	X
J1	IN	Disables 16-bit external memory bus and makes ZNEO MCU analog ports available through connector JP4. Refer to schematic for JP4 pinouts.	
J2*	OUT	RS-232 interface enabled	X
J2	IN	RS-232 interface disabled	
J3*	OUT	IrDA interface enabled	
J3	IN	IrDA interface disabled	X
J6	OUT	8-bit Modular Development System interface disabled	X
J6	IN	8-bit Modular Development System interface enabled	
J7	OUT	External Flash Write Protect disabled	X
J7	IN	External Flash Write Protect enabled	
Note: * These jumpers must not be OUT at the same time			

External Interface Headers JP1, JP2, and JP4

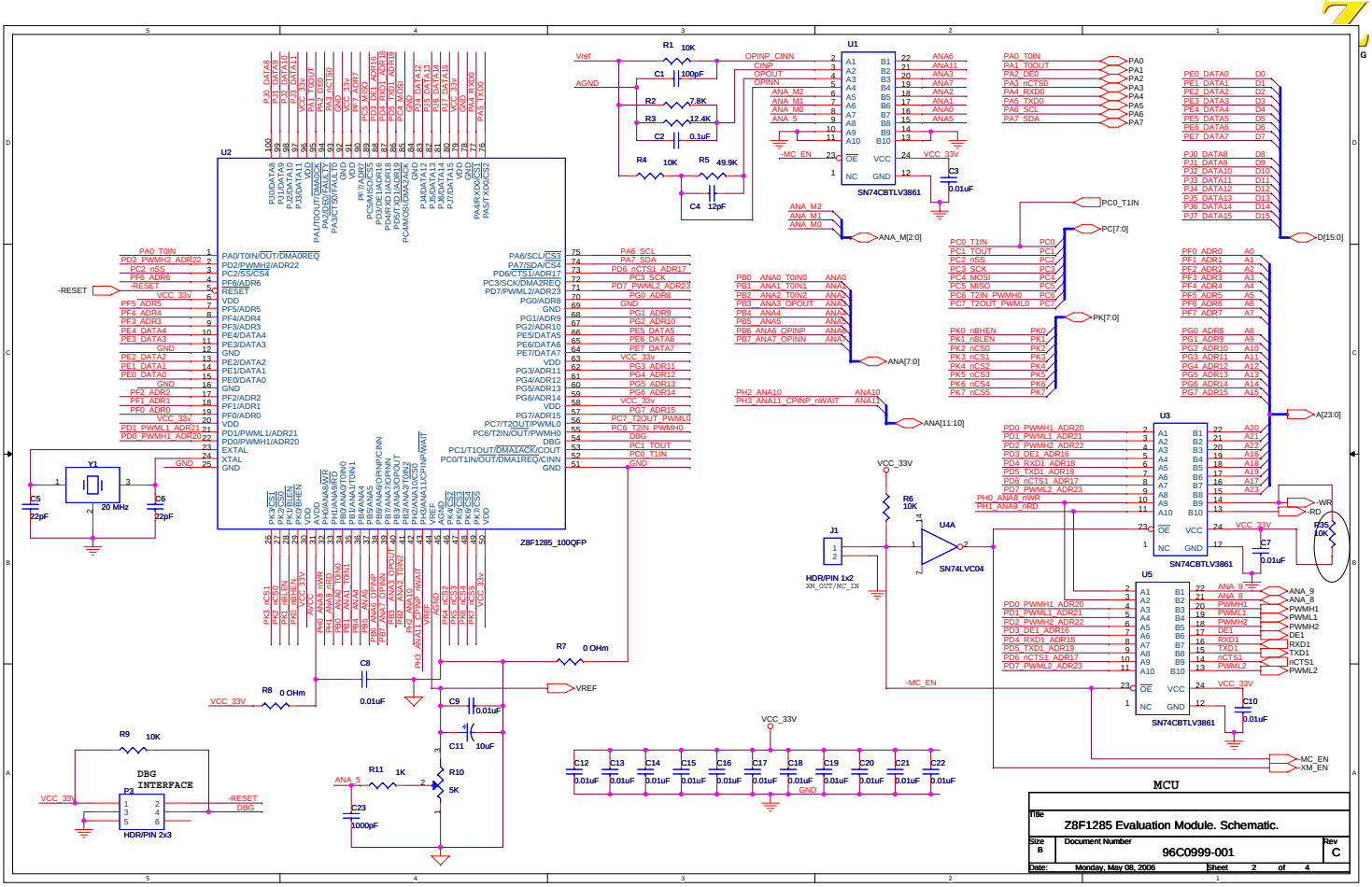
External interface headers JP1, JP2, and JP4 are shown in the schematic on page 21.

Schematic

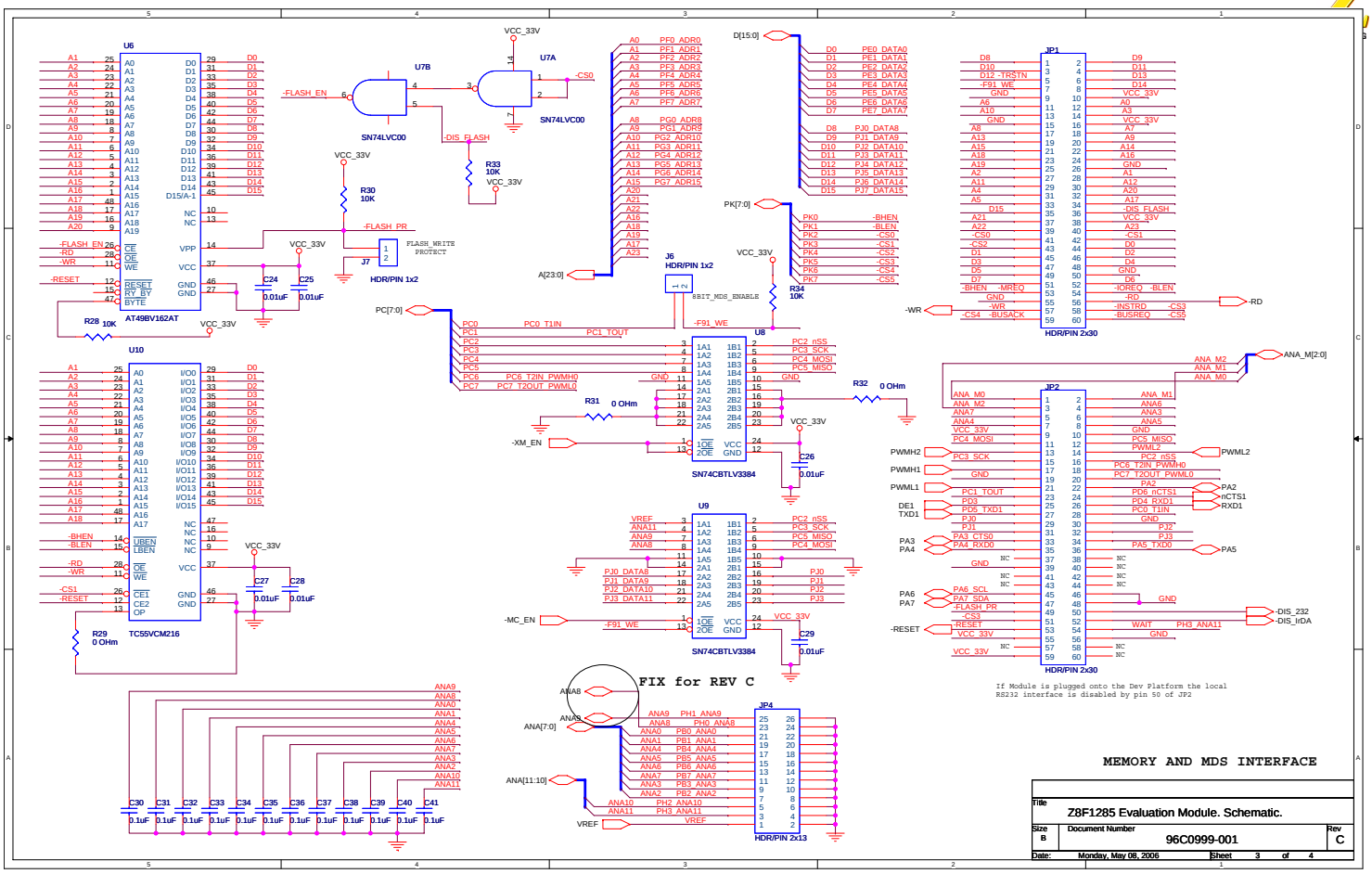
This section includes schematics for the ZNEO™ Series Development Board.



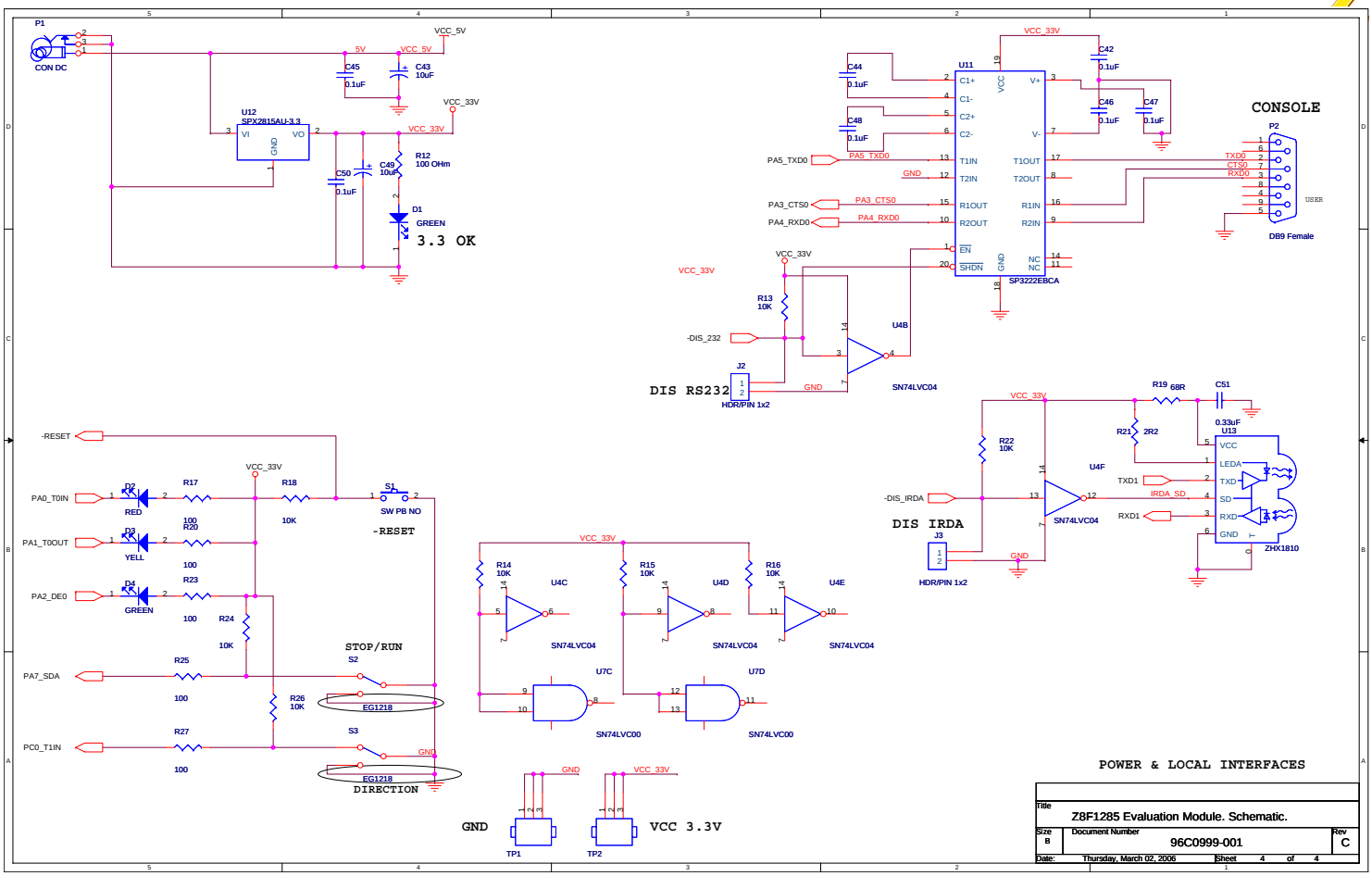
Schematic, ZNEO™ Series MCU Development Board, Page 1 of 4



Schematic, ZNEO™ Series MCU Development Board, Page 2 of 4



Schematic, ZNEO™ Series MCU Development Board, Page 3 of 4



Schematic, ZNEO™ Series MCU Development Board, Page 4 of 4