XC-2 Hardware Manual

(VERSION 1.4)

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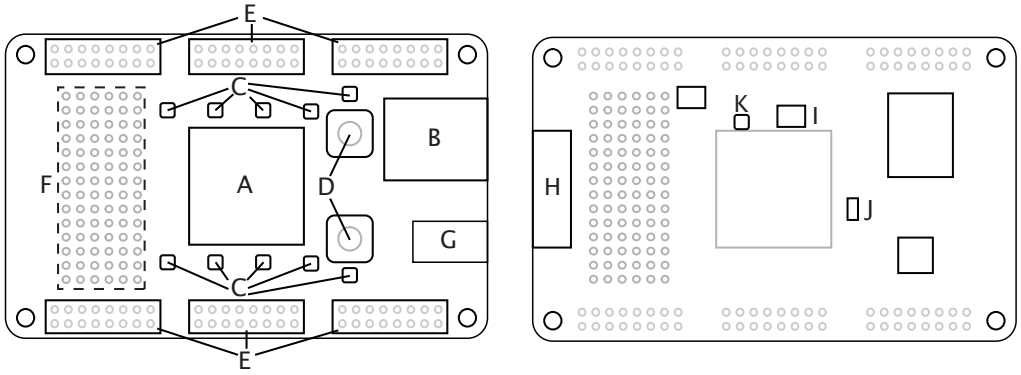
Authors:

XMOS LTD.

1 Introduction

The XC-2 is a Event-Driven Processor development card intended for designing Ethernet-based products such as audio/video bridging applications and industrial control systems. It comprises a single XS1-G4 device, 10/100-BASE-T Ethernet PHY, 4Mbits SPI flash memory, 10 LEDs and two press-buttons. I/O expansion areas are provided for connecting additional components, and an XSYS connector can be used to interface the card with a PC. The diagram below shows the layout of these components on the card.



A XS1-G4 Device

B RJ45 Connector

C User LEDs

D Push-Button Switches

E I/O Expansion Areas

F Prototyping Area

G Power Connector

H XSYS Connector

I SPI Flash Memory

J 10/100 BASE-T Ethernet PHY

K Power Regulator

L 25MHz Crystal Oscillator

M PLL Status LED

The XC-2 Development Kit also includes a 5V power supply and XTAG connector for booting the device from a PC. The card is fitted with four plastic feet, which can be removed to provide access to mounting holes for product integration.

The rest of this document provide a detailed description of these components.

2 XS1-G4 Device [A]

The XC-2 is based on a single XS1-G4 device in a 512BGA package. The XS1-G4 consists of four XCores, each comprising an event-driven multi-threaded processor with tightly integrated general purpose I/O pins and 64 KBytes of on-chip RAM. The pins are brought out of the package and connected to the card's components as follows:

Processor 0

- Two red and two green LEDs
- Two push-button switches
- An XSYS connector
- An SPI interface to flash memory
- 12 I/O pins to the prototyping area

Processor 1

- Two red LEDs
- Two 16-way I/O expansion headers (24 I/O bits)

Processor 2

- One 10/100-BASE-T Ethernet PHY
- Two red LEDs
- Two 16-way I/O expansion headers (24 I/O bits)

Processor 3

- Two red LEDs
- Two 16-way I/O expansion headers (24 I/O bits)

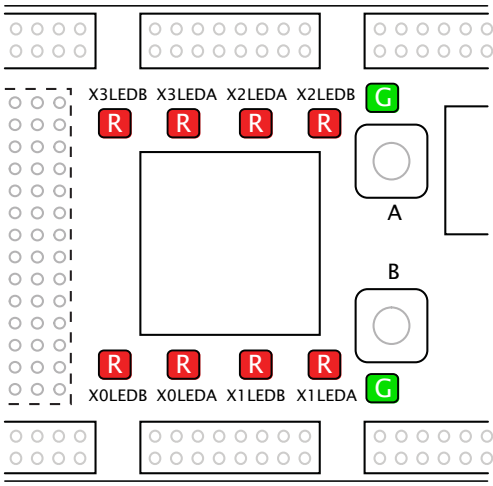
The processors have ports that are directly connected to the I/O pins. Examples of how to write software that interfaces over these ports with the XC-2 components is provided in a separate tutorial [1].

3 RJ45 Connector [B] and Ethernet PHY [J]

The RJ45 connector is wired to the 10/100-BASE-T Ethernet PHY. The MII and MAC level protocols are implemented in software.

4 User LEDs [C]

The XC-2 provides 10 user LEDs that can be driven by software. The layout of these LEDs is shown below.

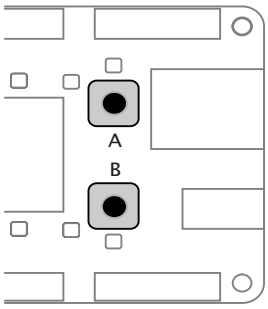


There are two green LEDs next to the two push-button switches and four red LEDs on both sides of the XS1-G4. Each LED is connected to a different pin, all of which are mapped to ports as described in the table below.

Pin	Port	Processor (*n*)			
	1b	0	1	2	3
X*n*D12	P1E0	PORT_BUTTON_LED_0			
X*n*D13	P1F0	PORT_BUTTON_LED_1			
X*n*D24	P1I0	PORT_LED_0_0	PORT_LED_1_0	PORT_LED_2_0	PORT_LED_3_0
X*n*D25	P1J0	PORT_LED_0_1	PORT_LED_1_1	PORT_LED_2_1	PORT_LED_3_1

5 Push-Button Switches [D]

The XC-2 provides two push-button switches whose states can be sampled at any time by software. The layout of these switches is shown below.



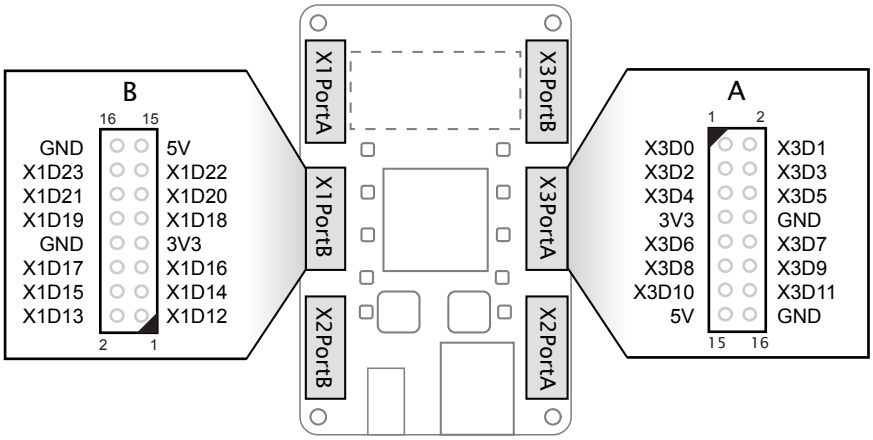
The switches are connected to two pins, which are mapped to ports as described in the table below.

Pin	Port		Processor
	4b	8b	0
X0D14	P4C0	P8B0	PORT_BUTTON_A
X0D16	P4D0	P8B2	PORT_BUTTON_B

Each pin can be configured either as a 4-bit port or an 8-bit port. The configuration is determined by the set of port initialisers used in the software [2].

6 I/O Expansion Areas [E]

The I/O pins of three of the processors are brought out to expansion areas on both sides of the card. These areas have 0.1” pitch through-plated holes and are suitable for use with IDC headers. To provide maximum flexibility, no headers are fitted, allowing the most suitable type to be selected depending on the design. The routing of the I/O and power pins in the expansion headers is shown below.



Each expansion header provides a bank of 12 I/O pins, which are mapped to the ports as described in the table on the next page.

Pin	Port				Processor (*n*)		
	1b	4b	8b	16b	1	2	3
X*n*D0	P1A0				Header 1/A	Header 2/A	Header 3/A
X*n*D1	P1B0						
X*n*D2		P4A0	P8A0	P16A0			
X*n*D3		P4A1	P8A1	P16A1			
X*n*D4		P4B0	P8A2	P16A2			
X*n*D5		P4B1	P8A3	P16A3			
X*n*D6		P4B2	P8A4	P16A4			
X*n*D7		P4B3	P8A5	P16A5			
X*n*D8		P4A2	P8A6	P16A6			
X*n*D9		P4A3	P8A7	P16A7			
X*n*D10	P1C0						
X*n*D11	P1D0						
X*n*D12	P1E0				Header 1/B	Header 2/B	Header 3/B
X*n*D13	P1F0						
X*n*D14		P4C0	P8B0	P16A8			
X*n*D15		P4C1	P8B1	P16A9			
X*n*D16		P4D0	P8B2	P16A10			
X*n*D17		P4D1	P8B3	P16A11			
X*n*D18		P4D2	P8B4	P16A12			
X*n*D19		P4D3	P8B5	P16A13			
X*n*D20		P4C2	P8B6	P16A14			
X*n*D21		P4C3	P8B7	P16A15			
X*n*D22	P1G0						
X*n*D23	P1H0						

Eight pins from each bank can be configured as either two 4-bit ports or a single 8-bit port. The A and B expansion headers can alternatively be used together as a single 16-bit port.

6.1 XMOS Link Configuration

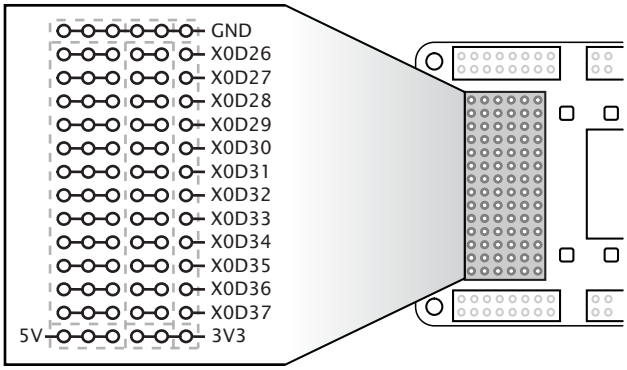
Some of the I/O pins on the expansion header can be configured as XMOS Links. The mapping of XMOS Links to the headers is shown in the table below.

Header 1/A			Header 2/A			Header 3/A		
Pin	XMOS Link 1		Pin	XMOS Link 2		Pin	XMOS Link 3	
	2 bit	5 bit		2 bit	5 bit		2 bit	5 bit
X1D0			X2D0			X3D0		
X1D1		XLA4 I	X2D1		XLA4 O	X3D1		XLA4 I
X1D2		XLA3 I	X2D2		XLA3 O	X3D2		XLA3 I
X1D3		XLA2 I	X2D3		XLA2 O	X3D3		XLA2 I
X1D4	XLA1in	XLA1 I	X2D4	XLA1 O	XLA1 O	X3D4	XLA1 I	XLA1 I
X1D5	XLA0in	XLA0 I	X2D5	XLA0 O	XLA0 O	X3D5	XLA0 I	XLA0 I
X1D6	XLA0out	XLA0 O	X2D6	XLA0 I	XLA0 I	X3D6	XLA0 O	XLA0 O
X1D7	XLA1out	XLA1 O	X2D7	XLA1 I	XLA1 I	X3D7	XLA1 O	XLA1 O
X1D8		XLA2 O	X2D8		XLA2 I	X3D8		XLA2 O
X1D9		XLA3 O	X2D9		XLA3 I	X3D9		XLA3 O
X1D10		XLA4 O	X2D10		XLA4 I	X3D10		XLA4 O
X1D11			X2D11			X3D11		

Header 1/B			Header 2/B			Header 3/B		
Pin	XMOS Link 1		Pin	XMOS Link 2		Pin	XMOS Link 3	
	2 bit	5 bit		2 bit	5 bit		2 bit	5 bit
X1D12			X2D12			X3D12		
X1D13		XLB4 I	X2D13		XLB4 O	X3D13		XLB4 I
X1D14		XLB3 I	X2D14		XLB3 O	X3D14		XLB3 I
X1D15		XLB2 I	X2D15		XLB2 O	X3D15		XLB2 I
X1D16	XLB1in	XLB1 I	X2D16	XLB1 O	XLB1 O	X3D16	XLB1 I	XLB1 I
X1D17	XLB0in	XLB0 I	X2D17	XLB0 O	XLB0 O	X3D17	XLB0 I	XLB0 I
X1D18	XLB0out	XLB0 O	X2D18	XLB0 I	XLB0 I	X3D18	XLB0 O	XLB0 O
X1D19	XLB1out	XLB1 O	X2D19	XLB1 I	XLB1 I	X3D19	XLB1 O	XLB1 O
X1D20		XLB2 O	X2D20		XLB2 I	X3D20		XLB2 O
X1D21		XLB3 O	X2D21		XLB3 I	X3D21		XLB3 O
X1D22		XLB4 O	X2D22		XLB4 I	X3D22		XLB4 O
X1D23			X2D23			X3D23		

7 Prototyping Area [F]

The XC-2 provides a 0.1” pitch through-hole plated area for adding components to the card. The routing of I/O and power pins in the prototyping area is shown below.



The prototyping area provides a bank of 12 I/O pins, which are mapped to the ports as described in the table below.

Pin	Port			Processor
	1b	4b	8b	0
X0D26		P4E0	P8C0	Prototyping Area
X0D27		P4E1	P8C1	
X0D28		P4F0	P8C2	
X0D29		P4F1	P8C3	
X0D30		P4F2	P8C4	
X0D31		P4F3	P8C5	
X0D32		P4E2	P8C6	
X0D33		P4E3	P8C7	
X0D34	P1K0			
X0D35	P1L0			
X0D36	P1M0		P8D0	
X9D37	P1N0		P8D0	

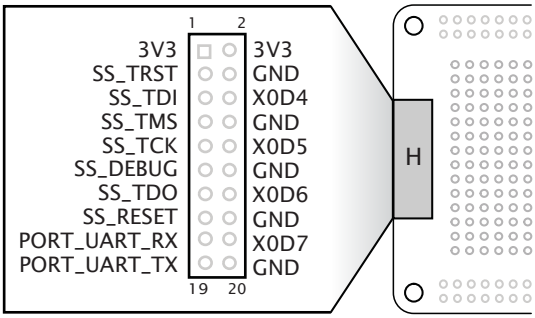
The prototyping area provides access to four 1-bit ports (1K, 1L, 1M and 1N) and either two 4-bit ports (4E and 4F) or one 8-bit port (8C).

8 Power Connector [D] and Regulator [K]

The XC-2 requires connection from an external 5V power supply. The voltage is converted by the on-board regulator to the 1V and 3V3 supplies used by the components.

9 XSYS Connector [H]

The XC-2 includes an XSYS connector, which can be used to boot and debug code on all of the XS1-G4's processors. The XSYS connector provides pins for JTAG control, system reset, processor debug, two UART links and one XMOS Link. The routing of these I/O pins along with the power pins is shown below.



The XMOS XTAG connector converts between XSYS and USB 2.0, allowing the XC-2 to be connected to most PCs. On power on, the XS1-G4 boots from the on-board flash memory. The XS1-G4 can then be put into JTAG mode by the PC, which then boots another program.

No UART hardware is provided. Instead, two UART pins are mapped to ports, as shown in the table below.

Pin	Port	Processor
	1b	0
X0D22	P1G0	PORT_UART_RX
X1D23	P1H0	PORT_UART_TX

If a UART is required, it can be implemented in software by sampling and driving these ports at the required rate. The XTAG performs a UART-to-USB conversion on these pins, presenting a virtual COM port to the PC that can be interfaced via a terminal emulator.

10 SPI Flash Memory [I]

The XC-2 provides 4Mbit of Serial Peripheral Interface (SPI) flash memory, which is interfaced by the four 1-bit connections described in the table below.

Pin	Port	Processor
	1b	0
X0D0	P1A0	PORT_SPI_MISO
X0D1	P1B0	PORT_SPI_SS
X0D10	P1C0	PORT_SPI_CLK
X0D11	P1D0	PORT_SPI_MOSI

The Development Tools include the XFLASH utility for programming compiled programs into the flash memory. XC-2 designs may also access the flash memory at run-time by interfacing with the above ports.

11 25MHz Crystal Oscillator [L]

The XS1-G4 is clocked at 25MHz by a crystal oscillator on the card. Each processor is clocked at 400MHz, the I/O ports at 100MHz, by an on-chip phase-locked loop (PLL).

12 PLL Status LED [M]

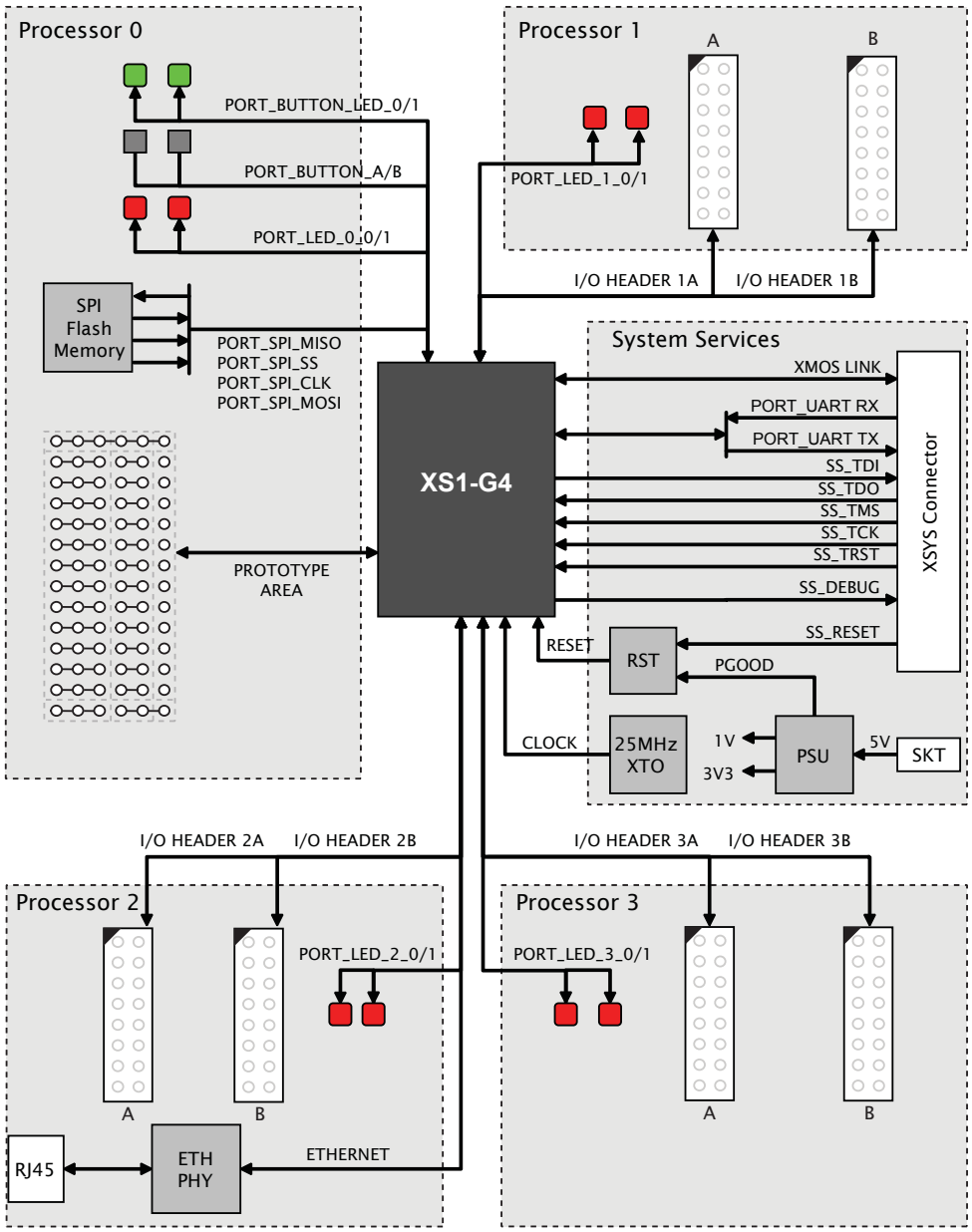
The PLL status LED remains off until the on-chip PLL has locked. Once the PLL clock is stable, the LED is illuminated red, indicating that the processor has power and the clock is running.

13 Dimensions

The XC-2 dimensions are 86 x 54mm. The mounting holes are 3mm in diameter.

14 XC-2 Block Diagram

The diagram below shows how the XC-2 components are connected to the XS1-G4.



14.1 I/O Port-to-Pin Mapping

The table below provides a full description of the port-to-pin mappings described throughout this document.

Pin	Port				Processor			
	1b	4b	8b	16b	0	1	2	3
X*n*D0	P1A0				PORT_SPI_MISO	Header 1/A	Header 2/A	Header 3/A
X*n*D1	P1B0				PORT_SPI_SS			
X*n*D2		P4A0	P8A0	P16A0				
X*n*D3		P4A1	P8A1	P16A1				
X*n*D4		P4B0	P8A2	P16A2	Host XMOS LINK			
X*n*D5		P4B1	P8A3	P16A3				
X*n*D6		P4B2	P8A4	P16A4				
X*n*D7		P4B3	P8A5	P16A5				
X*n*D8		P4A2	P8A6	P16A6				
X*n*D9		P4A3	P8A7	P16A7				
X*n*D10	P1C0				PORT_SPI_CLK			
X*n*D11	P1D0				PORT_SPI_MOSI			
X*n*D12	P1E0				PORT_BUTTON_LED_0	Header 1/B	Header 2/B	Header 3/B
X*n*D13	P1F0				PORT_BUTTON_LED_1			
X*n*D14		P4C0	P8B0	P16A8	PORT_BUTTON_A			
X*n*D15		P4C1	P8B1	P16A9				
X*n*D16		P4D0	P8B2	P16A10	PORT_BUTTON_B			
X*n*D17		P4D1	P8B3	P16A11				
X*n*D18		P4D2	P8B4	P16A12				
X*n*D19		P4D3	P8B5	P16A13				
X*n*D20		P4C2	P8B6	P16A14				
X*n*D21		P4C3	P8B7	P16A15				
X*n*D22	P1G0				PORT_UART_RX			
X*n*D23	P1H0				PORT_UART_TX			
X*n*D24	P1I0				PORT_LED_0_0	PORT_LED_1_0	PORT_LED_2_0	PORT_LED_3_0
X*n*D25	P1J0				PORT_LED_0_1	PORT_LED_1_1	PORT_LED_2_1	PORT_LED_3_1
X*n*D26		P4E0	P8C0	P16B0	Prototyping Area		PORT_ETH_RXD	
X*n*D27		P4E1	P8C1	P16B1				
X*n*D28		P4F0	P8C2	P16B2			PORT_ETH_TXD	
X*n*D29		P4F1	P8C3	P16B3				
X*n*D30		P4F2	P8C4	P16B4				
X*n*D31		P4F3	P8C5	P16B5				
X*n*D32		P4E2	P8C6	P16B6			PORT_ETH_RXD	
X*n*D33		P4E3	P8C7	P16B7				
X*n*D34	P1K0						PORT_ETH_TXCLK	
X*n*D35	P1L0						PORT_ETH_TXEN	
X*n*D36	P1M0		P8D0	P16B8			PORT_ETH_RXCLK	
X*n*D37	P1N0		P8D1	P16B9			PORT_ETH_RXDV	
X*n*D38	P1O0		P8D2	P16B10			PORT_ETH_RXER	
X*n*D39	P1P0		P8D3	P16B11			PORT_ETH_MDC	
X*n*D42			P8D6	P16B14			PORT_ETH_RST_N_MDIO	
X*n*D43			P8D7	P16B15				

15 XC-2 XN File

The XCore ports linked to the hardware features on the XC-2 are mapped to generic port identifiers as part of a platform specific XN file, which simplifies the process of porting a project between platforms.

The following table lists the defined identifiers for processors 0, 1, 2 and 3:

Processor	Port Location	Generic Identifier
0	XS1_PORT_1A	PORT_SPI_MISO
	XS1_PORT_1B	PORT_SPI_SS
	XS1_PORT_1C	PORT_SPI_CLK
	XS1_PORT_1D	PORT_SPI_MOSI
	XS1_PORT_1E	PORT_BUTTON_LED_0
	XS1_PORT_1F	PORT_BUTTON_LED_1
	XS1_PORT_1G	PORT_UART_RX
	XS1_PORT_1H	PORT_UART_TX
	XS1_PORT_1I	PORT_LED_0_0
	XS1_PORT_1J	PORT_LED_0_1
	XS1_PORT_4C	PORT_BUTTON_A
	XS1_PORT_4D	PORT_BUTTON_B
1	XS1_PORT_1I	PORT_LED_1_0
	XS1_PORT_1J	PORT_LED_1_1
2	XS1_PORT_1I	PORT_LED_2_0
	XS1_PORT_1J	PORT_LED_2_1
	XS1_PORT_1K	PORT_ETH_TXCLK
	XS1_PORT_1L	PORT_ETH_TXEN
	XS1_PORT_1M	PORT_ETH_RXCLK
	XS1_PORT_1N	PORT_ETH_RXDV
	XS1_PORT_1O	PORT_ETH_RXER
	XS1_PORT_1P	PORT_ETH_MDC
	XS1_PORT_4E	PORT_ETH_RXD
	XS1_PORT_4F	PORT_ETH_TXD
	XS1_PORT_8D	PORT_ETH_RST_N_MDIO
3	XS1_PORT_1I	PORT_LED_3_0
	XS1_PORT_1J	PORT_LED_3_1

16 Related Documents

The following documents provide more information on designing with the XC-2:

- *XC-2 Ethernet Kit Tutorial* [1]: provides an introduction to programming software on the XC-2 using the XC language.
- *XCore XS1 Architecture Tutorial* [3]: provides an overview of the XS1 instruction set architecture.

The most up-to-date information on the XC-2, including board schematics and product datasheets, is available from:

- `http://www.xmos.com/xc2/`

References

[1] Douglas Watt. XC-2 Ethernet Kit Tutorial. Website, 2009. http://www.xmos.com/published/xc2tut.

[2] Douglas Watt. Programming XC on XCore XS1 Devices. Website, 2009. http://www.xmos.com/published/xcxs1.

[3] David May and Henk Muller. XCore XS1 Architecture Tutorial. Website, 2009. http://www.xmos.com/published/xs1tut.