

ADIS16204 ANOMALIES

This anomaly list describes the known bugs, anomalies, and workarounds for the ADIS16204.

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADIS16204 ANOMALY STATUS

Reference Number	Description	Status
er001	Flash/EE memory update failures	Fixed
er002	Capture buffer recovery, single sample glitch	Fixed
er003	Scale calibration register math error	Fixed
er004	STATUS register not clearing when read	Fixed
er005	Autonull function results fail under negative acceleration	Fixed
er006	ALM_SMPL1/ALM_SMPL2 writes cause device failure	Fixed

MANUAL FLASH/EE MEMORY UPDATE FAILURES [er001]

Background	The ADIS16204 uses a dual memory structure to maintain its operational configuration. The RAM register structure controls the operation of the device and the Flash/EE memory contents determine what is loaded into the RAM at start-up and during reset recovery events. The Flash/EE memory is updated by using a control bit in the COMMAND register of this part.
Issue	Flash/EE memory update was failing at a rate of approximately 5%.
Workaround	Date Code 0718 and older can exhibit this behavior. If it is encountered, use the STATUS register to check for a failed flash memory update; if the error flag indicates a failure, try it again.
Related Issues	None.

CAPTURE BUFFER RECOVERY, SINGLE SAMPLE GLITCH [er002]

Background	The ADIS16204 capture buffers can be accessed in two different ways. The second method involves using the CAPT_PNTR register, which serves as a pointer. This pointer determines which memory location loads into the two output capture registers: CAPT_BUF1 and CAPT_BUF2, which can then be read by the system processor.
Issue	The CAPT_PNTR pointer was off by one memory location, which caused it to point to a single point in the memory space not assigned to the capture function. The net result was a single bad data point that can show up as a glitch in the capture record. If the CAPT_BUF1/CAPT_BUF2 registers are read repeatedly, the CAPT_PNTR points to the correct location and increments with each read. This anomaly only occurs when using the CAPT_PNTR to manually point to specific capture record samples.
Workaround	This issue is isolated to parts up to and including Date Code 0718. For newer date codes, this issue has been resolved.
Related Issues	None.

SCALE CALIBRATION REGISTER MATH ERROR [er003]

Background	The ADIS16204 provides scale correction registers to accommodate calibration adjustments after system-level installation. These registers are XACCL_SCALE, YACCL_SCALE, XINCL_SCALE, and YINCL_SCALE.
Issue	The lower byte of the scale adjustment registers was not computing correctly. Small adjustments result in large output errors.
Workaround	Date Code 0750 and older can exhibit this behavior. Firmware Revision 1.5 fixed this issue. Verify this by reading the contents of 0x52 (lower byte) which is 0x15, if the fix is in place. If it is equal to 0x14 or lower, this issue exists on the part. If scale adjustment is not used, then the device operates without error.
Related Issues	None.

Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113 ©2008 Analog Devices, Inc. All rights reserved.

STATUS REGISTER NOT CLEARING WHEN READ [er004]

Background	The STATUS register contains various diagnostic error flags, which clear when read.
Issue	The STATUS register clears when Address 0x3D is read, but not when Address 0x3C is read.
Workaround	Date Code 0750 and older can exhibit this behavior. Firmware Revision 1.5 fixed this issue. Verify this by reading the contents of 0x52 (lower byte) which is 0x15, if the fix is in place. If it is equal to 0x14 or lower, this issue exists on the part. If this issue is encountered, switch the read address to 0x3D to clear the flags.
Related Issues	None.

AUTONULL FUNCTION RESULTS FAIL UNDER NEGATIVE ACCELERATION [er005]

Background	The autonull function simply measures the output of each acceleration and inclinometer register and then loads an equal but opposite value into the user-configurable offset null registers. This restores the outputs to zero.
Issue	When a negative acceleration acts upon the device during the autonull, it can return a positive output rather than zero.
Workaround	Date Code 0750 and older can exhibit this behavior. Firmware Revision 1.5 fixed this issue. Verify this by reading the contents of 0x52 (lower byte) which is 0x15, if the fix is in place. If it is equal to 0x14 or lower, this issue exists on the part. If this issue is encountered, manual calibration adjustment is a better option.
Related Issues	None.

ALM_SMPL1/ALM_SMPL2 WRITE CAUSES DEVICE FAILURE [er006]

Background	The ALM_SMPL1/ALM_SMPL2 registers provide critical timing configuration data for rate-of-change alarm settings, limited to one byte. The upper bytes of this register are documented as not used.
Issue	Writing to the upper byte of these registers causes a device failure.
Workaround	Date Code 0750 and older can exhibit this behavior. Firmware Revision 1.5 fixed this issue. Verify this by reading the contents of 0x52 (lower byte) which is 0x15, if the fix is in place. If it is equal to 0x14 or lower, this issue exists on the part. Do not attempt to write to the upper bytes of these registers, which are located at Address 0x25 and Address 0x27.
Related Issues	None.