Programmable Low Power Gyroscope

ADIS16251

FEATURES

Yaw rate gyroscope with digital range scaling
±20°/sec, ±40°/sec, and ±80°/sec settings
14-bit digital gyroscope sensor outputs
12-bit digital temperature sensor output
Calibrated sensitivity and bias
In-system, auto-zero for bias drift calibration
Digitally controlled sample rate
Digitally controlled frequency response
Dual alarm settings with configurable operation
Embedded integration for short-term angle estimates
Digitally activated self-test
Digitally activated low power mode
Interrupt-driven wake-up
SPI-compatible serial interface
49 Hz sensor bandwidth
Auxiliary 12-bit ADC input and 12-bit DAC output
Auxiliary digital input/output
Single-supply operation: 4.75 V to 5.25 V
2000 *g* powered shock survivability

APPLICATIONS

Instrumentation control
Platform control and stabilization
Motion control and analysis
Avionics instrumentation
Navigation
Image stabilization
Robotics

FUNCTIONAL BLOCK DIAGRAM

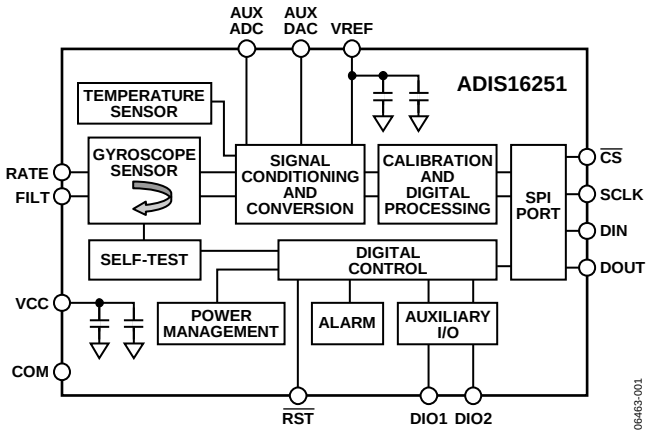

Figure 1.

GENERAL DESCRIPTION

The ADIS16251 is a complete angular rate, measurement system, available in a single compact package enabled by Analog Devices, Inc. *i*Sensor™ integration. By enhancing Analog Devices *i*MEMS® sensor technology with an embedded signal processing solution, the ADIS16251 provides factory-calibrated and tunable digital sensor data in a convenient format that can be accessed using a simple SPI serial interface. The SPI interface provides access to measurements for the gyroscope, temperature, power supply, and one auxiliary analog input. Easy access to calibrated digital sensor data provides developers with a system-ready device, reducing development time, cost, and program risk.

The device range can be digitally selected from three different settings: ±20°/sec, ±40°/sec, and ±80°/sec. Unique characteristics of the end system are accommodated easily through several built-in features, including a single-command auto-zero recalibration function, as well as a configurable sample rate and frequency response. Additional features can be used to further reduce system complexity, including:

- Configurable alarm function
- Auxiliary 12-bit ADC and DAC
- Two configurable digital I/O ports
- Digital self-test function

System power dissipation can be optimized via the ADIS16251 power management features, including an interrupt-driven wake-up. The ADIS16251 is available in an 11 mm × 11 mm × 5.5 mm, laminate-based, land grid array (LGA) package with a temperature range of −40°C to +85°C.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

11/09—Rev. 0 to Rev. A

Change to Endurance Parameter, Table 1 ... 4

4/07—Revision 0: Initial Version

SPECIFICATIONS

T_A = −40°C to +85°C, V_{CC} = 5.0 V, angular rate = 0°/sec, ±1 *g*, ±80°/sec range setting, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
SENSITIVITY	Clockwise rotation is positive output				
	At 25°C, dynamic range = ±80°/sec[1]		0.01832		°/sec/LSB
	At 25°C, dynamic range = ±40°/sec		0.00916		°/sec/LSB
	At 25°C, dynamic range = ±20°/sec		0.00458		°/sec/LSB
Initial Tolerance	At 25°C, dynamic range = ±80°/sec		±0.2	±1	%
Temperature Coefficient	See Figure 8		325		ppm/°C
Power Supply Variation	At 25°C, 1 σ, V_{CC} = 4.75 V to 5.25 V		0.21		%
Nonlinearity	Best fit straight line		0.1		% of FS
BIAS					
In Run Bias Stability	At 25°C, 1 σ		0.016		°/sec
Turn-On-to-Turn-On Bias Stability	At 25°C, 1 σ		0.018		°/sec
Angular Random Walk	At 25°C, 1 σ		3.6		°/√hour
Temperature Coefficient	See Figure 7		0.03		°/sec/°C
Linear Acceleration Effect	Any axis		0.2		°/sec/*g*
Power Supply Sensitivity	At 25°C, 1 σ, V_{CC} = 4.75 V to 5.25 V		0.4		°/sec/V
NOISE PERFORMANCE					
Output Noise	At 25°C, ±80°/sec range, no filtering		0.48		°/sec rms
	At 25°C, ±40°/sec range, 4-tap filter setting		0.28		°/sec rms
	At 25°C, ±20°/sec range, 16-tap filter setting		0.14		°/sec rms
Rate Noise Density	At 25°C, f = 25 Hz, ±80°/sec range, no filtering		0.056		°/sec/√Hz rms
FREQUENCY RESPONSE					
3 dB Bandwidth	See the Analog Bandwidth section for adjustment		49		Hz
Sensor Resonant Frequency			14		kHz
SELF-TEST STATE					
Change for Positive Stimulus	±80°/sec dynamic range setting	1672	2884	4449	LSB
Change for Negative Stimulus	±80°/sec dynamic range setting	−1672	−2884	−4449	LSB
Internal Self-Test Cycle Time			20		ms
TEMPERATURE SENSOR					
Output at 25°C			0		LSB
Scale Factor			6.88		LSB/°C
ADC INPUT					
Resolution			12		Bits
Integral Nonlinearity			±2		LSB
Differential Nonlinearity			±1		LSB
Offset Error			±4		LSB
Gain Error			±2		LSB
Input Range		0		2.5	V
Input Capacitance	During acquisition		20		pF
ON-CHIP VOLTAGE REFERENCE			2.5		V
Accuracy	At 25°C	−10		+10	mV
Temperature Coefficient			±40		ppm/°C
Output Impedance			70		Ω

Parameter	Conditions	Min	Typ	Max	Unit
DAC OUTPUT	5 kΩ/100 pF to GND				
Resolution			12		Bits
Relative Accuracy	For Code 101 to Code 4095		4		LSB
Differential Nonlinearity			1		LSB
Offset Error			±5		mV
Gain Error			±0.5		%
Output Range			0 to 2.5		V
Output Impedance			2		Ω
Output Settling Time			10		µs
LOGIC INPUTS					
Input High Voltage, V_{INH}		2.0			V
Input Low Voltage, V_{INL}				0.8	V
	For $\overline{CS}$ signal when used to wake up from sleep mode			0.55	V
Logic 1 Input Current, I_{INH}	V_{IH} = 3.3 V		±0.2	±10	µA
Logic 0 Input Current, I_{INL}	V_{IL} = 0 V				
All except $\overline{RST}$			−40	−60	µA
$\overline{RST}$[2]			−1		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1.6 mA			0.4	V
SLEEP TIMER					
Timeout Period[3]		0.5		128	sec
START-UP TIME					
Initial			160		ms
Sleep Mode Recovery			2.5		ms
FLASH MEMORY					
Endurance[4]		10,000			Cycles
Data Retention[5]	T_J = 55°C	20			Years
CONVERSION RATE					
Minimum Conversion Time	SMPL_PRD setting = 0x01		3.906		ms
Maximum Conversion Time	SMPL_PRD setting = 0x0F		7.75		sec
Maximum Throughput Rate	SMPL_PRD setting = 0x01		256		SPS
Minimum Throughput Rate	SMPL_PRD setting = 0x0F		0.129		SPS
POWER SUPPLY					
Operating Voltage Range, V_{CC}		4.75	5.0	5.25	V
Power Supply Current	Normal mode at 25°C		18		mA
	Fast mode at 25°C		44		mA
	Sleep mode at 25°C		335		µA

[1] The sensor is capable of ±150°/sec, but the specifications herein are for ±80°/sec only.
[2] The $\overline{RST}$ pin has an internal pull-up.
[3] Guaranteed by design.
[4] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[5] Retention lifetime equivalent at the junction temperature (T_J) of 55°C, as per JEDEC Standard 22 Method A117. Retention lifetime decreases with junction temperature.

TIMING SPECIFICATIONS

Table 2.

Parameter	Description	Min[1]	Typ	Max[1]	Unit
f_{SCLK}	Fast mode (SMPL_PRD ≥ 0x07; f_S ≥ 64 Hz)	0.01		2.5	MHz
	Normal mode (SMPL_PRD < 0x07; f_S ≤ 56.9 Hz)	0.01		1.0	MHz
$t_{DATARATE}$	Data rate period, fast mode (SMPL_PRD ≥ 0x07; f_S ≥ 64 Hz)	32			µs
	Data rate period, normal mode (SMPL_PRD < 0x07; f_S ≤ 56.9 Hz)	42			µs
$t_{DATASTALL}$	Data stall time, fast mode (SMPL_PRD ≥ 0x07; f_S ≥ 64 Hz)	9			µs
	Data stall time, normal mode (SMPL_PRD < 0x07; f_S ≤ 56.9 Hz)	12			µs
t_{CSHIGH}	Chip select high	$1/f_{SCLK}$			
t_{CS}	Chip select to clock edge	48.8			ns
t_{DAV}	Data output valid after SCLK edge[2]			100	ns
t_{DSU}	Data input setup time before SCLK rising edge	24.4			ns
t_{DHD}	Data input hold time after SCLK rising edge	48.8			ns
t_{DF}	Data output fall time		5	12.5	ns min
t_{DR}	Data output rise time		5	12.5	ns min
t_{SFS}	$\overline{CS}$ high after SCLK edge[3]	5			ns
	Flash update time (power supply must be within range)	50			ms

[1] Guaranteed by design; typical specifications are not tested or guaranteed.
[2] The MSB presents an exception to this parameter. The MSB clocks out on the falling edge of $\overline{CS}$. The rest of the DOUT bits are clocked out after the falling edge of SCLK and are governed by this specification.
[3] This parameter may need to be expanded to allow for proper capture of the LSB. After $\overline{CS}$ goes high, the DOUT line goes into a high impedance state.

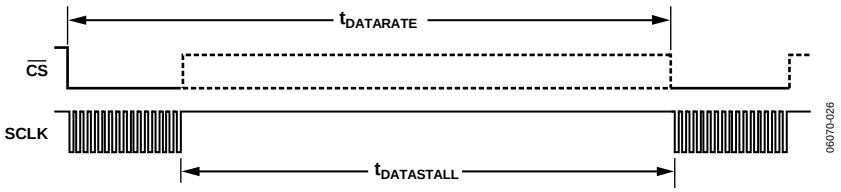

Figure 2. SPI Chip Select Timing

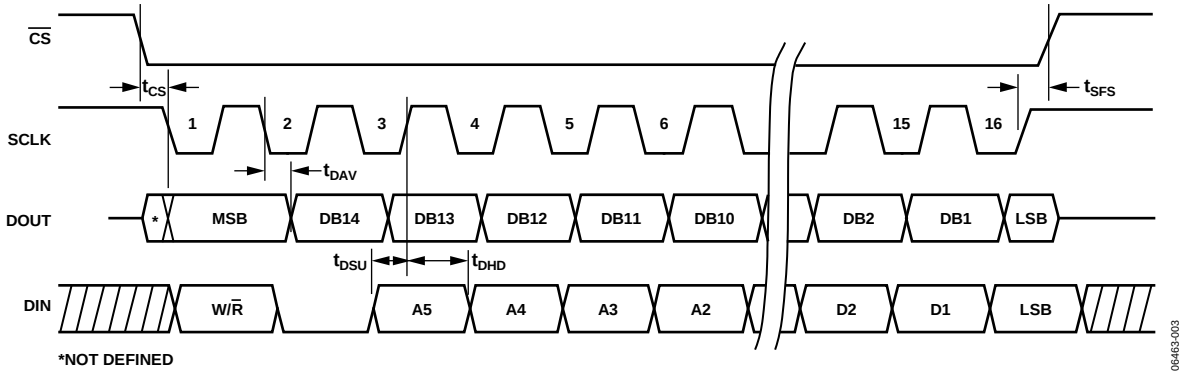

Figure 3. SPI Timing
(Utilizing SPI Settings Typically Identified as Phase = 1, Polarity = 1)

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration (Any Axis, Unpowered, 0.5 ms)	2000 *g*
Acceleration (Any Axis, Powered, 0.5 ms)	2000 *g*
V_{CC} to COM	−0.3 V to +6.0 V
Digital Input/Output Voltage to COM	−0.3 V to +5.5 V
Analog Inputs to COM	−0.3 V to +3.5 V
Operating Temperature Range[1]	−40°C to +125°C
Storage Temperature Range[1]	−65°C to +150°C

[1] Extended exposure to temperatures outside of the specified temperature range of −40°C to +85°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the parts within the specified operating range of −40°C to +85°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

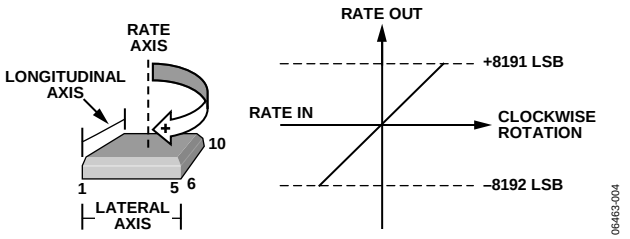

Figure 4. RATE OUT Level Increase with Clockwise Rotation Increase

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

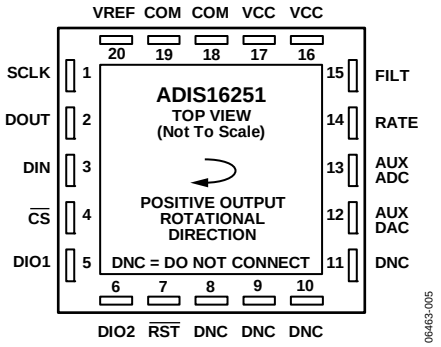

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	SCLK	I	SPI Serial Clock.
2	DOUT	O	SPI Data Output.
3	DIN	I	SPI Data Input.
4	$\overline{CS}$	I	SPI Chip Select, Active Low.
5, 6	DIO1, DIO2	I/O	Multifunction Digital Input/Outputs.
7	$\overline{RST}$	I	Reset, Active Low. This resets the sensor signal conditioning circuit and initiates a start-up sequence.
8, 9, 10, 11	DNC	–	Do Not Connect.
12	AUX DAC	O	Auxiliary DAC Analog Output Voltage.
13	AUX ADC	I	Auxiliary ADC Analog Input Voltage.
14	RATE	O	Analog Rate Signal Output (Uncalibrated).
15	FILT	I	Analog Amplifier Summing Junction. This is used for setting the analog bandwidth. See the Analog Bandwidth section for more details.
16, 17	VCC	S	5.0 V Power Supply.
18, 19	COM	S	Common. Reference point for all circuitry in the ADIS16251.
20	VREF	O	Precision Reference Output.

[1] S = supply; O = output; I = input.

RECOMMENDED LAYOUT

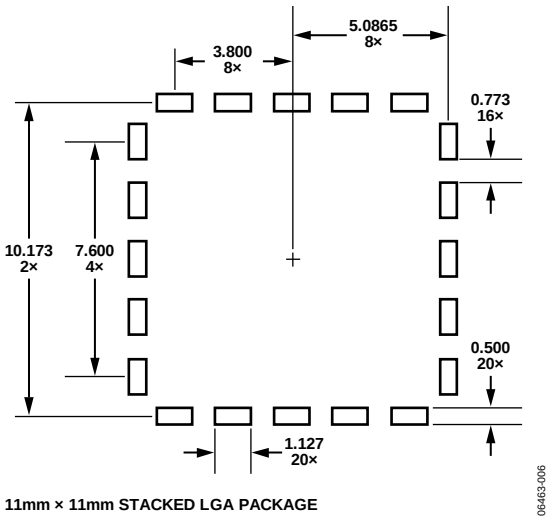

Figure 6. Recommended Pad Layout (Units in Millimeters)

TYPICAL PERFORMANCE CHARACTERISTICS

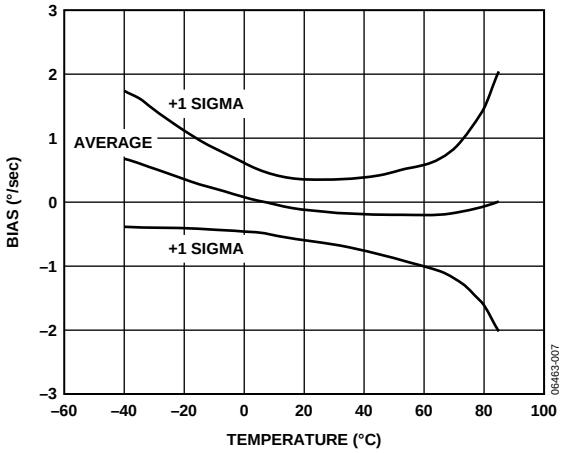

Figure 7. Bias vs. Temperature, ADIS16251

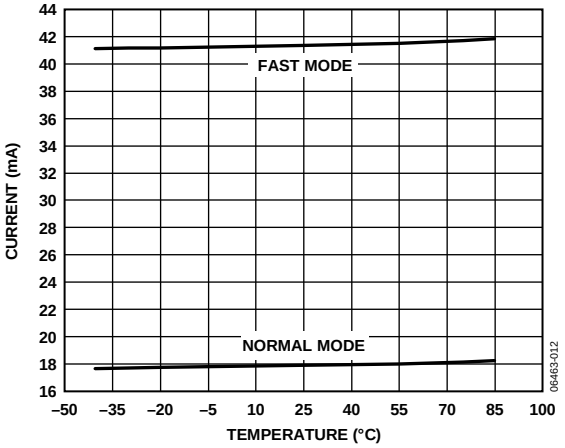

Figure 10. Current vs. Temperature

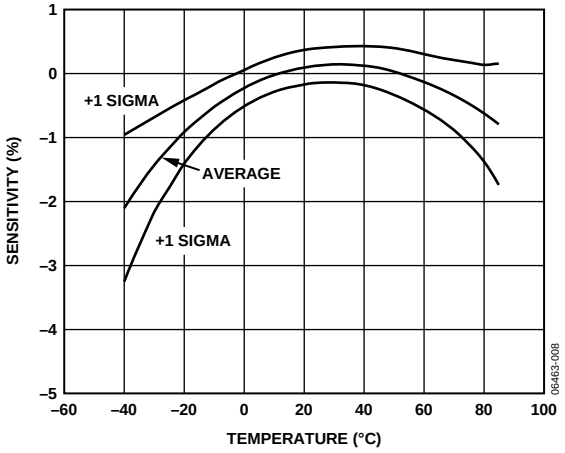

Figure 8. Sensitivity vs. Temperature, ADIS16251

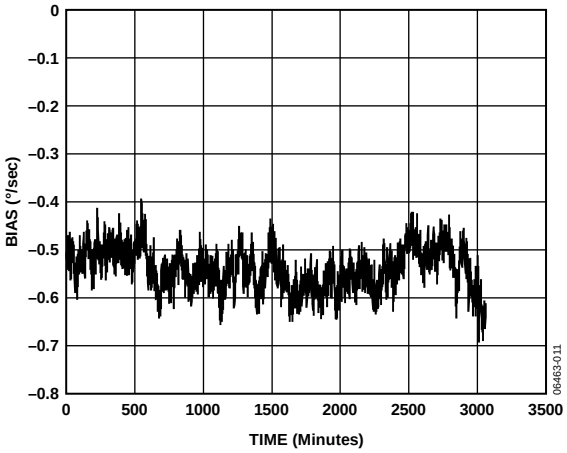

Figure 11. Bias vs. Time

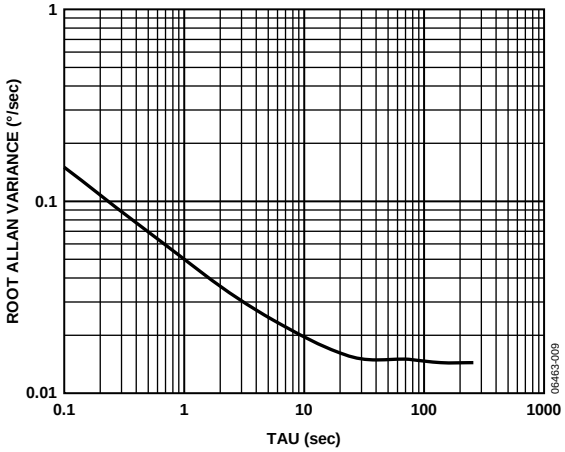

Figure 9. Root Allan Variance vs. TAU, ±80°/sec Range

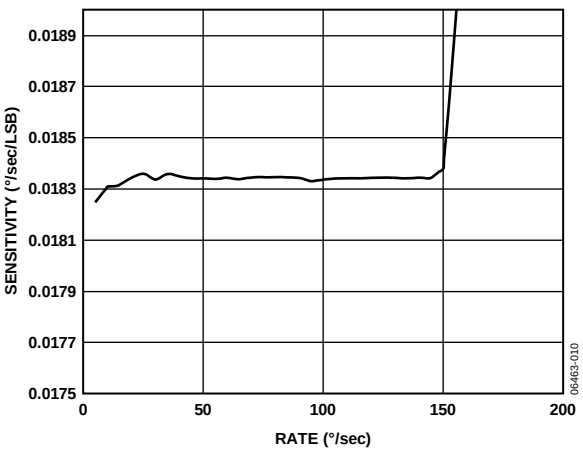

Figure 12. Sensitivity vs. Angular Rate, ±80°/sec Range

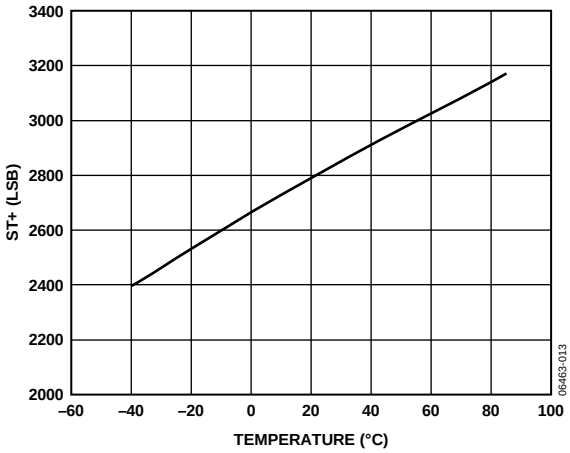

Figure 13. Positive Self-Test vs. Temperature

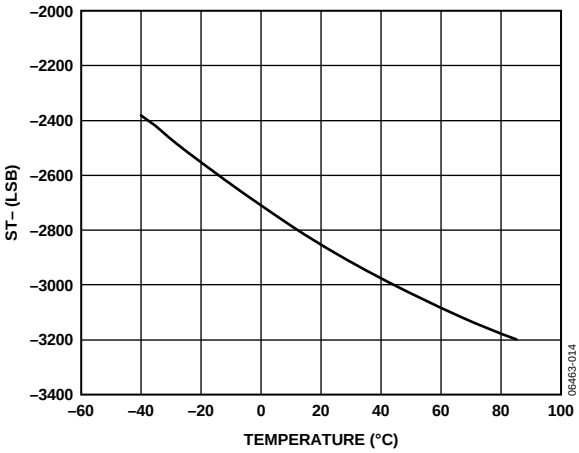

Figure 14. Negative Self-Test vs. Temperature

THEORY OF OPERATION

OVERVIEW

The core angular rate sensor integrated into the ADIS16251 is based on the Analog Devices *i*MEMS technology. This sensor operates on the principle of a resonator gyroscope. Two polysilicon sensing structures each contain a dither frame electrostatically driven to resonance. This provides the necessary velocity element to produce a Coriolis force during rotation. At two of the outer extremes of each frame (orthogonal to the dither motion) are movable fingers placed between fixed fingers to form a capacitive pickoff structure that senses Coriolis motion. The resulting signal is fed to a series of gain and demodulation stages that produce the electrical rate signal output.

The base sensor output signal is sampled using an ADC, and then the digital data is fed into a proprietary digital calibration circuit. This circuit contains calibration coefficients from the factory calibration, along with user-defined calibration registers that can be used to calibrate system-level errors.

The calibrated gyroscope data (GYRO_OUT) is made available through output data registers along with temperature, power supply, auxiliary ADC, and relative angle output calculations.

RELATIVE ANGLE ESTIMATE

The ANGL_OUT register offers the integration of the GYRO_OUT data. In order for this information to be useful, the reference angle must be known. This can be accomplished by reading the register contents at the initial time, before starting the monitoring, or by setting its contents to zero. This number is reset to zero during power-up and is executed when the null command is used as well as after a reset command. This function can be used to estimate change in an angle over a period of time. The user is cautioned to fully understand the stability requirements and the time period over which to use this estimated relative angle position.

FACTORY CALIBRATION

The ADIS16251 provides a factory calibration that includes correction for initial tolerance and power supply variation. This calibration includes individual sensor characterization and a custom correction coefficient calculation.

AUXILIARY ADC FUNCTION

The auxiliary ADC function integrates a standard 12-bit ADC into the ADIS16251 to digitize other system-level analog signals. The output of the ADC can be monitored through the AUX_ADC control register, see Table 5. The ADC is a 12-bit successive approximation converter. The output data is presented in straight binary format with the full-scale range extending from 0 V to 2.5 V. The 2.5 V upper limit is derived from the on-chip precision internal reference.

Figure 15 shows the equivalent circuit of the analog input structure of the ADC. The input capacitor (C1) is typically 4 pF and can be attributed to parasitic package capacitance. The two diodes provide ESD protection for the analog input. Care must be taken to ensure that the analog input signals never exceed the range of −0.3 V to +3.5 V. This causes the diodes to become forward-biased and to start conducting. The diodes can handle 10 mA without causing irreversible damage. The resistor is a lumped component that represents the on resistance of the switches. The value of this resistance is typically 100 Ω. Capacitor C2 represents the ADC sampling capacitor and is typically 16 pF.

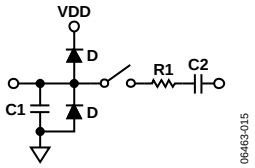

Figure 15. Equivalent Analog Input Circuit, Conversion Phase: Switch Open, Track Phase: Switch Closed

For ac applications, it is recommended to remove high frequency components from the analog input signal by using a low-pass filter on the analog input pin.

In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input must be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This can necessitate the use of an input buffer amplifier. When no input amplifier is used to drive the analog input, the source impedance should be limited to values lower than 1 kΩ.

BASIC OPERATION

The ADIS16251 is designed for simple integration into industrial system designs, requiring only a 5.0 V power supply and a 4-wire, industry standard serial peripheral interface (SPI). All outputs and user-programmable functions are handled by a simple register structure. Each register is 16 bits in length and has its own unique bit map. The 16 bits in each register consist of an upper byte (Bit 8 to Bit 15) and a lower byte (Bit 0 to Bit 7), each of which has its own 6-bit address.

SERIAL PERIPHERAL INTERFACE (SPI)

The ADIS16251 SPI port includes four signals: chip select ($\overline{CS}$), serial clock (SCLK), data input (DIN), and data output (DOUT). The $\overline{CS}$ line enables the ADIS16251 SPI port and frames each SPI event. When this signal is high, the DOUT lines are in a high impedance state and the signals on DIN and SCLK have no impact on operation. A complete data frame contains 16 clock cycles. Because the SPI port operates in full duplex mode, it supports simultaneous, 16-bit receive (DIN) and transmit (DOUT) functions during the same data frame.

See Table 2, Figure 2, and Figure 3 for detailed timing and operation of the SPI port.

Writing to Registers

Figure 16 displays a typical data frame for writing a command to a control register. In this case, the first bit of the DIN sequence is a 1, followed by a 0, the 6-bit address, and the 8-bit data command. Because each write command covers a single byte of data, two data frames are required when writing to the entire 16-bit space of a register.

Reading from Registers

Reading the contents of a register requires a modification to the sequence in Figure 16. In this case, the first two bits in the DIN sequence are 0, followed by the address of the register. Each register has two addresses (upper and lower), but either one can be used to access its entire 16 bits of data. The final eight bits of the DIN sequence are irrelevant and can be counted as don't cares during a read command. During the next data frame, the DOUT sequence contains the register's 16-bit data, as shown in Figure 17. Although a single read command requires two separate data frames, the full duplex mode minimizes this overhead, requiring only one extra data frame when continuously sampling.

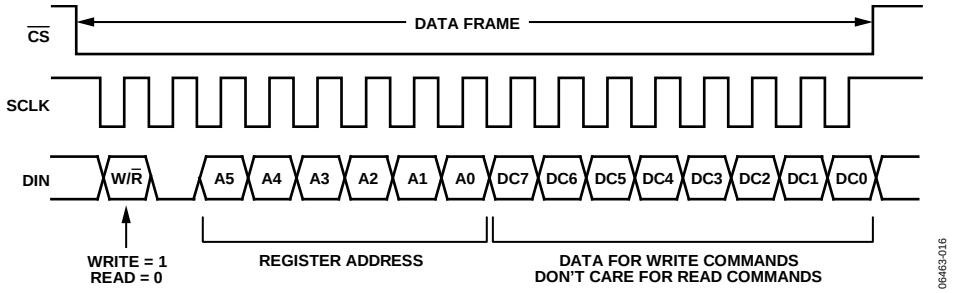

Figure 16. DIN Bit Sequence

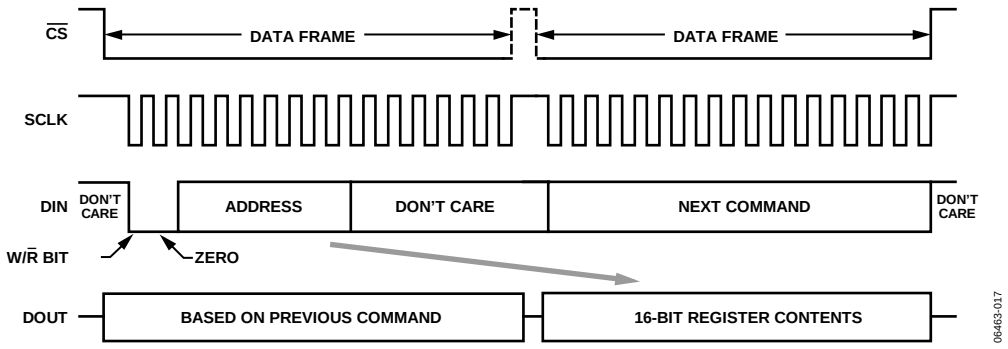

Figure 17. SPI Sequence for Read Commands

DATA OUTPUT REGISTER ACCESS

The ADIS16251 provides access to calibrated rotation measurements, relative angle estimates, power supply measurements, temperature measurements, and an auxiliary 12-bit ADC channel. This output data is continuously updating internally, regardless of user read rates. The following bit map describes the structure of all output data registers, except ENDURANCE.

MSB							LSB
ND	EA	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

The MSB holds the new data (ND) indicator. When the output registers are updated with new data, the ND bit goes to a 1 state. After the output data is read, it returns to a 0 state. The EA bit is used to indicate a system error or an alarm condition that can result from a number of conditions, such as a power supply that is out of the specified operating range. See the Status and Diagnostics section for more details. The output data is either 12 bits or 14 bits in length. For all 12-bit output data, Bit D13 and Bit D12 are assigned don't care status.

The output data register map located in Table 5 provides all the necessary details for accessing each register's data. Table 6 displays the output coding for the GYRO_OUT register. Figure 18 provides an example SPI read cycle for this register.

Table 5. Data Output Register Information

Name	Function	Address	Resolution (Bits)	Data Format	Scale Factor (per LSB)
ENDURANCE	Flash memory write counter	0x01, 0x00	16	Binary	1 count
SUPPLY_OUT	Power supply data	0x03, 0x02	12	Binary	1.8315 mV
GYRO_OUT	Gyroscope data	0x05, 0x04	14	Twos complement	0.01832°/sec[1]
AUX_ADC	Auxiliary analog input data	0x0B, 0x0A	12	Binary	0.6105 mV
TEMP_OUT	Sensor temperature data	0x0D, 0x0C	12	Twos complement	0.1453°C
ANGL_OUT	Angle output	0x0F, 0x0E	14	Binary	0.03663°/sec

[1] Assumes that the scaling is set to 80°/sec.

Table 6. Output Coding Example, GYRO_OUT[1, 2]

Rate of Rotation					
±80°/sec Range	±40°/sec Range	±20°/sec Range	Binary Output	Hex Output	Decimal
150°/sec	75°/sec	37.5°/sec	01 1111 1111 1111	0x1FFF	8191
80°/sec	40°/sec	20°/sec	01 0001 0001 0000	0x1110	4368
20°/sec	10°/sec	5°/sec	00 0100 0100 0100	0x0444	1092
10°/sec	5°/sec	2.5°/sec	00 0010 0010 0010	0x0222	546
0.01832°/sec	0.00916°/sec	0.00458°/sec	00 0000 0000 0001	0x0001	1
0°/sec	0°/sec	0°/sec	00 0000 0000 0000	0x0000	0
−0.01832°/sec	−0.00916°/sec	−0.00458°/sec	11 1111 1111 1111	0x3FFF	−1
−10°/sec	−5°/sec	−2.5°/sec	11 1101 1101 1110	0x3DDE	−546
−20°/sec	−10°/sec	−5°/sec	11 1011 1011 1100	0x3BBC	−1092
−80°/sec	−40°/sec	−20°/sec	10 1110 1111 0000	0x2EF0	−4368
−150°/sec	−75°/sec	−37.5°/sec	10 0000 0000 0000	0x2000	−8192

[1] Two MSBs have been masked off and are not considered in the coding.
[2] Nominal sensitivity and zero offset null performance are assumed.

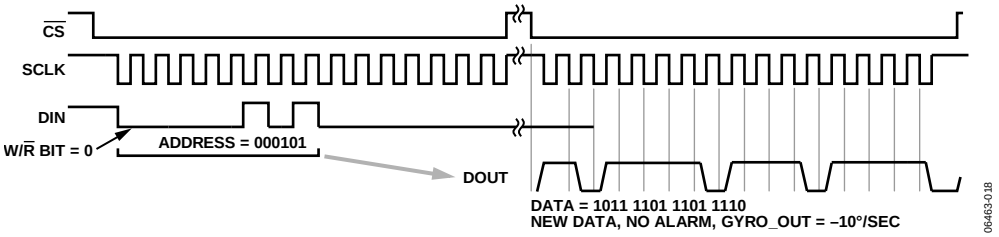

Figure 18. Example of a Read Cycle, ±80°/sec Setting

PROGRAMMING AND CONTROL

CONTROL REGISTER OVERVIEW

The ADIS16251 offers many programmable features controlled by writing commands to the appropriate control registers using the SPI. Table 7 provides a summary of these control registers, which controls the operation of the following parameters:

- Calibration
- Global commands
- Operational control
  - Sample rate
  - Power management
  - Digital filtering
  - Dynamic range
  - DAC output
  - Digital I/O
- Operational status and diagnostics
  - Self test
  - Status conditions
  - Alarms

CONTROL REGISTER STRUCTURE

The ADIS16251 uses a temporary, RAM-based memory structure to facilitate the control registers displayed in Table 7. The start-up configuration is stored in a flash memory structure that automatically loads into the control registers during the start-up sequence. Each nonvolatile register has a corresponding flash memory location for storing the latest configuration contents. Because flash memory has endurance limitations, the contents of each nonvolatile register must be stored to flash manually. Please note that the contents of the control register are only nonvolatile when they are stored to flash. The manual flash update command, made available in the COMMAND register, provides this function. The ENDURANCE register provides a counter, which allows for reliability management against the flash memory's write cycle specification.

Table 7. Control Register Mapping

Register Name	Type	Volatility	Address	Bytes	Function	Reference Table
GYRO_OFF	R/W	Nonvolatile	0x15, 0x14	2	Gyroscope bias offset factor	Table 8, Table 9
GYRO_SCALE	R/W	Nonvolatile	0x17, 0x16	2	Gyroscope scale factor	Table 10, Table 11
			0x18 to 0x1F	8	Reserved	
ALM_MAG1	R/W	Nonvolatile	0x21, 0x20	2	Alarm 1 amplitude threshold and polarity	Table 30, Table 31
ALM_MAG2	R/W	Nonvolatile	0x23, 0x22	2	Alarm 2 amplitude threshold and polarity	Table 34, Table 35
ALM_SMPL1	R/W	Nonvolatile	0x25, 0x24	2	Alarm 1 sample period	Table 32, Table 33
ALM_SMPL2	R/W	Nonvolatile	0x27, 0x26	2	Alarm 2 sample period	Table 36, Table 37
ALM_CTRL	R/W	Nonvolatile	0x29, 0x28	2	Alarm control register	Table 38, Table 39
			0x2A to 0x2F	6	Reserved	
AUX_DAC	R/W	Volatile	0x31, 0x30	2	Auxiliary DAC data	Table 20, Table 21
GPIO_CTRL	R/W	Volatile	0x33, 0x32	2	Auxiliary digital I/O control register	Table 22, Table 23
MSC_CTRL	R/W	Nonvolatile[1]	0x35, 0x34	2	Miscellaneous control register	Table 25, Table 26
SMPL_PRD	R/W	Nonvolatile	0x37, 0x36	2	ADC sample period control	Table 14, Table 15
SENS/AVG	R/W	Nonvolatile	0x39, 0x38	2	Defines the dynamic range (sensitivity setting) and the number of taps for the digital filter	Table 18, Table 19
SLP_CNT	R/W	Volatile	0x3B, 0x3A	2	Counter used to determine length of power-down mode	Table 16, Table 17
STATUS	R	Volatile	0x3D, 0x3C	2	System status register	Table 27, Table 28
COMMAND	W	N/A	0x3F, 0x3E	2	System command register	Table 12, Table 13

[1] The contents of the upper byte are nonvolatile; the contents of the lower byte are volatile.

CALIBRATION

The ADIS16251 is factory-calibrated for sensitivity and bias. It also provides several user calibration functions for simplifying field-level corrections. The calibration factors are stored in nonvolatile memory and are applied using the following linear calibration equation:

$$y = mx + b$$

where:
y is the calibrated output data.
m is the sensitivity scale factor.
x is the precalibration data.
b is the offset scale factor.

There are three options for system-level calibrations of the bias in the ADIS16251: autonull, factory calibration restore, and manual calibration updates. The autonull and factory reset options are described in the Global Commands section. Optional field-level calibrations use the preceding equation and require the following two steps:

1. Characterize the behavior of the ADIS16251 at predefined critical operating conditions.
2. Use this characterization data to calculate and load the contents of GYRO_OFF (b) and GYRO_SCALE (m).

The GYRO_OFF provides a calibration range of ±75°/sec, and its contents are nonvolatile. The GYRO_SCALE register provides a calibration range of 0 to 1.9995, and its contents are also nonvolatile.

Table 8. GYRO_OFF Register Definition

Address	Scale[1]	Default	Format	Access
0x15, 0x14	0.00458°/sec	0x0000	Twos complement	R/W

[1] Scale is the weight of each LSB.

Table 9. GYRO_OFF Bit Descriptions

Bit	Description
15:14	Not used
13:0	Data bits

Table 10. GYRO_SCALE Register Definition

Address	Scale[1]	Default[2]	Format	Access
0x17, 0x16	0.0487%	0x0800	Binary	R/W

[1] Scale is the weight of each LSB.
[2] Equates to a scale factor of one.

Table 11. GYRO_SCALE Bit Descriptions

Bit	Description
15:12	Not used
11:0	Data bits

GLOBAL COMMANDS

The ADIS16251 provides global commands for common operations such as autonull, factory calibration restore, manual flash update, auxiliary DAC latch, and software reset. Each of these global commands has a unique control bit assigned to it in the COMMAND register and is initiated by writing a 1 to its assigned bit.

The autonull function does two things: it resets the contents of the ANGL_OUT register to zero, and it adjusts the GYRO_OUT register to zero. This automated adjustment requires the following two steps:

1. Read GYRO_OUT.
2. Write the opposite of this value into the GYRO_OFF register. Sensor noise influences the accuracy of this step.

For optimal calibration accuracy, set the number of filtering taps to its maximum, wait for the appropriate number of samples to process through the filter, and then exercise this option.

The factory calibration restore command sets the contents of GYRO_OFF to 0x0000 and GYRO_SCALE to 0x0800, erasing any field-level calibration contents. The manual flash update writes the contents of each nonvolatile register into flash memory for storage. This process takes approximately 50 ms and requires the power supply voltage to be within specification for the duration of the event. It is worth noting that this operation also automatically follows the autonull and factory reset commands.

The DAC latch command loads the contents of AUX_DAC into the DAC latches. Since the AUX_DAC contents must be updated one byte at a time, this command ensures a stable DAC output voltage during updates. Finally, the software reset command sends the ADIS16251 digital processor into a restart sequence, effectively doing the same thing as the $\overline{\text{RST}}$ line.

Table 12. COMMAND Register Definition

Address	Default	Format	Access
0x3F, 0x3E	N/A	N/A	Write only

Table 13. COMMAND Bit Descriptions

Bit	Description
15:8	Not used
7	Software reset command
6:4	Not used
3	Manual flash update command
2	Auxiliary DAC data latch
1	Factory calibration restore command
0	Autonull command

OPERATIONAL CONTROL

Internal Sample Rate

The internal sample rate defines how often data output variables are updated, independent of the rate at which they are read out on the SPI port. The SMPL_PRD register controls the ADIS16251s internal sample rate and has two parts: a selectable time base and a multiplier. The sample period can be calculated using the following equation:

$$T_S = T_B \times (N_S + 1)$$

where:
T_S is the sample period.
T_B is the time base.
N_S is the increment setting.

The default value is the maximum 256 SPS, and the contents of this register are nonvolatile.

Table 14. SMPL_PRD Register Definition

Address	Default	Format	Access
0x37, 0x36	0x0001	N/A	R/W

Table 15. SMPL_PRD Bit Descriptions

Bit	Description
15:8	Not used
7	Time base, 0 = 1.953 ms, 1 = 60.54 ms
6:0	Multiplier

The following is an example calculation of the sample period for the ADIS16251:

If *SMPL_PRD* = 0x0007, *B7*…*B0* = 00000111

B7 = 0 → T_B = 1.953 ms

B6…*B0* = 000000111 → N_S = 7

$T_S = T_B \times (N_S + 1)$ = 1.953 ms × (7 + 1) = 15.624 ms

$f_S = 1/T_S$ = 64 SPS

The sample rate setting has a direct impact on the SPI data rate capability. For sample rates of 64 SPS and above, the SPI SCLK can run at a rate up to 2.5 MHz. For sample rates below 64 SPS, the SPI SCLK can run at a rate up to 1 MHz.

The sample rate setting also affects the power dissipation. When the sample rate is set below 64 SPS, the power dissipation reduces by a factor of 60%. The two different modes of operation offer a system-level trade-off between performance (sample rate, serial transfer rate) and power dissipation.

Power Management

In addition to offering two different performance modes for power optimization, the ADIS16251 offers a programmable shutdown period. Writing the appropriate sleep time to the SLP_CNT register shuts the device down for the specified time. The following example provides an illustration of this relationship:

B7 … *B0* = 00000110

Sleep period = 3 sec

After completing the sleep period, the ADIS16251 returns to normal operation. If the measurements are required before the sleep period completion, the ADIS16251 can be awakened by putting the $\overline{CS}$ line in a zero logic state. Otherwise, the $\overline{CS}$ line must be kept high to maintain sleep mode.

Table 16. SLP_CNT Register Definition

Address	Scale[1]	Default	Format	Access
0x3B, 0x3A	0.5 sec	0x0000	Binary	R/W

[1] Scale is the weight of each LSB.

Table 17. SLP_CNT Bit Descriptions

Bit	Description
15:8	Not used
7:0	Data bits

Analog Bandwidth

The analog bandwidth of the ADIS16251 is 49 Hz. This bandwidth can be reduced by placing an external capacitor across the RATE and FILT pins. In this case, the analog bandwidth can be calculated using the following equation:

$$f_{OUT} = 1/(2\pi \times R_{OUT} \times (C_{OUT} + 0.018\ \mu F))$$

where:
R_{OUT} = 180 kΩ.
C_{OUT} = external capacitance.

Digital Filtering

The ADIS16251 GYRO_OUT signal path has a nominal analog bandwidth of 49 Hz. The ADIS16251 provides a Bartlett Window FIR filter for additional noise reduction on all of the output data registers. The SENS/AVG register stores the number of taps in this filter in seven power-of-two, step sizes (that is, 2^M = 1, 2, 4, 16, 32, 64, and 128). Filter setup requires one simple step: write the appropriate M factor to the assigned bits in the SENS/AVG register. The bit assignments are listed in Table 19. The following equation offers a frequency response relationship for this filter:

$$H_B(f) = H_A^2(f) \Rightarrow H_A(f) = \frac{\sin(\pi \times N \times f \times t_S)}{N \times \sin(\pi \times f \times t_S)}$$

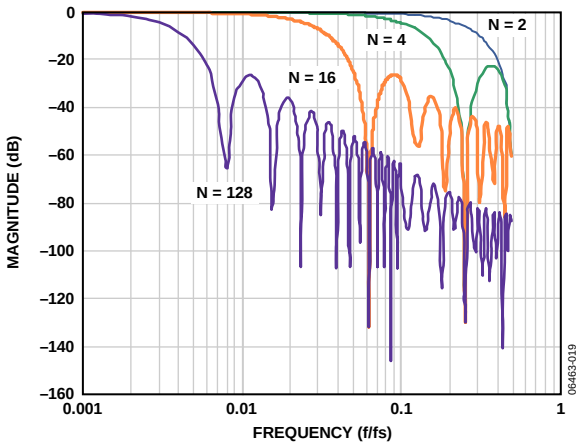

Figure 19. Bartlett Window FIR Frequency Response

Dynamic Range

The ADIS16251 provides three dynamic range settings: ±20°/sec, ±40°/sec, and ±80°/sec. The lower dynamic range settings (±20°/sec, ±40°/sec) limit the minimum filter tap sizes in order to maintain the resolution as the maximum rate measurements decrease. The recommended order for programming the SENS/AVG register is (1) dynamic range and (2) filtering response. The contents of the SENS/AVG register are nonvolatile.

Table 18. SENS/AVG Register Definition

Address	Default	Format	Access
0x39, 0x38	0x0402	Binary	R/W

Table 19. SENS/AVG Bit Descriptions

Bit	Value	Description
15:11		Not used
10:8		Sensitivity selection bits
	100	80°/sec (default condition)
	010	40°/sec, filter taps ≥ 4 (Bits [3:0] ≥ 0x02)
	001	20°/sec, filter taps ≥16 (Bits [3:0] ≥ 0x04)
7:4		Not used
3:0		Filter tap setting, M = binary number (number of taps, N = 2^M)

Auxiliary DAC

The auxiliary DAC provides a 12-bit level adjustment function. The AUX_DAC register controls the operation of this feature. It offers a rail-to-rail buffered output that has a range of 0 V to 2.5 V. The DAC can drive its output to within 5 mV of the ground reference when it is not a sinking current. As the output approaches ground, the linearity begins to degrade (100 LSB beginning point). As the sink current increases, the nonlinear range increases. The DAC output latch function, contained in the COMMAND register, provides continuous operation while writing each byte of this register. The contents of this register are volatile, which means that the desired output level must be set after every reset and power cycle event.

Table 20. AUX_DAC Register Definition

Address	Default	Format	Access
0x31, 0x30	0x0000	Binary	R/W

Table 21. AUX_DAC Bit Descriptions

Bit	Description
15:12	Not used
11:0	Data bits

General-Purpose I/O

The ADIS16251 provides two general-purpose pins that enable digital I/O control using the SPI. The GPIO_CTRL control register establishes the configuration of these pins and handles the SPI-to-pin controls. Each pin provides the flexibility of both input (read) and output (write) operations. For example, writing a 0x0202 to this register establishes Line 2 as an output and sets its level as a 1. Writing 0x0000 to this register establishes both lines as inputs, and their status can be read through Bit 0 and Bit 1 of this register.

The digital I/O lines are also available for data-ready and alarm/error indications. In the event of conflict, the following priority structure governs the digital I/O configuration:

- MSC_CTRL
- ALM_CTRL
- GPIO_CTRL

Table 22. GPIO_CTRL Register Definition

Address	Default	Format	Access
0x33, 0x32	0x0000	N/A	R/W

Table 23. GPIO_CTRL Bit Descriptions

Bit	Description
15:10	Not used
9	General-purpose I/O Line 2 polarity 1 = high 0 = low
8	General-purpose I/O Line 1 polarity 1 = high 0 = low
7:2	Not used
1	General-purpose I/O Line 2, data direction control 1 = output 0 = input
0	General-purpose I/O Line 1, data direction control 1 = output 0 = input

STATUS AND DIAGNOSTICS

The ADIS16251 provides a number of status and diagnostic functions. Table 24 provides a summary of these functions, along with their appropriate control registers.

Table 24. Status and Diagnostic Functions

Function	Register
Data-Ready I/O Indicator	MSC_CTRL
Self-Test, Mechanical Check For MEMS Sensor	MSC_CTRL
Status, Check For Predefined Error Conditions	STATUS
Flash Memory Endurance	ENDURANCE
Alarms, Configure And Check For User-Specific Conditions	ALM_MAG1/ALM_MAG2 ALM_SMPL1/ALM_SMPL2 ALM_CTRL

Data-Ready I/O Indicator

The data-ready function provides an indication of updated output data. The MSC_CTRL register provides the opportunity to configure either of the general-purpose I/O pins (DIO1 and DIO2) as a data-ready indicator signal. After each output register update, the digital I/O changes states, and then returns to its original state, creating a pulsed waveform. The duty cycle of that waveform is between 15% and 35%.

Table 25. MSC_CTRL Register Definition

Address	Default	Format	Access
0x35, 0x34	0x0000	N/A	R/W

Table 26. MSC_CTRL Bit Descriptions

Bit	Description
15:11	Not used
10	Internal self-test enable 1 = enabled 0 = disabled
9	External negative rotation self-test enable 1 = enabled 0 = disabled
8	External positive rotation self-test enable 1 = enabled 0 = disabled
7:3	Not used
2	Data-ready enable 1 = enabled 0 = disabled
1	Data-ready polarity 1 = active high 0 = active low
0	Data-ready line select 1 = DIO2 0 = DIO1

Self-Test

The MSC_CTRL register also provides a self-test function, which verifies the MEMS sensor's mechanical integrity. There are two different self-test options: (1) internal self-test and (2) external self-test. The internal test provides a simple, two-step process for checking the MEMS sensor: (1) start the process by writing a 1 to Bit 10 in the MSC_CTRL register and (2) check the result by reading Bit 5 of the STATUS register, after 35 ms.

The external self-test is a static condition that can be enabled and disabled. In this test, both positive and negative MEMS sensor movements are available. After writing to the appropriate control bit, the GYRO_OUT register reflects the changes after a delay that reflects the sensor signal chain response time. For example, the standard 49 Hz bandwidth reflects an exponential response with a time constant of 3.2 ms. If the bandwidth is reduced externally (a capacitor across RATE and FILT pins) or internally (increasing the number of filter taps, see SENS/AVG register), this time constant increases. For the internal self-test option, increasing the delay can produce false alarms, since the internal timing for this function is optimized for maximum bandwidth. The appropriate bit definitions for self-test are listed in Table 25 and Table 26.

Status Conditions

The STATUS register contains the following error-condition flags: Alarm conditions, self-test status, angular rate over range, SPI communication failure, control register update failure, and power supply out of range. See Table 27 and Table 28 for the appropriate register access and bit assignment for each flag. The bits assigned for checking the power supply range and the angular rate overrange automatically reset to zero when the error condition no longer exists. The remaining error-flag bits in the STATUS register require a read in order to return them to zero. Note that a STATUS register read clears all of the bits to zero.

Table 27. STATUS Register Definition

Address	Default	Format	Access
0x3D, 0x3C	0x0000	N/A	Read-only

Table 28. STATUS Bit Descriptions

Bit	Description
15:10	Not used
9	Alarm 2 status 1 = active 0 = inactive
8	Alarm 1 status 1 = active 0 = inactive
7:6	Not used
5	Self-test diagnostic error flag 1 = error condition 0 = normal operation
4	Angular rate over range 1 = error condition 0 = normal operation
3	SPI communications failure 1 = error condition 0 = normal operation
2	Control register update failed 1 = error condition 0 = normal operation
1	Power supply above 5.25 V 1 = above 5.25 V 0 = below 5.25 V (normal)
0	Power supply below 4.75 V 1 = below 4.75 V 0 = above 4.75 V (normal)

Flash Memory Endurance

The ENDURANCE register maintains a running count of writes to the flash memory. It provides up to 32,768 counts. Note that if this count is exceeded, the register wraps around, and goes back to zero, before beginning to increment again.

Table 29. ENDURANCE Register Definition

Address	Default	Format	Access
0x01, 0x00	N/A	Binary	Read-only

Alarms

The ADIS16251 provides two independent alarm options for event detection. Event detections occur when output register data meets the configured conditions. Configuration options are:

- All output data registers are available for monitoring as the source data.
- The source data can be filtered or unfiltered.
- Comparisons can be static or dynamic (rate of change).
- The threshold levels and times are configurable.
- Comparison can be greater than or less than.

The ALM_MAG1 register and the ALM_MAG2 register both establish the threshold level for detecting events. They take on the format of the source data and provide a bit for establishing the greater than/less than comparison direction. When making dynamic comparisons, the ALM_SMPL1 register and the ALM_SMPL2 register establish the number of averages taken for the source data as a reference for comparison. In this configuration, each subsequent source data sample is subtracted from the previous one, establishing an instantaneous delta. The rate of change calculation is

$$Y_C = \frac{1}{N_{DS}} \sum_{n=1}^{N_{DS}} y(n+1) - y(n)$$

$$Rate\ of\ change\ alarm \Rightarrow \text{is } Y_C > \text{or} < M_C\ ?$$

where:
N_{DS} is the number of samples in ALM_SMPL1/ALM_SMPL2.
$y(n)$ is the sampled output data.
M_C is the magnitude for comparison in ALM_MAG1/ALM_MAG2.
Y_C is the factor to be compared with M_C.
> or < is determined by the MSB in ALM_MAG1/ALM_MAG2.

The ALM_CTRL register controls the source data selection, static/dynamic selection, filtering selection, and digital I/O usage for the alarms.

Table 30. ALM_MAG1 Register Definition

Address	Default	Format	Access
0x21, 0x20	0x0000	N/A	R/W

Table 31. ALM_MAG1 Bit Descriptions

Bit	Description
15	Comparison polarity: 1 = greater than, 0 = less than
14	Not used
13:0	Data bits: format matches source data format

Table 32. ALM_SMPL1 Register Definition

Address	Default	Format	Access
0x25, 0x24	0x0000	Binary	R/W

Table 33. ALM_SMPL1 Bit Descriptions

Bit	Description
15:8	Not used
7:0	Data bits

Table 34. ALM_MAG2 Register Definition

Address	Default	Format	Access
0x23, 0x22	0x0000	N/A	R/W

Table 35. ALM_MAG2 Bit Descriptions

Bit	Description
15	Comparison polarity 1 = greater than 0 = less than
14	Not used
13:0	Data bits: format matches source data format

Table 36. ALM_SMPL2 Register Definition

Address	Default	Format	Access
0x27, 0x26	0x0000	Binary	R/W

Table 37. ALM_SMPL2 Bit Descriptions

Bit	Description
15:8	Not used
7:0	Data bits

Table 38. ALM_CTRL Register Definition

Address	Default	Format	Access
0x29, 0x28	0x0000	N/A	R/W

Table 39. ALM_CTRL Bit Descriptions

Bit	Value	Description
15		Rate of change (ROC) enable for Alarm 2 1 = rate of change 0 = static level
14:12		Alarm 2 source selection
	000	Disable
	001	Power supply output
	010	Gyroscope output
	011	Inactive
	100	Inactive
	101	Auxiliary ADC output
	110	Temperature sensor output
	111	Inactive
11		Rate of change (ROC) enable for Alarm 1 1 = rate of change 0 = static level
10:8		Alarm 1 source selection, same coding as Alarm 2, Bits [14:12]
7:5		Not used
4		Filtered data comparison 1 = filtered data 0 = unfiltered data
3		Not used
2		Alarm output enable 1 = enabled 0 = disabled
1		Alarm output polarity 1 = active high 0 = active low
0		Alarm output line select 1 = DIO2 0 = DIO1

SECOND-LEVEL ASSEMBLY

The ADIS16251 can be attached to the second-level assembly board using SN63 (or equivalent) or a Pb-free solder. Figure 20 and Table 40 provide acceptable solder reflow profiles for each solder type. Please note that these profiles may not be the optimum profile for the user's application. In no case should 260°C be exceeded. It is recommended that the user develop a reflow profile based upon the specific application.

In general, the lowest peak temperature and shortest dwell time above the melt temperature of the solder result in less shock and less stress to the product. In addition, evaluating the cooling rate and peak temperature can result in a more reliable assembly.

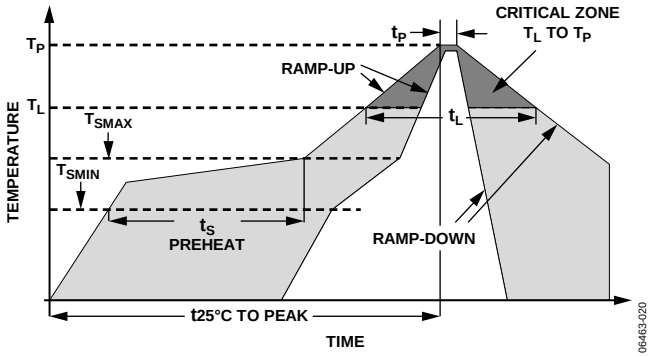

Figure 20. Acceptable Solder Reflow Profiles

Table 40. Acceptable Solder Reflow Profiles[1]

	Conditions	
Profile Feature	**Sn63/Pb37**	**Pb-Free**
Average Ramp Rate (T_L to T_P)	3°C/sec max	3°C/sec max
Preheat		
Minimum Temperature (T_{SMIN})	100°C	150°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time (Between T_{SMIN} to T_{SMAX}) (t_s)	60 sec to 120 sec	60 sec to 180 sec
T_{SMAX} to T_L		
Ramp-Up Rate	3°C/sec	3°C/sec
Time Maintained Above Liquidous Temperature (T_L)		
Liquidous Temperature (T_L)	183°C	217°C
Time (t_L)	60 sec to 150 sec	60 sec to 150 sec
Peak Temperature (T_P)	240°C + 0°C/−5°C	260°C + 0°C/−5°C
Time Within 5°C of Actual T_p	10 sec to 30 sec	20 sec to 40 sec
Ramp-Down Rate	6°C/sec max	6°C/sec max
Time 25°C to T_p	6 min max	8 min max

[1] Per IPC/JEDEC J-STD-020C.

OUTLINE DIMENSIONS

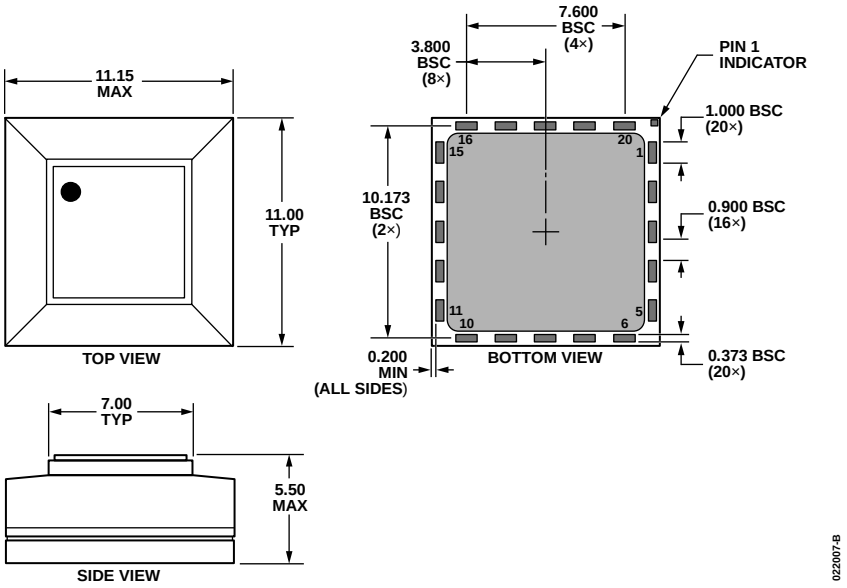

Figure 21. 20-Terminal Stacked Land Grid Array [LGA]
(CC-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADIS16251ACCZ[1]	−40°C to +85°C	20-Terminal Stacked Land Grid Array [LGA]	CC-20-1
ADIS16251/PCBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES

D06463-0-11/09(A)