Data Sheet | June 28, 2007 | FN6312.1

Dual and Quad Micropower Single Supply Rail-to-Rail Input and Output (RRIO) Precision Op Amp

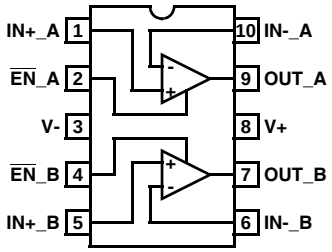
The ISL28286 and ISL28486 are dual and quad channel micropower operational amplifiers optimized for single supply operation over the 2.4V to 5V range. They can be operated from one lithium cell or two Ni-Cd batteries. For equivalent performance in a single channel op amp reference EL8186.

These devices feature an Input Range Enhancement Circuit (IREC) which enables them to maintain CMRR performance for input voltages 10% above the positive supply rail and down to the negative supply. The output operation is rail to rail.

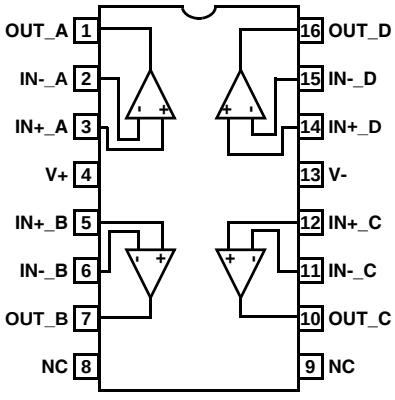
The ISL28286 and ISL28486 draw minimal supply current while meeting excellent DC-accuracy, AC-performance, noise and output drive specifications. The ISL28286 contains a power down enable pin that reduces the power supply current to less than 4µA max in the disabled state.

Pinouts

ISL28286
(10 LD MSOP)
TOP VIEW



ISL28486
(16 LD QSOP)
TOP VIEW



Features

- Low power 120µA typical supply current (ISL28286)
- 600µV maximum offset voltage
- 500pA typical input bias current
- 400kHz typical gain-bandwidth product
- 115dB typical PSRR and CMRR
- Single supply operation down to 2.4V
- Input is capable of swinging above V+ and to V- (ground sensing)
- Rail-to-rail input and output (RRIO)
- Pb-free plus anneal available (RoHS compliant)

Applications

- Battery- or solar-powered systems
- 4mA to 25mA current loops
- Handheld consumer products
- Medical devices
- Thermocouple amplifiers
- Photodiode pre-amps
- pH probe amplifiers

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL28286FUZ*	8286Z	10 Ld MSOP	MDP0043
ISL28486FAZ*	28486 FAZ	16 Ld QSOP	MDP0040

*Add “-T7” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage 5.5V
Supply Turn On Voltage Slew Rate 1V/µs
Differential Input Current 5mA
Differential Input Voltage 0.5V
Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
Output Short-Circuit Duration. . . . . Indefinite
ESD Rating
Human Body Model 3kV
Machine Model. 300V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
10 Ld MSOP Package	115
16 Ld QSOP Package	112

Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature Range . . . . . .-40°C to +125°C
Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . .+125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage		-600 **-650**	±20	600 **650**	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage vs Temperature			0.7		µV/°C
I_{OS}	Input Offset Current		-2.5 **-2.5**	±0.25	2.5 **2.5**	nA
I_B	Input Bias Current		-2 **-2.5**	±0.5	2 **2.5**	nA
CMIR	Common-Mode Voltage Range	Guaranteed by CMRR	**0**		**5**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	90 **80**	115		dB
PSRR	Power Supply Rejection Ratio	V_+ = 2.4V to 5V	90 **80**	115		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V, R_L = 100kΩ	275 **275**	500		V/mV
		V_O = 0.5V to 4.5V, R_L = 1kΩ		95		V/mV
V_{OUT}	Maximum Output Voltage Swing	Output low, R_L = 100kΩ		3	6 **30**	mV
		Output low, R_L = 1kΩ		130	175 **225**	mV
		Output high, R_L = 100kΩ	4.990 **4.970**	4.996		V
		Output high, R_L = 1kΩ	4.800 **4.750**	4.880		V
$I_{S,ON}$	Supply Current, Enabled	ISL28286, All channels enabled.		120	156 **175**	µA
		ISL28486, All channels enabled.		240	315 **350**	µA
$I_{S,OFF}$	Supply Current, Disabled	ISL28286, All channels disabled.		4	7 **9**	µA

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
$I_{SC}+$	Short Circuit Sourcing Capability	R_L = 10Ω	29 **23**	31		mA
$I_{SC}-$	Short Circuit Sinking Capability	R_L = 10Ω	24 **19**	26		mA
V_{SUPPLY}	Supply Operating Range	V_+ to V_-	**2.4**		**5**	V
$V_{\overline{ENH}}$	$\overline{EN}$ Pin High Level (ISL28286)		**2**			V
$V_{\overline{ENL}}$	$\overline{EN}$ Pin Low Level (ISL28286				**0.8**	V
$I_{\overline{ENH}}$	$\overline{EN}$ Pin Input High Current (ISL28286)	$V_{\overline{EN}}$ = V_+		0.7	1.3 **1.5**	µA
$I_{\overline{ENL}}$	$\overline{EN}$ Pin Input Low Current (ISL28286)	$V_{\overline{EN}}$ = V_-		0	**0.1**	µA
AC SPECIFICATONS						
GBW	Gain Bandwidth Product	A_V = 100, R_F = 100kΩ, R_G = 1kΩ, R_L = 10kΩ to V_{CM}		400		kHz
e_n	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz		4.5		$µV_{P-P}$
	Input Noise Voltage Density	f_O = 1kHz		50		nV/√Hz
i_n	Input Noise Current Density	f_O = 1kHz		0.18		pA/√Hz
CMRR @ 60Hz	Input Common Mode Rejection Ratio	V_{CM} = $1V_{P-P}$, R_L = 10kΩ to V_{CM}		78		dB
PSRR+ @ 120Hz	Power Supply Rejection Ratio (V_+)	V_+, V_- = ±12V and ±2.5V, V_{SOURCE} = $1V_{P-P}$, R_L = 10kΩ to V_{CM}		-105		dB
PSRR- @ 120Hz	Power Supply Rejection Ratio (V_-)	V_+, V_- = ±12V and ±2.5V V_{SOURCE} = $1V_{P-P}$, R_L = 10kΩ to V_{CM}		-73		dB
TRANSIENT RESPONSE						
SR	Slew Rate		±0.10 ±**0.09**	±0.17	±0.20 ±**0.25**	V/µs
$t_{\overline{EN}}$	Enable to Output Turn-on Delay Time, 10% $\overline{EN}$ to 10% V_{OUT}, (ISL28286)	$V_{\overline{EN}}$ = 5V to 0V, A_V = -1, R_g = R_f = R_L = 1k to V_{CM}		2		µs
	Enable to Output Turn-off Delay Time, 10% $\overline{EN}$ to 10% V_{OUT}, (ISL28286)	$V_{\overline{EN}}$ = 0V to 5V, A_V = -1, R_g = R_f = R_L = 1k to V_{CM}		0.1		µs

NOTE:

1. Parts are 100% tested at +25°C. Over temperature limits established by characterization and are not production tested.

Typical Performance Curves $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open$

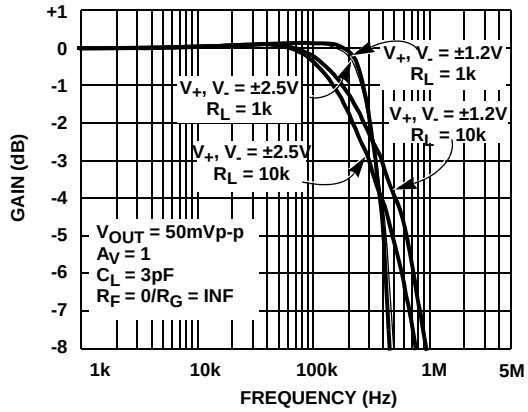


FIGURE 1. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

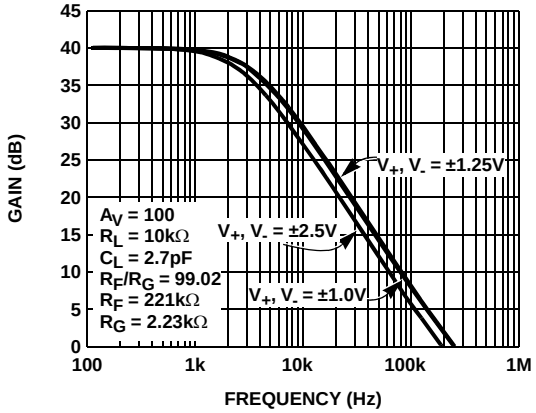


FIGURE 2. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

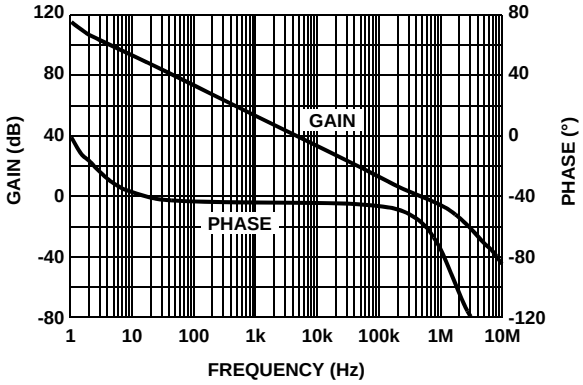


FIGURE 3. A_{VOL} vs FREQUENCY @ 100kΩ LOAD

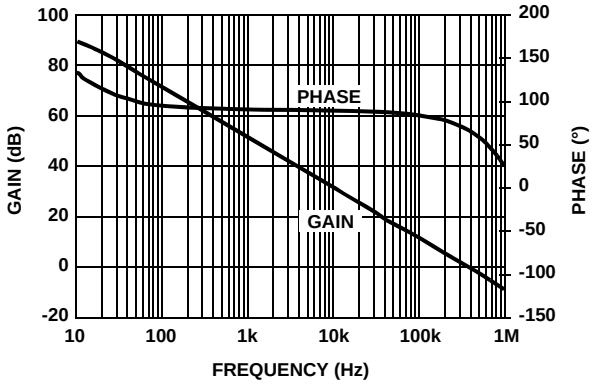


FIGURE 4. A_{VOL} vs FREQUENCY @ 1kΩ LOAD

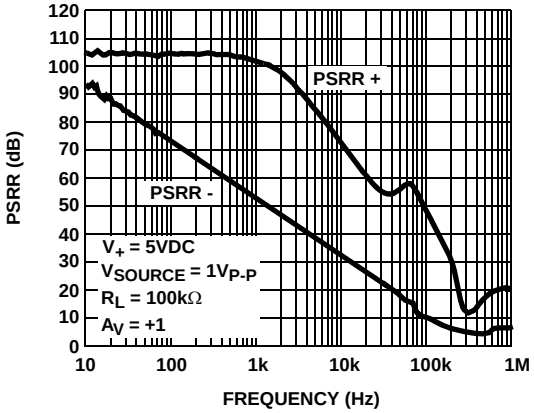


FIGURE 5. PSRR vs FREQUENCY

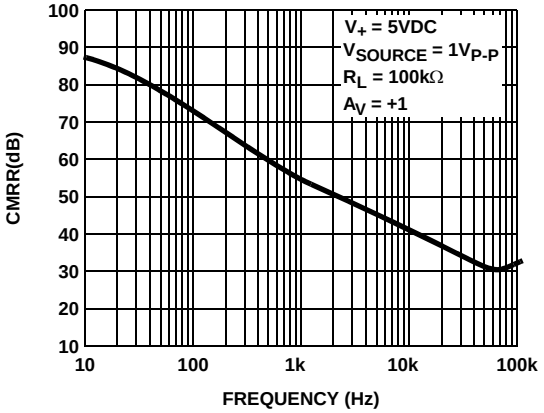


FIGURE 6. CMRR vs FREQUENCY

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

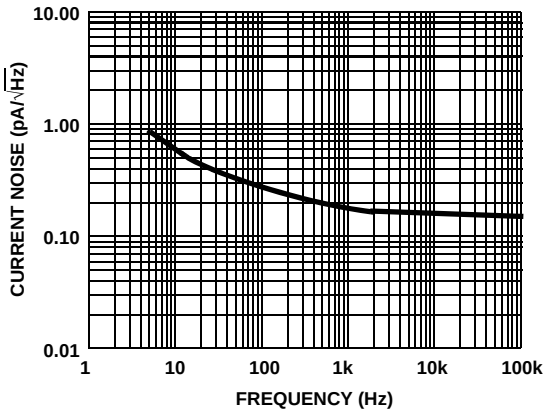


FIGURE 7. CURRENT NOISE vs FREQUENCY

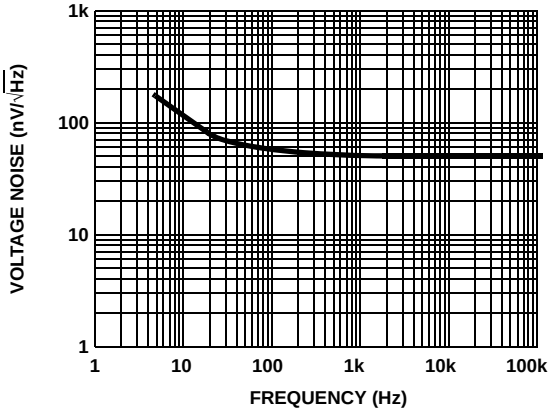


FIGURE 8. VOLTAGE NOISE vs FREQUENCY

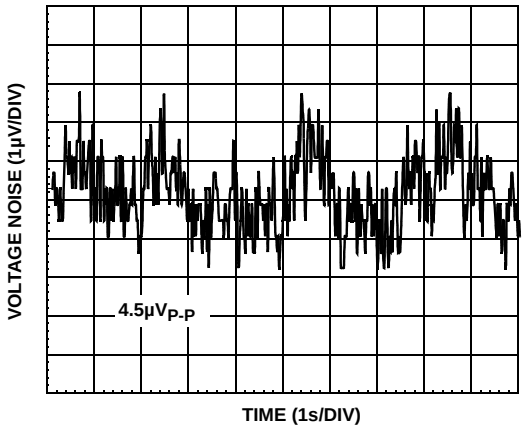


FIGURE 9. 0.1Hz TO 10Hz INPUT VOLTAGE NOISE

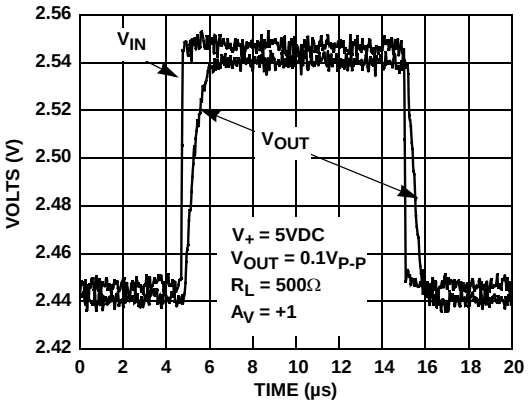


FIGURE 10. SMALL SIGNAL TRANSIENT RESPONSE

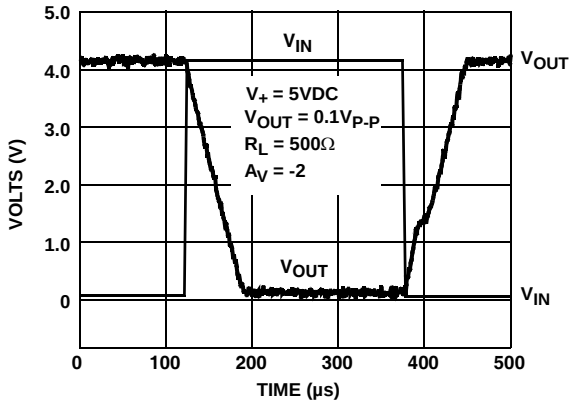


FIGURE 11. LARGE SIGNAL TRANSIENT RESPONSE

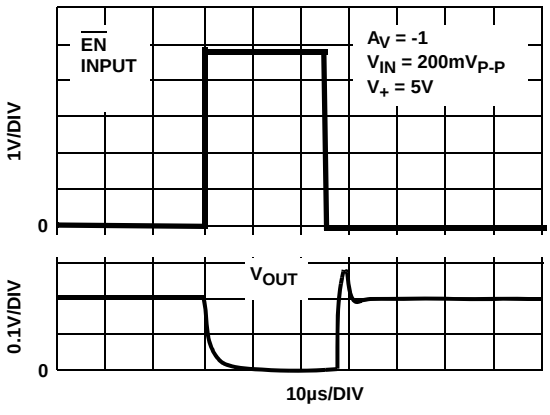


FIGURE 12. ENABLE TO OUTPUT DELAY TIME

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

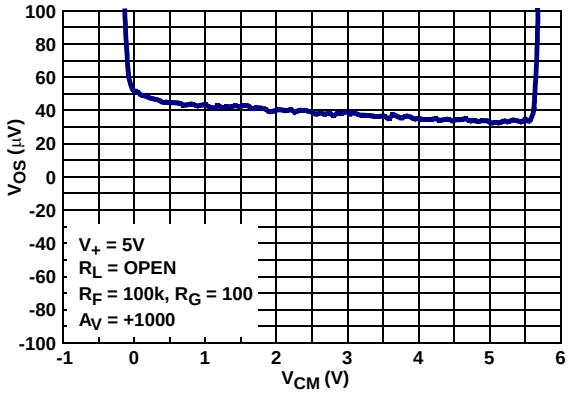


FIGURE 13. INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

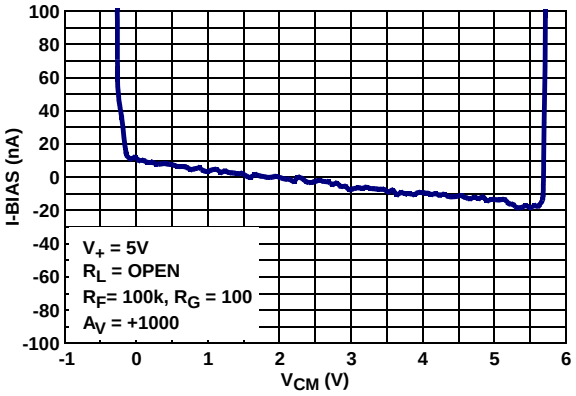


FIGURE 14. INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

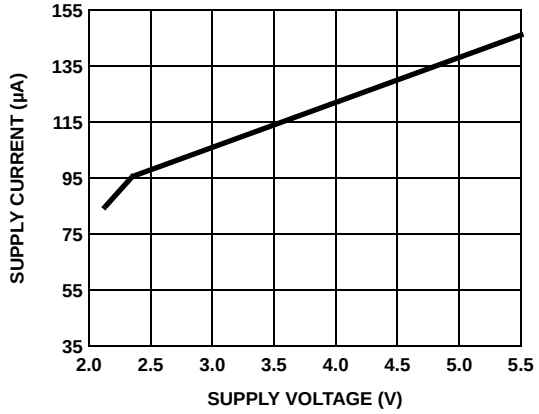


FIGURE 15. ISL28286 SUPPLY CURRENT vs SUPPLY VOLTAGE

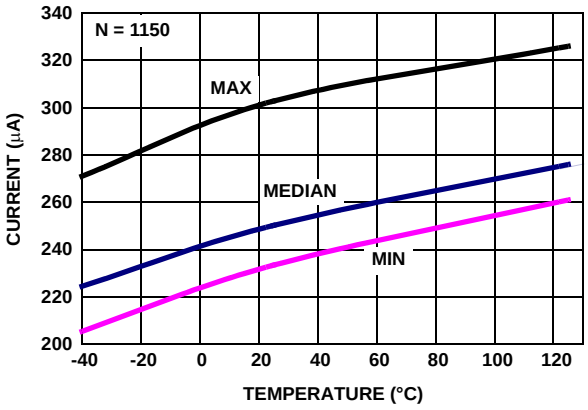


FIGURE 16. ISL28486 SUPPLY CURRENT vs TEMPERATURE, V_+, V_- = ±2.5V ENABLED, R_L = INF

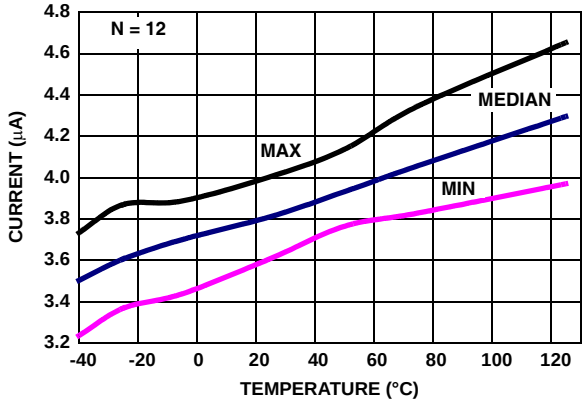


FIGURE 17. ISL28286 SUPPLY CURRENT vs TEMPERATURE, V_+, V_- = ±2.5V DISABLED, R_L = INF

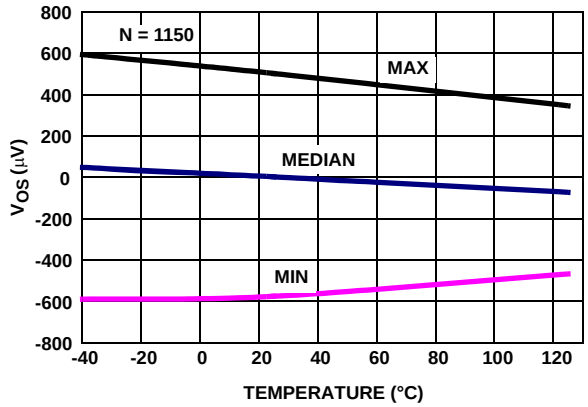


FIGURE 18. V_{OS} vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±2.5V

Typical Performance Curves $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

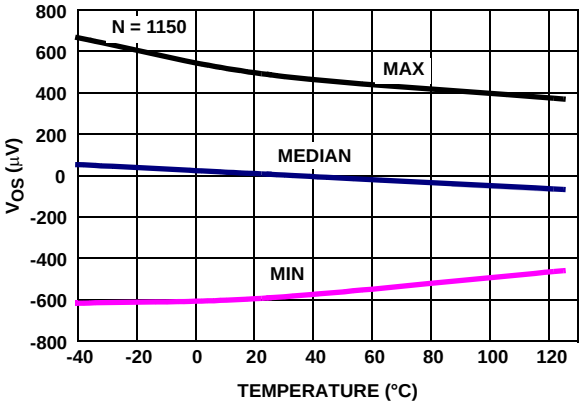


FIGURE 19. V_{OS} vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±1.2V

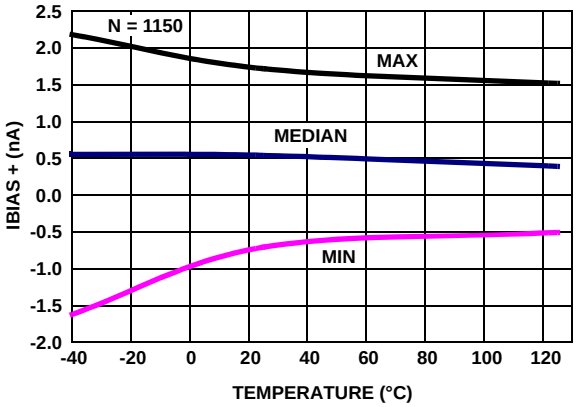


FIGURE 20. IBIAS + vs TEMPERATURE, V_+, V_- = ±2.5V

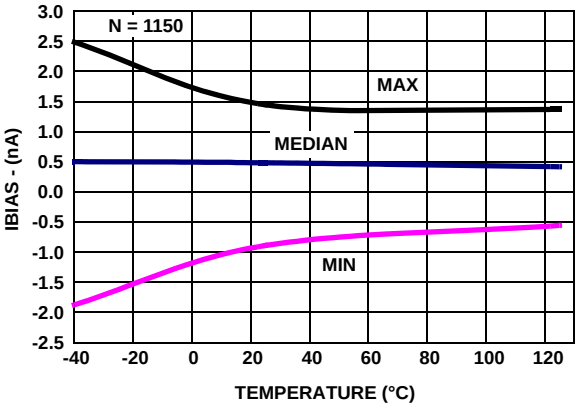


FIGURE 21. IBIAS - vs TEMPERATURE, V_+, V_- = ±2.5V

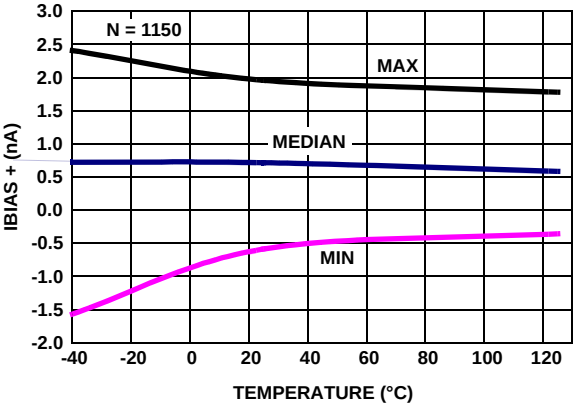


FIGURE 22. IBIAS + vs TEMPERATURE, V_+, V_- = ±1.2V

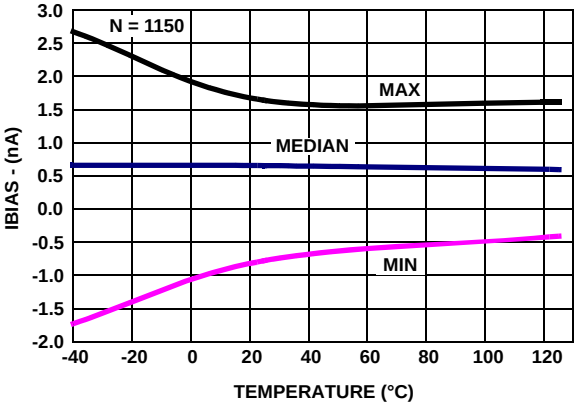


FIGURE 23. IBIAS - vs TEMPERATURE, V_+, V_- = ±1.2V

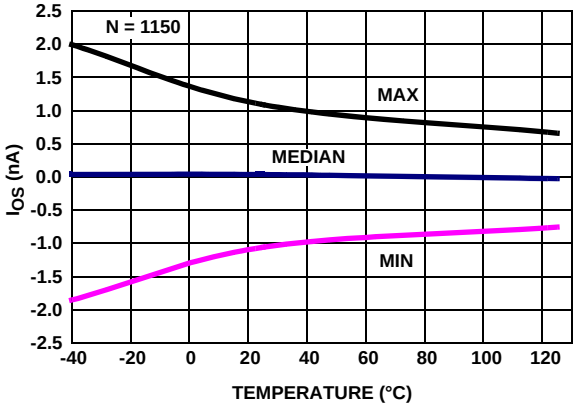


FIGURE 24. I_{OS} vs TEMPERATURE, V_+, V_- = ±2.5V

Typical Performance Curves $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

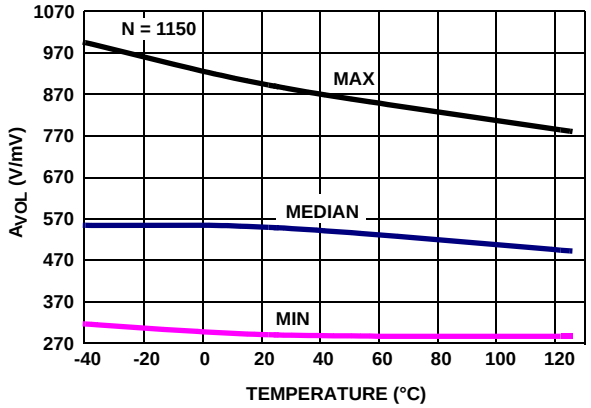


FIGURE 25. A_{VOL} vs TEMPERATURE, $V_+, V_- = \pm 2.5V, R_L = 100k$

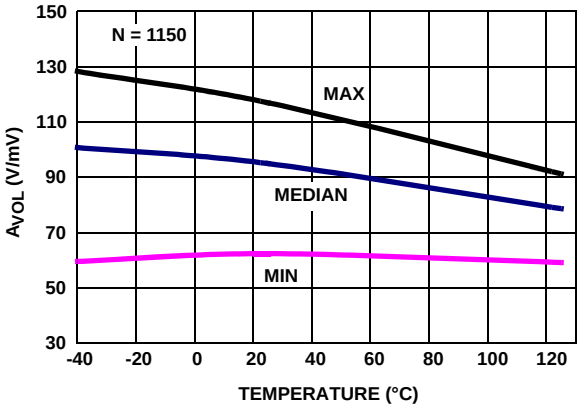


FIGURE 26. A_{VOL} vs TEMPERATURE, $V_+, V_- = \pm 2.5V, R_L = 1k$

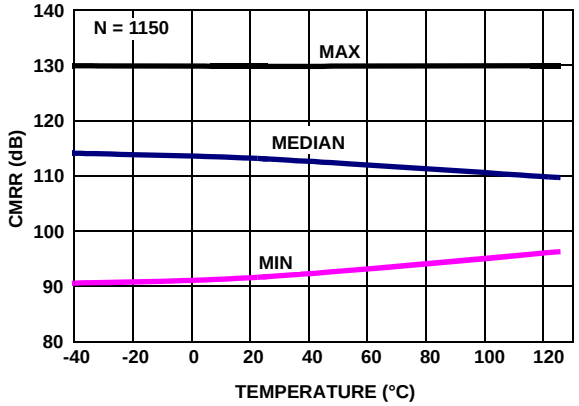


FIGURE 27. CMRR vs TEMPERATURE, V_{CM} = +2.5V TO -2.5V, $V_+, V_- = \pm 2.5V$

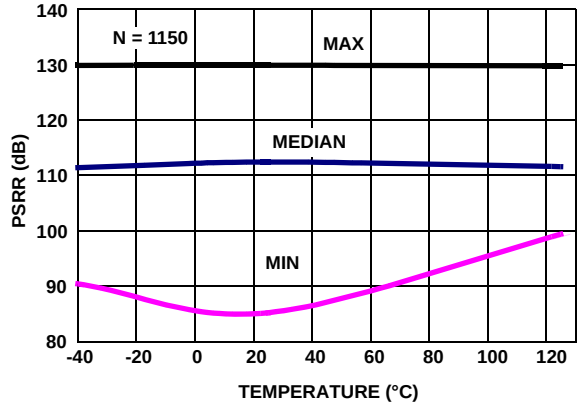


FIGURE 28. PSRR vs TEMPERATURE, $V_+, V_- = \pm 1.2V$ TO $\pm 2.75V$

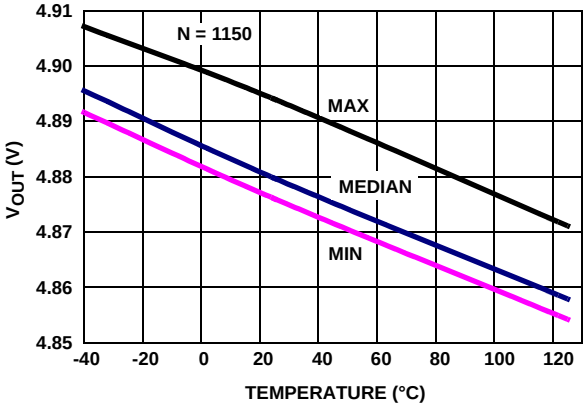


FIGURE 29. V_{OUT} HIGH vs TEMPERATURE, $V_+, V_- = \pm 2.5V$, $R_L = 1k$

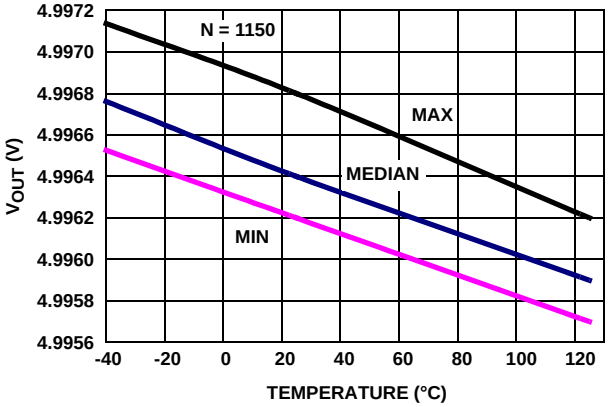


FIGURE 30. V_{OUT} HIGH vs TEMPERATURE, $V_+, V_- = \pm 2.5V$, $R_L = 100k$

Typical Performance Curves $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L$ = Open **(Continued)**

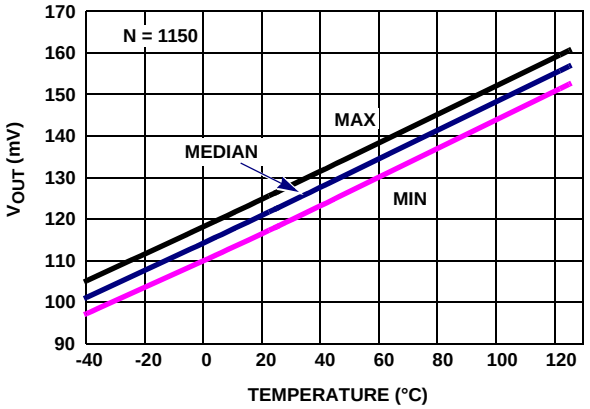


FIGURE 31. V_{OUT} LOW vs TEMPERATURE, $V_+, V_- = \pm 2.5V$, $R_L = 1k$

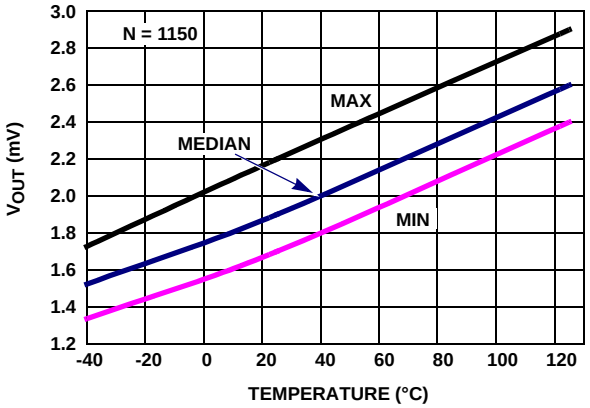


FIGURE 32. V_{OUT} LOW vs TEMPERATURE, $V_+, V_- = \pm 2.5V$, $R_L = 100k$

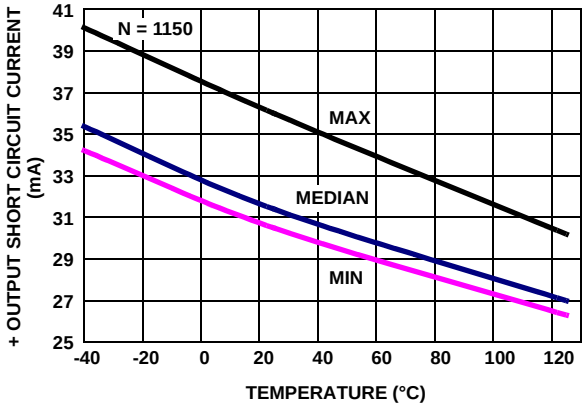


FIGURE 33. + OUTPUT SHORT CIRCUIT CURRENT vs TEMPERATURE, $V_{IN} = -2.55V, R_L = 10$, $V_+, V_- = \pm 2.5V$

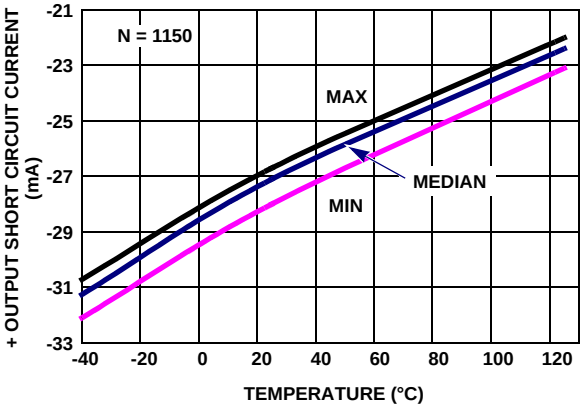


FIGURE 34. - OUTPUT SHORT CIRCUIT CURRENT vs TEMPERATURE, $V_{IN} = -2.55V, R_L = 10$, $V_+, V_- = \pm 2.5V$

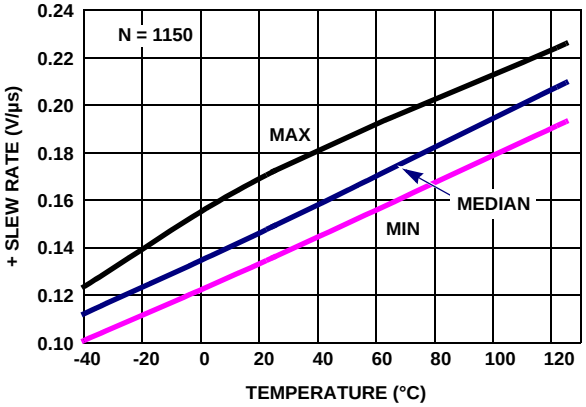


FIGURE 35. + SLEW RATE vs TEMPERATURE, $V_{OUT} = 1.5V$, $A_V = +2$

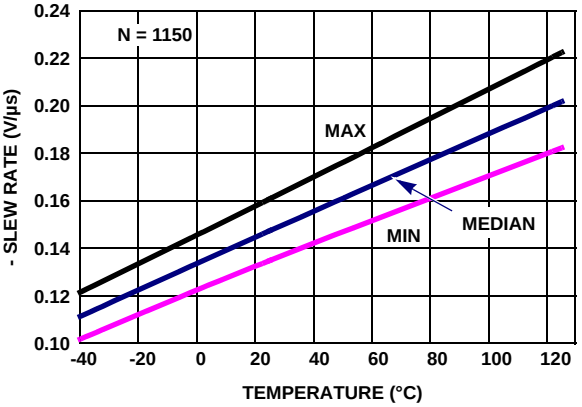
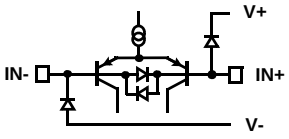


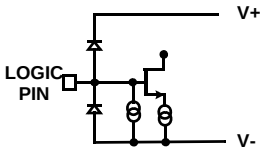
FIGURE 36. - SLEW RATE vs TEMPERATURE, $V_{OUT} = 1.5V$, $A_V = +2$

Pin Descriptions

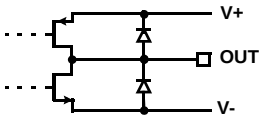
ISL28286 (10 LD MSOP)	ISL28486 (16 LD QSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	3	IN+_A	Circuit 1	Amplifier A non-inverting input
2		$\overline{EN}$_A	Circuit 2	Amplifier A enable pin internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.
3	13	V-	Circuit 4	Negative power supply
4		$\overline{EN}$_B	Circuit 2	Amplifier B enable pin with internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.
5	5	IN+_B	Circuit 1	Amplifier B non-inverting input
6	6	IN-_B	Circuit 1	Amplifier B inverting input
7	7	OUT_B	Circuit 3	Amplifier B output
8	4	V+	Circuit 4	Positive power supply
9	1	OUT_A	Circuit 3	Amplifier A output
10	2	IN-_A	Circuit 1	Amplifier A inverting input
	10	OUT_C	Circuit 3	Amplifier C output
	11	IN-_C	Circuit 1	Amplifier C inverting input
	12	IN+_C	Circuit 1	Amplifier C non-inverting input
	14	IN+_D	Circuit 1	Amplifier D non-inverting input
	15	IN-_D	Circuit 1	Amplifier D inverting input
	16	OUT_D	Circuit 3	Amplifier D output
	8, 9	NC	-	No internal connection



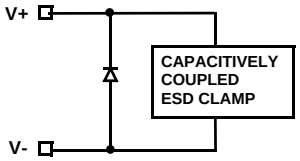
CIRCUIT 1



CIRCUIT 2



CIRCUIT 3



CIRCUIT 4

Applications Information

Introduction

The ISL28286 and ISL28486 are dual and quad BiCMOS rail-to-rail input, output (RRIO) micropower precision operational amplifiers. These devices are designed to operate from a single supply (2.4V to 5.0V) or dual supplies (±1.2V to ±2.5V) while drawing only 120µA (ISL28286) of supply current. This combination of low power and precision performance makes these devices suitable for solar and battery power applications.

Rail-to-Rail Input

Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The ISL28286 and ISL28486 achieve input rail-to-rail without sacrificing important precision specifications and degrading distortion performance. The devices' input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range gives us an undistorted behavior from typically down to the negative rail to 10% higher than the V+ rail (0.5V higher than V+ when V+ equals 5V).

Input Protection

All input terminals have internal ESD protection diodes to positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. Both parts have additional back-to-back diodes across the input terminals. If overdriving the inputs is necessary, the external input current must never exceed 5mA. External series resistors may be used as an external protection to limit excessive external voltage and current from damaging the inputs.

Input Bias Current Compensation

The ISL28286 and ISL28486 contain an input bias cancellation circuit which reduces the bias currents down to a typical of 500pA while maintaining an excellent bandwidth for a micro-power operational amplifier. The input stage transistors are still biased with adequate current for speed but the canceling circuit sinks most of the base current, leaving a small fraction as input bias current.

Rail-to-Rail Output

A pair of complementary MOSFET devices are used to achieve the rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. Both parts with a 100kΩ load will swing to within 4mV of the supply rails.

Enable/Disable Feature

The ISL28286 offers two $\overline{EN}$ pins ($\overline{EN}$_A and $\overline{EN}$_B) which disable the op amp when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part consumes typically 4µA. By disabling the part, multiple parts can be connected together as a MUX. The outputs are tied together in parallel and a channel can be selected by the $\overline{EN}$ pins. The $\overline{EN}$ pins also have an internal pull-down. If left open, the $\overline{EN}$ pins will pull to the negative rail and the op amp will be enabled by default.

Using Only One Channel

The ISL28286 and ISL28486 are dual and quad channel op amps. If the application only requires one channel when using the ISL28286 or less than 4 channels when using the ISL28486, the user must configure the unused channel(s) to prevent them from oscillating. The unused channel(s) will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 37).

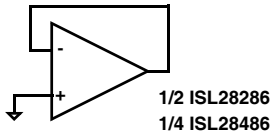


FIGURE 37. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance and low offset voltage of the ISL28286 and ISL28486, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. When input leakage current is a concern, the use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 38 shows a guard ring example for a unity gain amplifier that uses the low impedance amplifier output at the same voltage as the high impedance input to eliminate surface leakage. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.

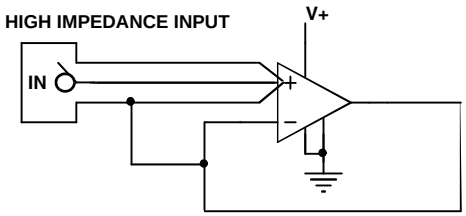


FIGURE 38. GUARD RING EXAMPLE FOR UNITY GAIN AMPLIFIER

Current Limiting

The ISL28286 and ISL28486 have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

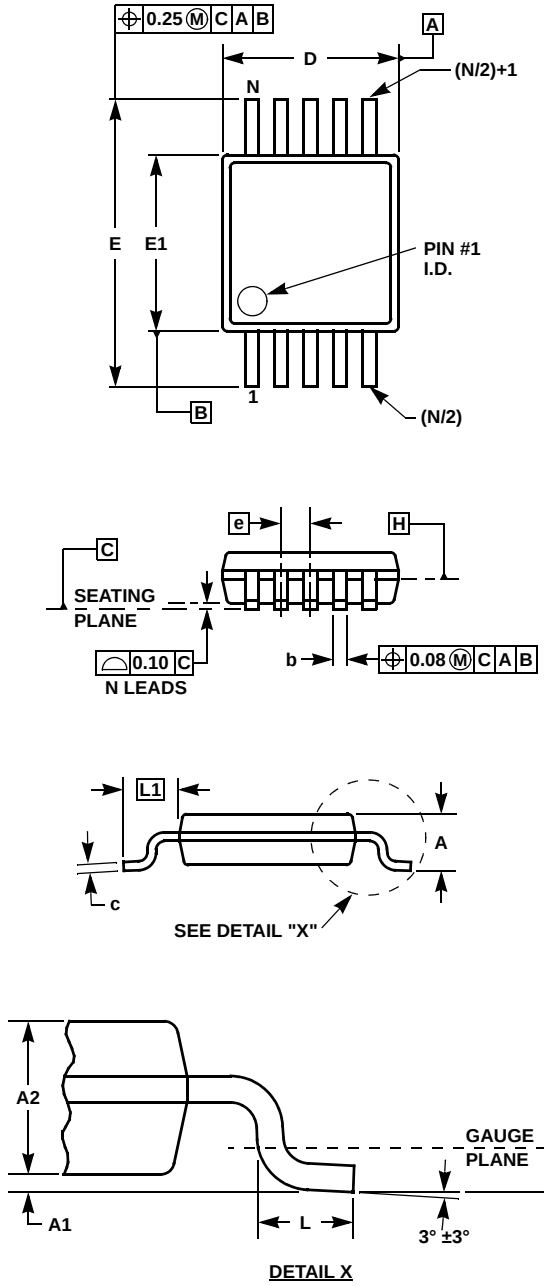
- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated as follows:

$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage (Magnitude of V_+ and V_-)
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

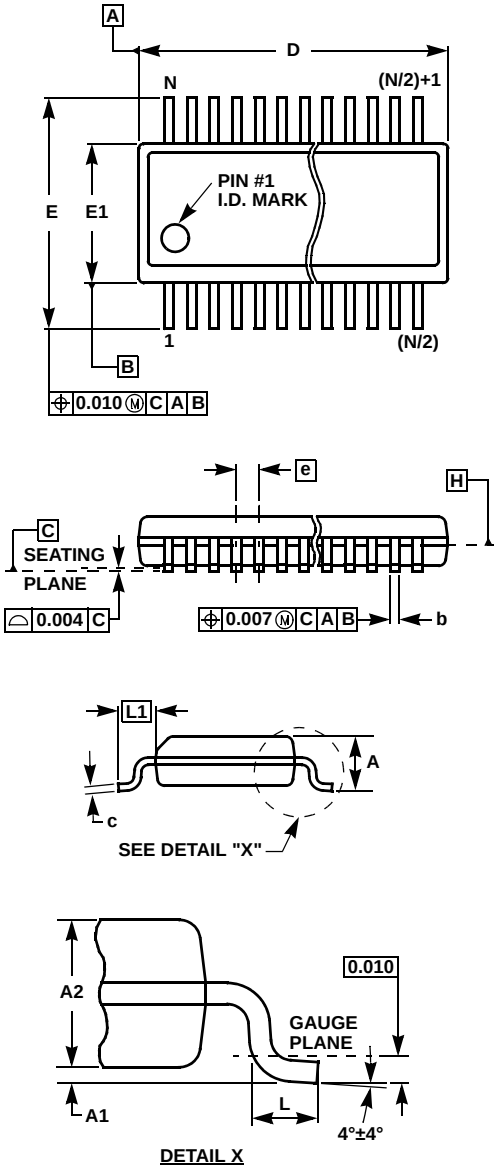
SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

SYMBOL	INCHES			TOLERANCE	NOTES
	QSOP16	QSOP24	QSOP28		
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.