## Single and Dual Single Supply Ultra-Low Noise, Low Distortion Rail-to-Rail Output, Op Amp

The ISL28191 and ISL28291 are tiny single and dual ultra-low noise, ultra-low distortion operational amplifiers. They are fully specified to operate down to +3 V single supply. These amplifiers have outputs that swing rail-to-rail and an input common mode voltage that extends to ground (ground sensing).

The ISL28191 and ISL28291 are unity gain stable with an input referred voltage noise of $1.7 \mathrm{nV} / \sqrt{ } \mathrm{Hz}$. Both parts feature $0.00018 \% \mathrm{THD}+\mathrm{N}$ at 1 kHz .

The ISL28191 is available in the space-saving 6 Ld $\mu$ TDFN ( $1.6 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ ) and 6 Ld SOT-23 packages. The ISL28291 is available in the 8 Ld SOIC, 10 Ld $1.8 \mathrm{~mm} \times 1.4 \mathrm{~mm} \mu$ TQFN and 10 Ld MSOP packages. All devices are guaranteed over $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.

## Ordering Information

| PART <br> NUMBER | PART <br> MARKING | PACKAGE <br> (Pb-free) | PKG. <br> DWG. \# |
| :--- | :--- | :--- | :--- |
| ISL28191FHZ-T7* (Note 1) | GABJ | 6 Ld SOT-23 | MDP0038 |
| ISL28191FRUZ-T7* (Note 2) | M8 | 6 Ld $\mu$ TDFN | L6.1.6x1.6A |
| ISL28291FUZ (Note 1) | $8291 Z$ | 10 Ld MSOP | MDP0043 |
| ISL28291FUZ-T7* (Note 1) | $8291 Z$ | 10 Ld MSOP | MDP0043 |
| ISL28291FBZ (Note 1) | 28291 FBZ | 8 Ld SOIC | MDP0027 |
| ISL28291FBZ-T7 (Note 1) | 28291 FBZ | 8 Ld SOIC | MDP0027 |
| ISL28291FRUZ-T7* (Note 2) | F | 10 Ld $\mu$ TQFN | L10.1.8x1.4A |
| ISL28291EVAL1Z | Evaluation Board |  |  |

*Please refer to TB347 for details on reel specifications.
NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb -free material sets, molding compounds/die attach materials, and $100 \%$ matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb -free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb free requirements of IPC/JEDEC J STD-020.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb -free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Features

- $1.7 \mathrm{nV} / \sqrt{ } \mathrm{Hz}$ input voltage noise at 1 kHz
- 1 kHz THD+N typical $0.00018 \%$ at $2 \mathrm{~V}_{\mathrm{P}-\mathrm{P}} \mathrm{V}_{\text {OUT }}$
- Harmonic Distortion $-76 \mathrm{dBc},-70 \mathrm{dBc}, \mathrm{f}_{\mathrm{O}}=1 \mathrm{MHz}$
- 61 MHz -3dB bandwidth
- $630 \mu \mathrm{~V}$ maximum offset voltage
- $3 \mu \mathrm{~A}$ input bias current
- 100dB typical CMRR
- 3 V to 5.5 V single supply voltage range
- Rail-to-rail output
- Ground Sensing
- Enable pin (not available in the 8 Ld SOIC package option)
- Pb-free (RoHS compliant)


## Applications

- Low noise signal processing
- Low noise microphones/preamplifiers
- ADC buffers
- DAC output amplifiers
- Digital scales
- Strain gauges/sensor amplifiers
- Radio systems
- Portable equipment
- Infrared detectors


## Pinouts



| Absolute Maximum Ratings ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ ) |  |
| :---: | :---: |
| Supply Voltage. | 5.5 V |
| Supply Turn On Voltage Slew Rate | 1V/us |
| Differential Input Current | 5mA |
| Differential Input Voltage | 0.5 V |
| Input Voltage | V- -0.5V to V+ + 0.5V |
| ESD Tolerance |  |
| Human Body Model | .3kV |
| Machine Model. | . 300 V |
| Charged Device Model (CDM) | 1200 V |

## Thermal Information

| Thermal Resistance (Typical, Note ) | $\theta_{\mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ |
| :---: | :---: |
| 6 Ld SOT-23 Package | 230 |
| 6 Ld $\mu$ TDFN Package | 125 |
| 8 Ld SO Package. | 125 |
| 10 Ld MSOP Package | 150 |
| 10 Ld $\mu$ TQFN Package | 180 |
| Ambient Operating Temperature Range | . $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Storage Temperature Range | . $65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Operating Junction Temperature | $+125^{\circ} \mathrm{C}$ |
| Pb -free reflow profile http://www.intersil.com/pbfree/Pb-Fr | .see link below |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:
3. $\theta_{\mathrm{JA}}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_{J}=T_{C}=T_{A}$

Electrical Specifications $\quad V+=5.0 \mathrm{~V}, \mathrm{~V}-=G N D, R_{L}=O p e n, R_{F}=1 k \Omega, A_{V}=-1$ unless otherwise specified. Parameters are per amplifier. Typical values are at $\mathrm{V}+=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. Boldface limits apply over the operating temperature range, $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, temperature data guaranteed by characterization.

| PARAMETER | DESCRIPTION | CONDITIONS | $\begin{gathered} \text { MIN } \\ \text { (Note 4) } \end{gathered}$ | TYP | $\begin{gathered} \text { MAX } \\ \text { (Note 4) } \end{gathered}$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DC SPECIFICATIONS |  |  |  |  |  |  |
| Vos | Input Offset Voltage |  |  | 270 | $\begin{aligned} & 630 \\ & 840 \end{aligned}$ | $\mu \mathrm{V}$ |
| $\frac{\Delta \mathrm{V}_{\mathrm{OS}}}{\Delta \mathrm{~T}}$ | Input Offset Drift vs Temperature | Figure 21 |  | 3.1 |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{l}_{1}$ | Input Offset Current |  |  | 35 | $\begin{aligned} & 500 \\ & 900 \end{aligned}$ | nA |
| $\mathrm{I}_{\mathrm{B}}$ | Input Bias Current |  |  | 3 | $\begin{aligned} & 6 \\ & 7 \end{aligned}$ | $\mu \mathrm{A}$ |
| CMIR | Common-Mode Input Range |  | 0 |  | 3.8 | V |
| CMRR | Common-Mode Rejection Ratio | $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ to 3.8 V | 78 | 100 |  | dB |
| PSRR | Power Supply Rejection Ratio | $\mathrm{V}_{\mathrm{S}}=3 \mathrm{~V}$ to 5 V | 74 | 80 |  | dB |
| Avol | Large Signal Voltage Gain | $\mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V}$ to $4 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ | $\begin{aligned} & 90 \\ & 86 \end{aligned}$ | 98 |  | dB |
| V OUT | Maximum Output Voltage Swing | Output low, $\mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ |  | 20 | $\begin{aligned} & 50 \\ & 80 \end{aligned}$ | mV |
|  |  | Output high, $\mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega, \mathrm{V}+=5 \mathrm{~V}$ | $\begin{aligned} & 4.95 \\ & 4.92 \end{aligned}$ | 4.97 |  | V |
| $\mathrm{I}_{\mathrm{S}, \mathrm{ON}}$ | Supply Current per Amplifier, Enabled |  |  | 2.6 | $\begin{aligned} & 3.5 \\ & 3.9 \end{aligned}$ | mA |
| Is, OFF | Supply Current per Amplifier, Disabled |  |  | 26 | $\begin{aligned} & 35 \\ & 48 \end{aligned}$ | $\mu \mathrm{A}$ |
| ${ }^{1}{ }^{+}$ | Short-Circuit Output Current | $R_{L}=10 \Omega$ | $\begin{aligned} & 95 \\ & 90 \end{aligned}$ | 130 |  | mA |
| $\mathrm{I}^{-}$ | Short-Circuit Output Current | $\mathrm{R}_{\mathrm{L}}=10 \Omega$ | $\begin{aligned} & 95 \\ & 90 \end{aligned}$ | 130 |  | mA |
| V SUPPLY | Supply Operating Range | V+ to V- | 3 |  | 5.5 | V |
| $\mathrm{V}_{\text {ENH }}$ | $\overline{\mathrm{EN}}$ High Level | Referred to V- | 2 |  |  | V |

## Electrical Specifications

$\mathrm{V}+=5.0 \mathrm{~V}, \mathrm{~V}-=\mathrm{GND}, \mathrm{R}_{\mathrm{L}}=$ Open, $\mathrm{R}_{\mathrm{F}}=1 \mathrm{k} \Omega, \mathrm{A}_{\mathrm{V}}=-1$ unless otherwise specified. Parameters are per amplifier. Typical values are at $\mathrm{V}+=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. Boldface limits apply over the operating temperature range, $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, temperature data guaranteed by characterization. (Continued)

| PARAMETER | DESCRIPTION | MIN <br> (Note 4) | TYP | MAX <br> (Note 4) | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |

## AC SPECIFICATIONS

| GBW | -3dB Unity Gain Bandwidth | $\mathrm{R}_{\mathrm{F}}=0 \Omega, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF}, \mathrm{A}_{\mathrm{V}}=1, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ |  | 61 | MHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| THD +N | Total Harmonic Distortion + Noise | $\mathrm{f}=1 \mathrm{kHz} . \mathrm{V}_{\text {OUT }}+2 \mathrm{~V}_{\text {P-P, }}, A_{V}=+1, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$ |  | 0.00018 | \% |
| $\begin{array}{\|l} \mathrm{HD} \\ (1 \mathrm{MHz}) \end{array}$ | 2nd Harmonic Distortion | $2 \mathrm{~V}_{\mathrm{P}-\mathrm{P}}$ output voltage, $\mathrm{A}_{\mathrm{V}}=1$ |  | -76 | dBc |
|  | 3rd Harmonic Distortion |  |  | -70 | dBc |
| ISO | Off-state Isolation $\mathrm{f}_{\mathrm{O}}=100 \mathrm{kHz}$ | $\begin{aligned} & A_{V}=+1, V_{I N}=100 \mathrm{mV}_{\mathrm{P}-\mathrm{P},} \mathrm{R}_{\mathrm{F}}=0 \Omega \\ & \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF}, A_{\mathrm{V}}=1, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \end{aligned}$ |  | -38 | dB |
| $\begin{aligned} & \text { X-TALK } \\ & \text { ISL28291 } \end{aligned}$ | Channel-to-Channel Crosstalk $\mathrm{f}_{\mathrm{O}}=100 \mathrm{kHz}$ | $\begin{aligned} & V_{S}= \pm 2.5 \mathrm{~V}, A_{V}=+1, V_{I N}=1 V_{P-P} \\ & R_{F}=0 \Omega, C_{L}=20 \mathrm{pF}, A_{V}=1, R_{L}=10 k \Omega \end{aligned}$ |  | -105 | dB |
| PSRR | Power Supply Rejection Ratio $\mathrm{f}_{\mathrm{O}}=100 \mathrm{kHz}$ | $\begin{aligned} & V_{S}= \pm 2.5 \mathrm{~V}, A_{V}=+1, V_{\text {SOURCE }}=1 V_{P-P}, \\ & R_{F}=0 \Omega, C_{L}=20 \mathrm{pF}, A_{V}=1, R_{L}=10 \mathrm{k} \Omega \end{aligned}$ |  | -70 | dB |
| CMRR | Common Mode Rejection Ratio $\mathrm{f}_{\mathrm{O}}=100 \mathrm{kHz}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{S}}= \pm 2.5 \mathrm{~V}, \mathrm{~A}_{\mathrm{V}}=+1, \mathrm{~V}_{\mathrm{CM}}=1 \mathrm{~V}_{\mathrm{P}-\mathrm{P},} \\ & \mathrm{R}_{\mathrm{F}}=0 \Omega, \mathrm{C}_{\mathrm{L}}=20 \mathrm{pF}, \mathrm{~A}_{\mathrm{V}}=1, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \end{aligned}$ |  | -65 | dB |
| $\mathrm{e}_{\mathrm{n}}$ | Input Referred Voltage Noise | $\mathrm{f}_{\mathrm{O}}=1 \mathrm{kHz}$ |  | 1.7 | $\mathrm{nV} / \mathrm{VHz}$ |
| $\mathrm{i}_{\mathrm{n}}$ | Input Referred Current Noise | $\mathrm{f}_{\mathrm{O}}=1 \mathrm{kHz}$ |  | 1.8 | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |
| TRANSIENT RESPONSE |  |  |  |  |  |
| SR | Slew Rate |  | $\begin{aligned} & 12 \\ & 12 \end{aligned}$ | 17 | V/us |
| $\mathrm{t}_{\mathrm{r},} \mathrm{t}_{\mathrm{f}}$, Small Signal | Rise Time, $\mathrm{t}_{\mathrm{r}} 10 \%$ to 90\% | $A_{V}=1, V_{O U T}=0.1 V_{P-P,} R_{L}=10 \mathrm{k} \Omega, C_{L}=1.2 \mathrm{pF}$ |  | 7 | ns |
|  | Fall Time, $\mathrm{t}_{\mathrm{f}} 90 \%$ to $10 \%$ |  |  | 12 | ns |
| $t_{r}, t_{f}$ Large Signal | Rise Time, $\mathrm{t}_{\mathrm{r}} 10 \%$ to $90 \%$ | $\begin{aligned} & A_{V}=2, V_{O U T}=1 V_{P-P} ; R_{L}=10 k \Omega, \\ & R_{F} / R_{G}=499 \Omega / 499 \Omega, C_{L}=1.2 \mathrm{pF} \end{aligned}$ |  | 44 | ns |
|  | Fall Time, $\mathrm{t}_{\mathrm{f}} 90 \%$ to $10 \%$ |  |  | 50 | ns |
|  | Rise Time, $\mathrm{t}_{\mathrm{r}} 10 \%$ to $90 \%$ | $\begin{aligned} & A_{V}=2, V_{O U T}=4.7 \mathrm{~V}_{\mathrm{P}-\mathrm{P}} ; \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \\ & \mathrm{R}_{\mathrm{F}} / \mathrm{R}_{\mathrm{G}}=499 \Omega / 499 \Omega, \mathrm{C}_{\mathrm{L}}=1.2 \mathrm{pF} \end{aligned}$ |  | 190 | ns |
|  | Fall Time, $\mathrm{t}_{\mathrm{f}} 90 \%$ to $10 \%$ |  |  | 190 | ns |
| t $\overline{\text { EN }}$ | ENABLE to Output Turn-on Delay Time; $10 \% \overline{\mathrm{EN}}-10 \% \mathrm{~V}_{\text {OUT }}$ | $A_{V}=1, V_{\text {OUT }}=1 \mathrm{VDC}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=1.2 \mathrm{pF}$ |  | 330 | ns |
|  | ENABLE to Output Turn-off Delay Time; $10 \%$ EN $-10 \% V_{\text {OUT }}$ | $A_{V}=1, V_{\text {OUT }}=0 \mathrm{VDC}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=1.2 \mathrm{pF}$ |  | 50 | ns |

NOTE:
4. Parameters with MIN and/or MAX limits are $100 \%$ tested at $+25^{\circ} \mathrm{C}$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

## Typical Performance Curves



FIGURE 1. GAIN vs FREQUENCY FOR VARIOUS RLOAD


FIGURE 3. -3dB BANDWIDTH vs VOUT


FIGURE 5. INPUT IMPEDANCE vs FREQUENCY


FIGURE 2. GAIN vs FREQUENCY FOR VARIOUS CLOAD


FIGURE 4. FREQUENCY RESPONSE vs CLOSED LOOP GAIN


FIGURE 6. DISABLED OUTPUT IMPEDANCE vs FREQUENCY

Typical Performance Curves (Continued)


FIGURE 7. ENABLED OUTPUT IMPEDANCE vs FREQUENCY


FIGURE 9. PSRR vs FREQUENCY


FIGURE 11. CHANNEL TO CHANNEL CROSSTALK vs FREQUENCY


FIGURE 8. CMRR vs FREQUENCY


FIGURE 10. OFF ISOLATION vs FREQUENCY


FIGURE 12. THD+N vs FREQUENCY

Typical Performance Curves (Continued)


FIGURE 13. THD+N @ 1 kHz vs $\mathrm{V}_{\text {OUT }}$


FIGURE 15. INPUT REFERRED NOISE CURRENT vs FREQUENCY


FIGURE 17. SMALL SIGNAL STEP RESPONSE


FIGURE 14. INPUT REFERRED NOISE VOLTAGE vs FREQUENCY


FIGURE 16. ENABLE/DISABLE TIMING


FIGURE 18. LARGE SIGNAL (1V) STEP RESPONSE

Typical Performance Curves (Continued)


FIGURE 19. LARGE SIGNAL (4.7V) STEP RESPONSE


FIGURE 21. $\mathrm{V}_{\mathrm{OS}}$ vs TEMPERATURE, $\mathrm{v}_{\mathrm{S}}= \pm 2.5 \mathrm{~V}$


FIGURE 23. $\mathrm{I}_{\mathrm{BIAS}}$ - vS TEMPERATURE, $\mathrm{v}_{\mathrm{S}}= \pm \mathbf{2 . 5 \mathrm { V }}$


FIGURE 20. SUPPLY CURRENT vs TEMPERATURE, $\mathrm{V}_{\mathrm{S}}= \pm 2.5 \mathrm{~V}$ ENABLED, $\mathrm{R}_{\mathrm{L}}=\operatorname{INF}$


FIGURE 22. $\mathrm{I}_{\mathrm{BIAS}}+\mathrm{vS}$ TEMPERATURE, $\mathrm{V}_{\mathrm{S}}= \pm 2.5 \mathrm{~V}$


FIGURE 24. $\mathrm{I}_{\mathrm{IO}}$ vs TEMPERATURE, $\mathrm{v}_{\mathrm{S}}= \pm 2.5 \mathrm{~V}$

## Typical Performance Curves (Continued)



FIGURE 25. CMRR vs TEMPERATURE, VCM $=3.8 \mathrm{~V}$, $\mathrm{V}_{\mathrm{S}}= \pm 2.5 \mathrm{~V}$


FIGURE 27. POSITIVE $V_{\text {OUT }}$ vS TEMPERATURE, $R_{L}=\mathbf{1 k}$ $\mathrm{V}_{\mathrm{S}}= \pm 2.5 \mathrm{~V}$


FIGURE 26. PSRR vs TEMPERATURE $\pm 1.5 \mathrm{~V}$ TO $\pm 2.5 \mathrm{~V}$


FIGURE 28. NEGATIVE $V_{\text {OUT }}$ vs TEMPERATURE, $R_{L}=\mathbf{1 k}$ $\mathrm{V}_{\mathrm{S}}= \pm 2.5 \mathrm{~V}$

## Pin Descriptions

| $\begin{aligned} & \text { ISL28191 } \\ & \text { (6 Ld SOT-23) } \end{aligned}$ | $\begin{aligned} & \text { ISL28191 } \\ & (6 \text { Ld } \mu \text { TDFN }) \end{aligned}$ | $\begin{aligned} & \text { ISL28291 } \\ & \text { (8 Ld SOIC) } \end{aligned}$ | $\begin{aligned} & \text { ISL28291 } \\ & \text { (10 Ld MSOP) } \end{aligned}$ | $\begin{gathered} \text { ISL28291 } \\ (10 \text { Ld } \mu \text { TQFN }) \end{gathered}$ | PIN NAME | FUNCTION | EQUIVALENT CIRCUIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 4 | 2 | $\begin{aligned} & 2(A) \\ & 6(B) \end{aligned}$ | $\begin{aligned} & 2(\mathrm{~A}) \\ & 8 \text { (B) } \end{aligned}$ | $\begin{aligned} & 1 \text { (A) } \\ & 7 \text { (B) } \end{aligned}$ | $\begin{aligned} & \text { IN- } \\ & \text { IN-_A } \\ & \text { IN-_B } \end{aligned}$ | Inverting input |  |
| 3 | 3 | $\begin{aligned} & 3 \text { (A) } \\ & 5 \text { (B) } \end{aligned}$ | $\begin{aligned} & 3 \text { (A) } \\ & 7 \text { (B) } \end{aligned}$ | $\begin{aligned} & 2(A) \\ & 6(B) \end{aligned}$ | $\begin{gathered} \text { IN+ } \\ \text { IN+_B } \\ \text { IN+_B } \end{gathered}$ | Non-inverting input | (See circuit 1) |
| 2 | 4 | 4 | 4 | 3 | V- | Negative supply |  |

## Pin Descriptions (Continued)

| $\begin{aligned} & \text { ISL28191 } \\ & \text { (6 Ld SOT-23) } \end{aligned}$ | $\begin{aligned} & \text { ISL28191 } \\ & (6 \text { Ld } \mu \text { TDFN }) \end{aligned}$ | $\begin{aligned} & \text { ISL28291 } \\ & \text { (8 Ld SOIC) } \end{aligned}$ | $\begin{aligned} & \text { ISL28291 } \\ & \text { (10 Ld MSOP) } \end{aligned}$ | $\begin{gathered} \text { ISL28291 } \\ (10 \text { Ld } \mu \text { TQFN) } \end{gathered}$ | PIN NAME | FUNCTION | EQUIVALENT CIRCUIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | $\begin{aligned} & 1 \text { (A) } \\ & 7 \text { (B) } \end{aligned}$ | $\begin{aligned} & 1 \text { (A) } \\ & 9 \text { (B) } \end{aligned}$ | $\begin{gathered} 10(A) \\ 8(B) \end{gathered}$ | $\begin{aligned} & \text { OUT } \\ & \text { OUT_A } \\ & \text { OUT_B } \end{aligned}$ | Output |  |
| 6 | 6 | 8 | 10 | 9 | V+ | Positive supply |  |
| 5 | 5 | N/A | $\begin{aligned} & 5(\mathrm{~A}) \\ & 6 \text { (B) } \end{aligned}$ | $\begin{aligned} & 4(A) \\ & 5(B) \end{aligned}$ | $\begin{aligned} & \overline{\overline{E N}} \\ & \overline{\mathrm{EN}} \text { _A } \\ & \overline{\mathrm{EN}} \text { _B } \end{aligned}$ | Enable BAR pin internal pull-down; Logic "1" selects the disabled state; Logic "0" selects the enabled state. | Circuit 3 |

## Applications Information

## Product Description

The ISL28191 and ISL28291 are voltage feedback operational amplifiers designed for communication and imaging applications requiring low distortion, very low voltage and current noise. Both parts feature high bandwidth while drawing moderately low supply current. They use a classical voltage-feedback topology, which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier.

## Enable/Power-Down

The ISL28191 and ISL28291 amplifiers are disabled by applying a voltage greater than 2 V to the $\overline{\mathrm{EN}}$ pin, with respect to the V - pin. In this condition, the output(s) will be in a high impedance state and the amplifier(s) current will be reduced to $13 \mu \mathrm{~A} / \mathrm{Amp}$. By disabling the part, multiple parts can be connected together as a MUX. The outputs are tied together in parallel and a channel can be selected by the $\overline{\mathrm{EN}}$ pin. The $\overline{\mathrm{EN}}$ pin also has an internal pull-down. If left open, the $\overline{\mathrm{EN}}$ pin will pull to the negative rail and the device will be enabled by default.

## Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. Both parts have additional back-to-back diodes across the input terminals (as shown in Figure 29). In pulse applications where the input Slew Rate exceeds the Slew Rate of the amplifier, the possibility exists for the input protection diodes to become forward biased. This can cause excessive input current and distortion at the outputs. If overdriving the inputs is necessary, the external input current must never exceed 5 mA . An
external series resistor may be used to limit the current, as shown in Figure 29.


FIGURE 29. LIMITING THE INPUT CURRENT TO LESS THAN 5 mA

## Using Only One Channel

The ISL28291 is a dual channel op amp. If the application only requires one channel when using the ISL28291, the user must configure the unused channel to prevent it from oscillating. Oscillation can occur if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 30).


## FIGURE 30. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

## Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Low impedance ground plane construction is essential. Surface mount components are recommended, but if leaded components are used, lead lengths should be as short as possible. The power supply pins must be well bypassed to
reduce the risk of oscillation. The combination of a $4.7 \mu \mathrm{~F}$ tantalum capacitor in parallel with a $0.01 \mu \mathrm{~F}$ capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum, especially at the inverting input. When ground plane construction is used, it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of additional series inductance. Use of sockets, particularly for the SOIC package, should be avoided if possible. Sockets add parasitic inductance and capacitance, which will result in additional peaking and overshoot.

## Current Limiting

The ISL28191 and ISL28291 have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device. This is why the output short circuit current is specified and tested with $\mathrm{R}_{\mathrm{L}}=10 \Omega$.

## Power Dissipation

It is possible to exceed the $+125^{\circ} \mathrm{C}$ maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature ( $\mathrm{T}_{\mathrm{JMAX}}$ ) for all applications to determine if power supply voltages, load conditions, or
package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:
$T_{\text {JMAX }}=T_{\text {MAX }}+\left(\theta_{\text {JA }} \times\right.$ PD $\left._{\text {MAXTOTAL }}\right)$
where:

- PDMAXTOTAL is the sum of the maximum power dissipation of each amplifier in the package ( $\mathrm{PD}_{\mathrm{MAX}}$ )
- PD $_{\text {MAX }}$ for each amplifier can be calculated in Equation 2:

(EQ. 2)
where:
- $\mathrm{T}_{\text {MAX }}=$ Maximum ambient temperature
- $\theta_{\mathrm{JA}}=$ Thermal resistance of the package
- $\mathrm{PD}_{\mathrm{MAX}}=$ Maximum power dissipation of 1 amplifier
- $\mathrm{V}_{\mathrm{S}}=$ Supply voltage
- $I_{\text {MAX }}=$ Maximum supply current of 1 amplifier
- $\mathrm{V}_{\text {OUTMAX }}=$ Maximum output voltage swing of the application
- $\mathrm{R}_{\mathrm{L}}=$ Load resistance


## SOT-23 Package Family



## MDP0038

SOT-23 PACKAGE FAMILY

| SYMBOL | MILLIMETERS |  |  |
| :---: | :---: | :---: | :---: |
|  | SOT23-5 | SOT23-6 |  |
| A | 1.45 | 1.45 | MAX |
| A1 | 0.10 | 0.10 | $\pm 0.05$ |
| A2 | 1.14 | 1.14 | $\pm 0.15$ |
| b | 0.40 | 0.40 | $\pm 0.05$ |
| c | 0.14 | 0.14 | $\pm 0.06$ |
| D | 2.90 | 2.90 | Basic |
| E | 2.80 | 2.80 | Basic |
| E1 | 1.60 | 1.60 | Basic |
| e | 0.95 | 0.95 | Basic |
| e1 | 1.90 | 1.90 | Basic |
| L | 0.45 | 0.45 | $\pm 0.10$ |
| L1 | 0.60 | 0.60 | Reference |
| N | 5 | 6 | Reference |

## NOTES:

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.
3. This dimension is measured at Datum Plane " H ".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin \#1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

## Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)



BOTTOM VIEW


LAND PATTERN 6

L6.1.6x1.6A
6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

| SYMBOL | MILLIMETERS |  |  | NOTES |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | NOMINAL | MAX |  |  |  |  |
| A | 0.45 | 0.50 | 0.55 | - |  |  |  |
| A1 | - | - | 0.05 | - |  |  |  |
| A3 | 0.127 REF |  |  | - |  |  |  |
| b | 0.15 | 0.20 | 0.25 | - |  |  |  |
| D | 1.55 | 1.60 | 1.65 | 4 |  |  |  |
| D2 | 0.40 | 0.45 | 0.50 | - |  |  |  |
| E | 1.55 | 1.60 | 1.65 | 4 |  |  |  |
| E2 | 0.95 | 1.00 | 1.05 | - |  |  |  |
| e | 0.50 BSC |  |  |  |  |  | - |
| L | 0.25 | 0.30 | 0.35 | - |  |  |  |

Rev. 1 6/06
NOTES:

1. Dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08 mm .
3. Warpage shall not exceed 0.10 mm .
4. Package length/package width are considered as special characteristics.
5. JEDEC Reference MO-229.
6. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

## Small Outline Package Family (SO)



MDP0027
SMALL OUTLINE PACKAGE FAMILY (SO)

| SYMBOL | INCHES |  |  |  |  |  |  | TOLERANCE | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | SO-8 | SO-14 | $\begin{gathered} \text { SO16 } \\ (0.150 ") \end{gathered}$ | $\begin{gathered} \text { SO16 (0.300") } \\ \text { (SOL-16) } \end{gathered}$ | $\begin{gathered} \text { SO20 } \\ \text { (SOL-20) } \end{gathered}$ | $\begin{gathered} \text { SO24 } \\ (\mathrm{SOL}-24) \end{gathered}$ | $\begin{gathered} \text { SO28 } \\ \text { (SOL-28) } \end{gathered}$ |  |  |
| A | 0.068 | 0.068 | 0.068 | 0.104 | 0.104 | 0.104 | 0.104 | MAX | - |
| A1 | 0.006 | 0.006 | 0.006 | 0.007 | 0.007 | 0.007 | 0.007 | $\pm 0.003$ | - |
| A2 | 0.057 | 0.057 | 0.057 | 0.092 | 0.092 | 0.092 | 0.092 | $\pm 0.002$ | - |
| b | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | $\pm 0.003$ | - |
| c | 0.009 | 0.009 | 0.009 | 0.011 | 0.011 | 0.011 | 0.011 | $\pm 0.001$ | - |
| D | 0.193 | 0.341 | 0.390 | 0.406 | 0.504 | 0.606 | 0.704 | $\pm 0.004$ | 1,3 |
| E | 0.236 | 0.236 | 0.236 | 0.406 | 0.406 | 0.406 | 0.406 | $\pm 0.008$ | - |
| E1 | 0.154 | 0.154 | 0.154 | 0.295 | 0.295 | 0.295 | 0.295 | $\pm 0.004$ | 2, 3 |
| e | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | 0.030 | 0.030 | 0.030 | 0.030 | $\pm 0.009$ | - |
| L1 | 0.041 | 0.041 | 0.041 | 0.056 | 0.056 | 0.056 | 0.056 | Basic | - |
| h | 0.013 | 0.013 | 0.013 | 0.020 | 0.020 | 0.020 | 0.020 | Reference | - |
| N | 8 | 14 | 16 | 16 | 20 | 24 | 28 | Reference | - |

NOTES:
Rev. M 2/07

1. Plastic or metal protrusions of 0.006 " maximum per side are not included.
2. Plastic interlead protrusions of 0.010 " maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

## Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



L10.1.8x1.4A
10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

| SYMBOL | MILLIMETERS |  |  | MIN |
| :---: | :---: | :---: | :---: | :---: |
|  | MAX | NOTES |  |  |
| A | 0.45 | 0.50 | 0.55 | - |
| A1 | - | - | 0.05 | - |
| A3 | 0.127 REF |  |  | - |
| b | 0.15 | 0.20 | 0.25 | 5 |
| D | 1.75 | 1.80 | 1.85 | - |
| E | 1.35 | 1.40 | 1.45 | - |
| e | 0.40 BSC |  |  | - |
| L | 0.35 | 0.40 | 0.45 | - |
| L1 | 0.45 | 0.50 | 0.55 | - |
| N | 10 |  |  |  |
| Nd | 2 |  |  |  |
| Ne | 3 |  |  |  |
| $\theta$ | 0 | - | 12 | 4 |

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. $N$ is the number of terminals.
3. Nd and Ne refer to the number of terminals on $D$ and $E$ side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension $b$ applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip.
6. The configuration of the pin \#1 identifier is optional, but must be located within the zone indicated. The pin \#1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05 mm .
8. Maximum allowable burrs is 0.076 mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

Mini SO Package Family (MSOP)


MDP0043
MINI SO PACKAGE FAMILY

| SYMBOL | MILLIMETERS |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MSOP8 | MSOP10 | TOLERANCE |  |
| A | 1.10 | 1.10 | Max. | - |
| A1 | 0.10 | 0.10 | $\pm 0.05$ | - |
| A2 | 0.86 | 0.86 | $\pm 0.09$ | - |
| b | 0.33 | 0.23 | $+0.07 /-0.08$ | - |
| c | 0.18 | 0.18 | $\pm 0.05$ | - |
| D | 3.00 | 3.00 | $\pm 0.10$ | 1,3 |
| E | 4.90 | 4.90 | $\pm 0.15$ | - |
| E1 | 3.00 | 3.00 | $\pm 0.10$ | 2,3 |
| e | 0.65 | 0.50 | Basic | - |
| L | 0.55 | 0.55 | $\pm 0.15$ | - |
| L1 | 0.95 | 0.95 | Basic | - |
| N | 8 | 10 | Reference | - |

Rev. D 2/07
NOTES:

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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