ADC Driver Evaluation Boards

National Semiconductor
Application Note 1812
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General Description

The ADC driver evaluation boards are designed to aid in the characterization of National Semiconductor's high-speed operational amplifier portfolio. Utilize these evaluation boards as guides for high frequency layout and as tools to aid in the design of ADC driver applications.

ADC Driver Configuration	Package	Device
Single to Single	6-Pin SOT23	LMH6611MK or LMH6618MK
Single to Differential	8-Pin SOIC	LMH6612MA or LMH6619MA
Differential to Differential	8-Pin SOIC	LMH6612MA or LMH6619MA

Although specifically designed for high speed op amps, these evaluation boards can be used for op amps in these packages with the same pinout.

Basic Operation

Single to Single ADC Driver

This architecture has a single-ended input source connected to the input of the op amp and the single-ended output of the op amp can then be fed off board to the single-ended input of an ADC. Figure 1 shows the board schematic of the single to single ADC driver in a 2nd order multiple-feedback inverting configuration. The inverting configuration is preferred over the non-inverting configuration, as it offers more linear output response. The ADC driver's cutoff frequency is found from the equation:

$$f_0 = \frac{1}{2\pi} * \sqrt{\frac{1}{R_2 * R_3 * C_2 * C_3}}$$

The op amp's gain is set by the equation:

$$\text{GAIN} = -\frac{R_2}{R_1}$$

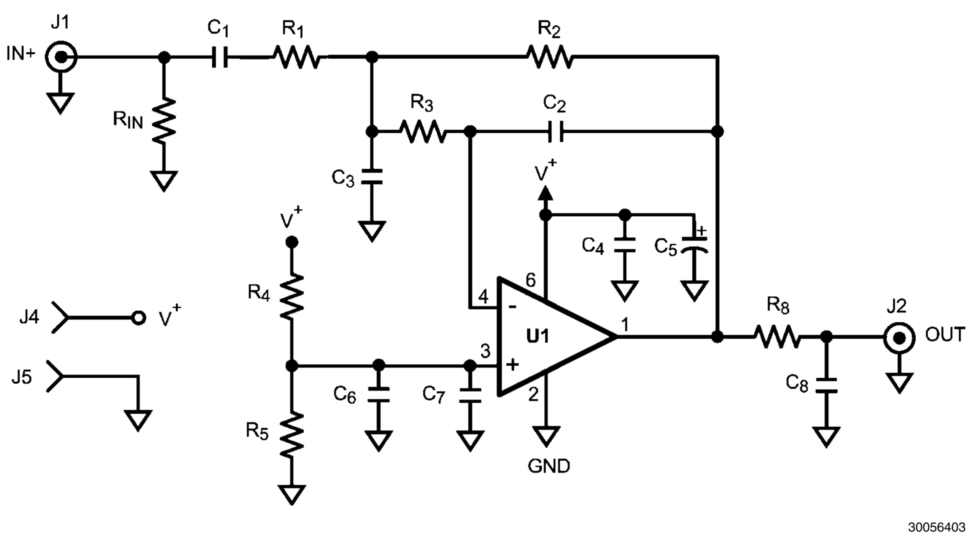

FIGURE 1. Single to Single ADC Driver Board Schematic

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A sample Bill of Material (BOM) for a single to single ADC driver board is given in the table below. The ADC driver will have a cutoff frequency of 500 kHz and a gain of -1.

Designator	Description	Comment
C_1	0805 Capacitor	1 µF
C_2	0805 Capacitor	150 pF
C_3	0805 Capacitor	1 nF
C_4	0603 Capacitor	0.1 µF
C_5	Tantalum Capacitor	6.8 µF
C_6	0805 Capacitor	5.6 µF
C_7	0805 Capacitor	0.1 µF
C_8	0805 Capacitor	220 pF
J1	SMA Connector	IN+
J2	SMA Connector	OUT
J4, J5	Test Point	Test Point
R_1, R_2	0805 Capacitor	549
R_3	0805 Capacitor	1.24k
R_4, R_5	0805 Capacitor	14.3k
R_8	0805 Capacitor	22
R_{IN}	0805 Capacitor	50
U1	6-Pin SOT23	LMH6611/LMH6618

Single to Differential ADC Driver

The single to differential ADC driver board schematic in *Figure 2* utilizes a dual op amp to buffer a single-ended source to drive an ADC with differential inputs. One of the op amps, U1A, is configured as a unity gain buffer that drives the inverting (IN−) input of the op amp U1B and the non-inverting (IN+) input of the ADC. U1B inverts the input signal and drives the inverting input of the ADC. The ADC driver is configured for a gain of +2 to reduce the noise without sacrificing THD performance. The common mode voltage of 2.5V is supplied at the non-inverting inputs of both op amps U1A and U1B. This configuration produces differential ±2.5 V_{PP} output signals, when the single-ended input signal of 0 to VREF is AC coupled into the non-inverting terminal of the op amp and each non-inverting terminal of the op amp is biased at the mid-scale of 2.5V. The two output RC anti-aliasing filters are used between the outputs of both U1A and U1B and the inputs of the ADC to minimize the effect of undesired high frequency noise coming from the input source. Each RC filter's cutoff frequency is found from the equation:

$$f_0 = \frac{1}{2\pi RC}$$

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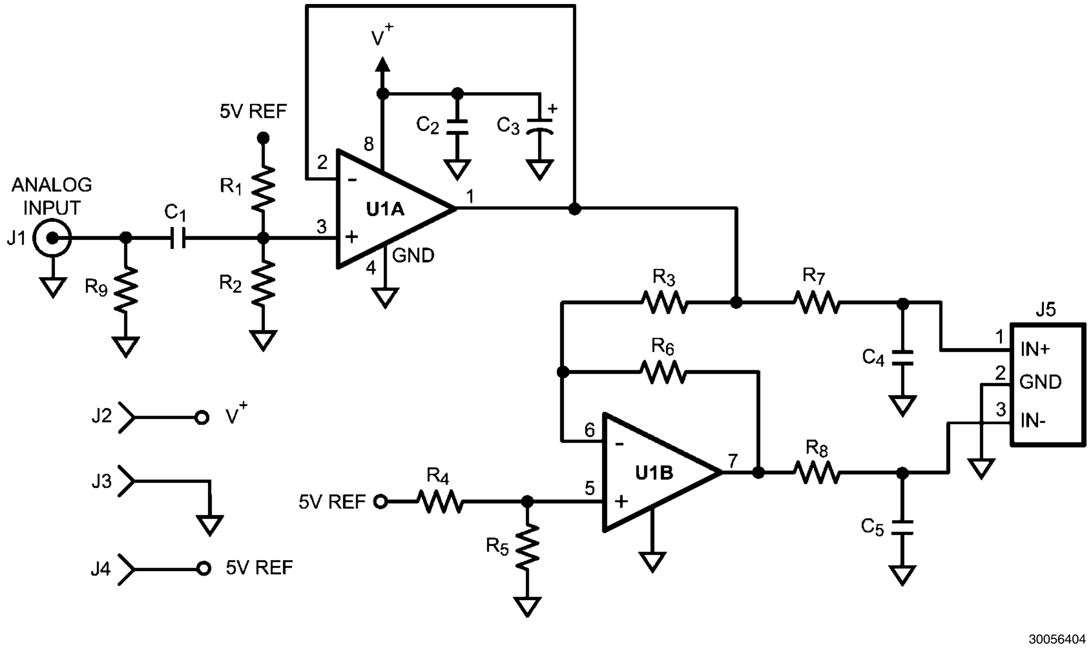

FIGURE 2. Single to Differential ADC Driver Board Schematic

A sample Bill of Material (BOM) for a single to differential ADC driver board is given in the table below.

Designator	Description	Comment
C_1	0805 Capacitor	10 µF
C_2	0805 Capacitor	0.1 µF
C_3	Tantalum Capacitor	6.8 µF
C_4, C_5	0805 Capacitor	220 pF
J1	SMA Connector	Analog Input
J2, J3, J4	Test Point	Test Point
J5	SIP3	Out
R_1, R_2, R_4, R_5	0805 Capacitor	2.5k
R_3, R_6	0805 Capacitor	560
R_7, R_8	0805 Capacitor	33
R_9	0805 Capacitor	50
U1	8-Pin SOIC	LMH6612/LMH6619

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Differential to Differential ADC Driver

A dual op amp can be configured as a differential to differential ADC driver to buffer a differential source to a differential input ADC as shown in *Figure 3*. The differential to differential ADC driver can be formed using two single to single ADC drivers. Each output from these drivers goes to a separate input of the differential ADC. Each single to single ADC driver uses the same components and is in a multi-feedback inverting configuration.

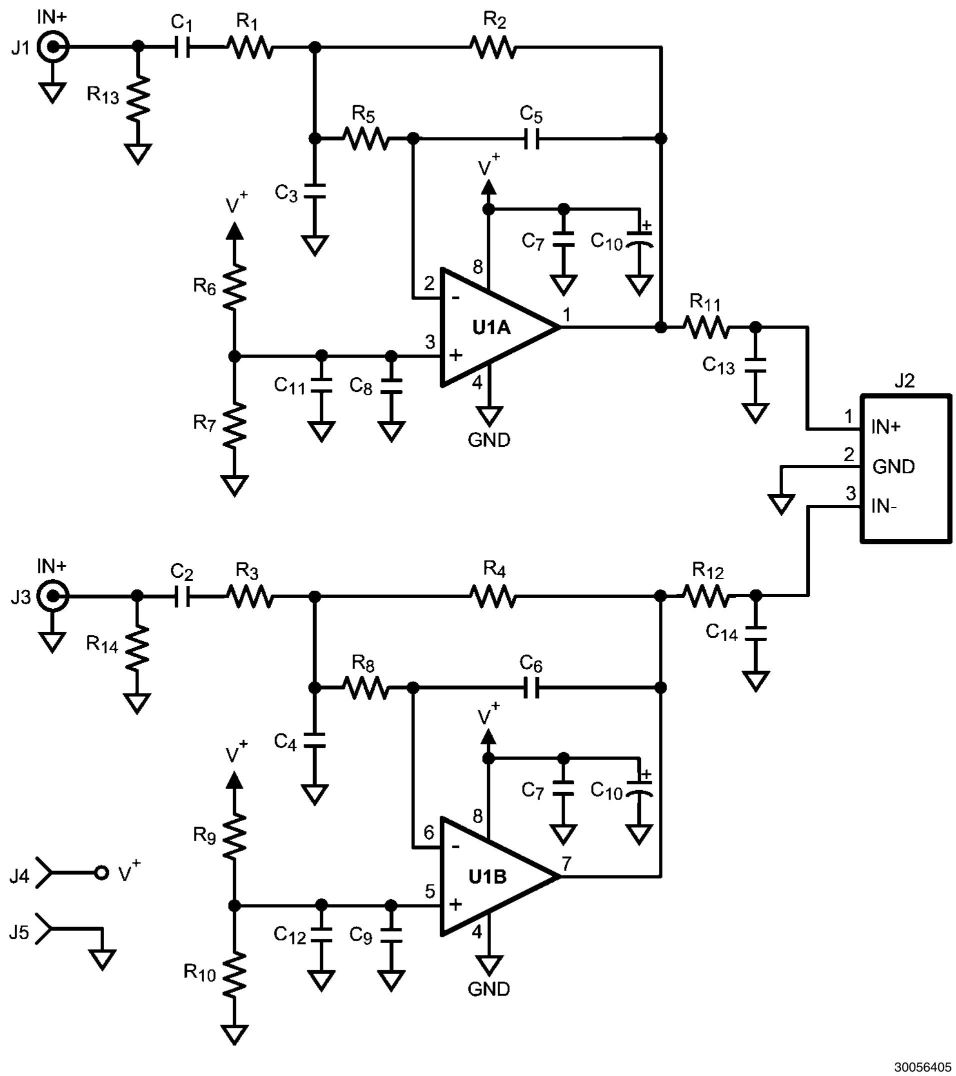

FIGURE 3. Differential to Differential ADC Driver Board Schematic

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A sample Bill of Material (BOM) for a differential to differential ADC driver board is given in the table below. The ADC driver will have a cutoff frequency of 500 kHz and a gain of -1.

Designator	Description	Comment
C_1, C_2	0805 Capacitor	1 µF
C_3, C_4	0805 Capacitor	1 nF
C_5, C_6	0603 Capacitor	150 pF
C_7, C_8, C_9	0805 Capacitor	0.1 µF
C_{10}	Tantalum Capacitor	6.8 µF
C_{11}, C_{12}	0805 Capacitor	5.6 µF
C_{13}, C_{14}	0805 Capacitor	220 pF
J1, J3	SMA Connector	IN+
J2	SIP3	Out
J4, J5	Test Point	Test Point
R_1, R_2, R_3, R_4	0805 Capacitor	549
R_5, R_8	0805 Capacitor	1.24k
R_6, R_7, R_9, R_{10}	0805 Capacitor	14.3k
R_{11}, R_{12}	0805 Capacitor	22
R_{13}, R_{14}	0805 Capacitor	50
U1	8-Pin SOIC	LMH6612/LMH6619

Measurement Hints

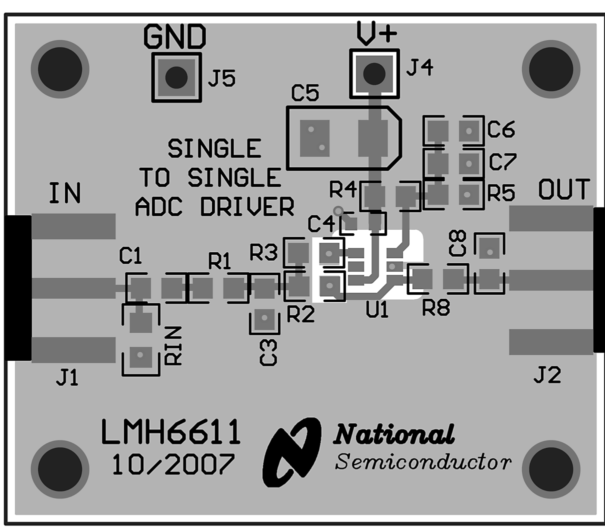
It is important to connect the input source ground with the supply ground. For each ADC driver configuration, it is important to account for the impedance of the signal source when setting up the resistor networks to ensure that the differential outputs have the same gain. For example, an audio precision signal generator has about 22Ω of source impedance and the typical board termination is 50Ω, so the gain and input signal must be adjusted in order to obtain the desired signal at the output of the op amp.

Layout Considerations

The following are recommendations for PCB layout in order to obtain the optimum high frequency performance:

- Place the ADC and amplifier as close together as possible.
- Put the supply bypassing capacitors as close as possible to the device (<1”).
- Utilize surface mount components instead of through-hole components.
- Keep the traces short where possible.
- Use terminated transmission lines for long traces.

The top and bottom layouts of all three ADC driver configurations are shown in Figure 4 below.



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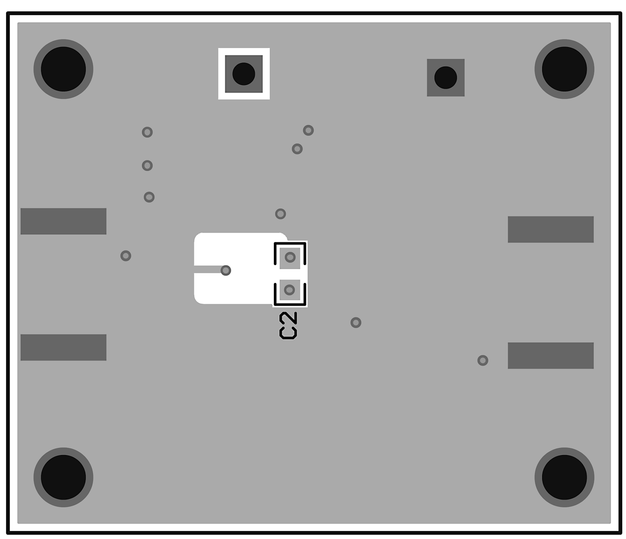
Single to Single Top Layer



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Single to Single Bottom Layer

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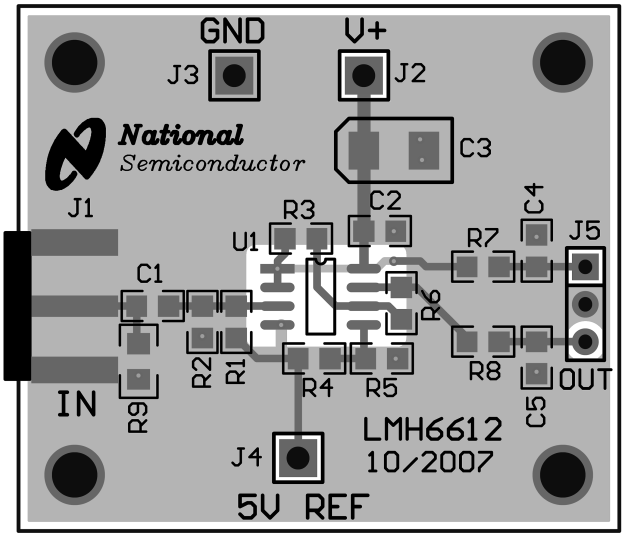

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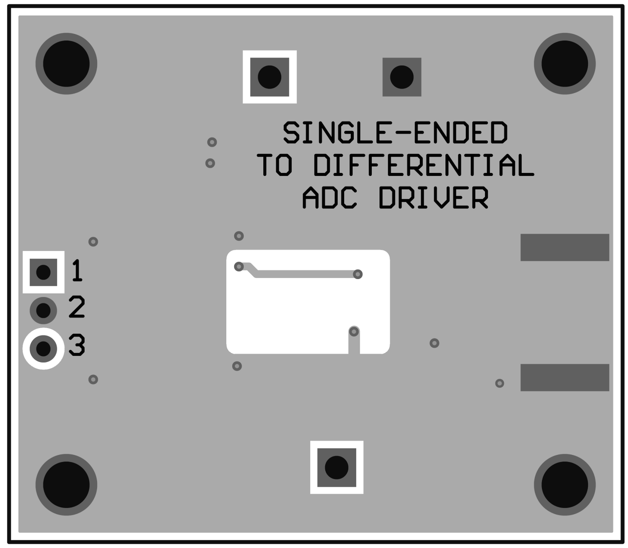
Single to Differential Top Layer



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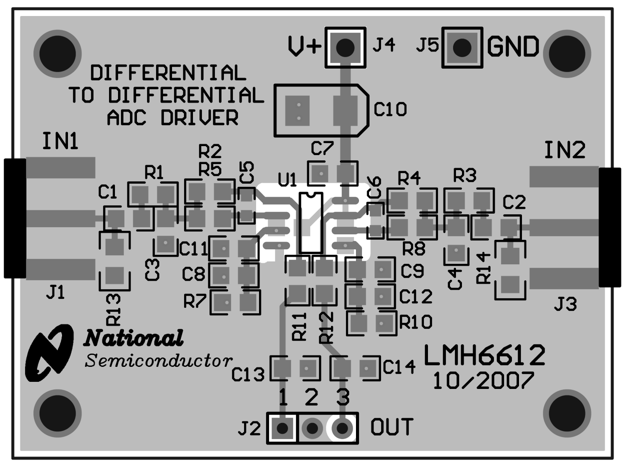
Single to Differential Bottom Layer



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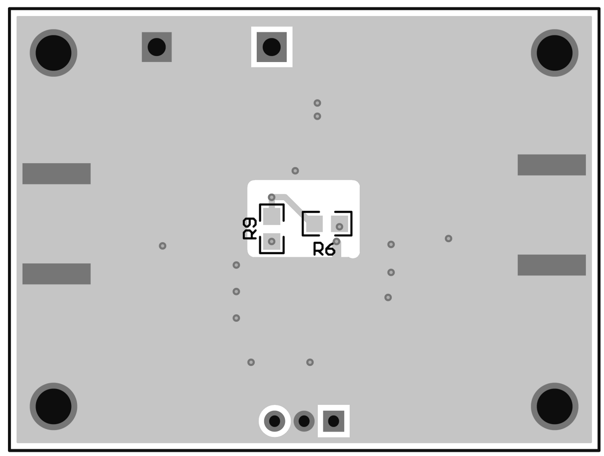
Differential to Differential Top Layer



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Differential to Differential Bottom Layer

FIGURE 4. Top and Bottom Layouts of All Three ADC Driver Configurations

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Notes

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Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
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