National Semiconductor

December 2004

LMH6560
Quad, High-Speed, Closed-Loop Buffer

General Description

The LMH™6560 is a high speed, closed-loop buffer designed for applications requiring the processing of very high frequency signals. While offering a small signal bandwidth of 680MHz, and a very high slew rate of 3100V/μs the LMH6560 consumes only 46mA of quiescent current for all four buffers. Total harmonic distortion into a load of 100Ω at 20MHz is −51dBc. The LMH6560 is configured internally for a loop gain of one. Input resistance is 100kΩ and output resistance is but 1.5Ω. Crosstalk between the buffers is only −55dB. These characteristics make the LMH6560 an ideal choice for the distribution of high frequency signals on printed circuit boards. Differential gain and phase specifications of 0.10% and 0.03˚ respectively at 3.58MHz make the LMH6560 well suited for the buffering of video signals.

The device is fabricated on National's high speed VIP10 process using National's proven high performance circuit architectures.

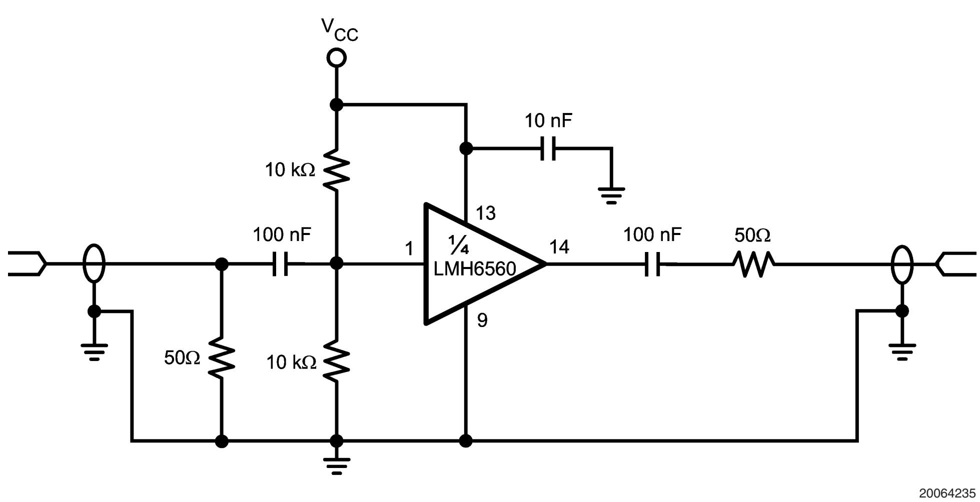
Features

- Closed-loop quad buffer
- 680MHz small signal bandwidth
- 3100V/μs slew rate
- 0.10% / 0.03˚ differential gain / phase
- −51dBc THD at 20MHz
- Single supply operation (3V min.)
- 80mA output current

Applications

- Multi-channel video distribution
- Video switching and routing
- High-speed analog multiplexing
- Channelized EW
- High-density buffering
- Active filters
- Broadcast and high definition TV systems
- Medical imaging
- Test equipment and instrumentation

Typical Schematic



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	
Human Body Model	2000V (Note 2)
Machine Model	200V (Note 3)
Output Short Circuit Duration	(Note 4),(Note 5)
Supply Voltage ($V^+ - V^-$)	13V
Voltage at Input/Output Pins	V^+ +0.8V, V^- −0.8V
Soldering Information	
Infrared or Convection (20 sec.)	235˚C
Wave Soldering (10 sec.)	260˚C
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 6)	+150˚C

Operating Ratings (Note 1)

Supply Voltage ($V^+ - V^-$)	3-10V
Operating Temperature Range (Note 6), (Note 7)	−40˚C to +85˚C
Package Thermal Resistance (θ_{JA}) (Note 6), (Note 7)	
14-Pin SOIC	137˚C/W
14-Pin TSSOP	160˚C/W

±5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = +5V, V^- = −5V, V_O = V_{CM} = 0V and R_L = 100Ω to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	V_O < 0.5V_{PP}		680		MHz
GFN	Gain Flatness < 0.1dB	V_O < 0.5V_{PP}		375		MHz
FPBW	Full Power Bandwidth (−3dB)	V_O = 2V_{PP} (+10dBm)		280		MHZ
DG	Differential Gain	R_L = 150Ω to 0V; f = 3.58MHz		0.10		%
DP	Differential Phase	R_L = 150Ω to 0V; f = 3.58MHz		0.03		deg
Time Domain Response						
t_r	Rise Time	3.3V Step (20-80%)		0.6		ns
t_f	Fall Time			0.7		ns
t_s	Settling Time to 0.1%	3.3V Step		9		ns
OS	Overshoot	1V Step		4		%
SR	Slew Rate	(Note 11)		3100		V/μs
Distortion And Noise Performance						
HD2	2nd Harmonic Distortion	V_O = 2V_{PP}; f = 20MHz		−58		dBc
HD3	3rd Harmonic Distortion	V_O = 2V_{PP}; f = 20MHz		−52		dBc
THD	Total Harmonic Distortion	V_O = 2V_{PP}; f = 20MHz		−51		dBc
e_n	Input-Referred Voltage Noise	f = 1MHz		3		$nV/\sqrt{Hz}$
CP	1dB Compression Point	f = 10MHz		+23		dBm
CT	Amplifier Crosstalk	Receiving Amplifier: R_S = 50Ω to 0V; f = 10MHz		−55		dB
SNR	Signal to Noise Ratio	f = 5MHz; V_O = 1V_{PP}		120		dB
AGM	Amplifier Gain Matching	R_L = 2kΩ to 0V; f = 5MHz; V_O = 1V_{PP}		0.05		dB
Static, DC Performance						
A_{CL}	Small Signal Voltage Gain	V_O = 100mV_{PP} R_L = 100Ω to 0V	**0.97**	0.995		V/V
		V_O = 100mV_{PP} R_L = 2kΩ to 0V	**0.99**	0.998		V/V
V_{OS}	Input Offset Voltage			2	20 **25**	mV
TC V_{OS}	Temperature Coefficient Input Offset Voltage	(Note 12)		28		μV/˚C

±5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = +5V, V^- = –5V, V_O = V_{CM} = 0V and R_L = 100Ω to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
I_B	Input Bias Current	(Note 10)	–10 **–14**	–5		µA
TC I_B	Temperature Coefficient Input Bias Current	(Note 12)		–4.7		nA/˚C
R_{OUT}	Output Resistance	R_L = 100Ω to 0V; f = 100kHz		1.5		Ω
		R_L = 100Ω to 0V; f = 10MHz		1.6		
PSRR	Power Supply Rejection Ratio	V_S = ±5V to V_S = ±5.25V; V_{IN} = 0V	48 **44**	67		dB
I_S	Supply Current, All 4 Buffers	No Load		46	58 **63**	mA
Miscellaneous Performance						
R_{IN}	Input Resistance			100		kΩ
C_{IN}	Input Capacitance			2		pF
V_O	Output Swing Positive	R_L = 100Ω to 0V	3.10 **3.08**	3.34		V
		R_L = 2kΩ to 0V	3.58 **3.55**	3.64		
	Output Swing Negative	R_L = 100Ω to 0V		–3.34	–3.20 **–3.17**	V
		R_L = 2kΩ to 0V		–3.64	–3.58 **–3.55**	
I_{SC}	Output Short Circuit Current	Sourcing: V_{IN} = V^+; V_O = 0V		–83		mA
		Sinking: V_{IN} = V^-; V_O = 0V		83		
I_O	Linear Output Current	Sourcing: V_{IN} - V_O = 0.5V (Note 10)	–50 **–42**	–74		mA
		Sinking: V_{IN} - V_O = –0.5V (Note 10)	50 **40**	74		

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = +5V, V^- = 0V, V_O = V_{CM} = $V^+/2$ and R_L = 100Ω to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	V_O < $0.5V_{PP}$		455		MHz
GFN	Gain Flatness < 0.1dB	V_O < $0.5V_{PP}$		75		MHz
FPBW	Full Power Bandwidth (–3dB)	V_O = $2V_{PP}$ (+10dBm)		175		MHZ
DG	Differential Gain	R_L = 150Ω to $V^+/2$; f = 3.58MHz		0.4		%
DP	Differential Phase	R_L = 150Ω to $V^+/2$; f = 3.58MHz		0.09		deg
Time Domain Response						
t_r	Rise Time	$2.3V_{PP}$ Step (20-80%)		0.8		ns
t_f	Fall Time			1.0		ns
t_s	Settling Time to 0.1%	2.3V Step		10		ns
OS	Overshoot	1V Step		0		%
SR	Slew Rate	(Note 11)		1445		V/µs

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = +5V, V^- = 0V, V_O = V_{CM} = V^+/2 and R_L = 100Ω to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
Distortion And Noise Performance						
HD2	2nd Harmonic Distortion	V_O = 2V_{PP}; f = 20MHz		–52		dBc
HD3	3rd Harmonic Distortion	V_O = 2V_{PP}; f = 20MHz		–54		dBc
THD	Total Harmonic Distortion	V_O = 2V_{PP}; f = 20MHz		–50		dBc
e_n	Input-Referred Voltage Noise	f = 1MHz		3		$nV/\sqrt{Hz}$
CP	1dB Compression Point	f = 10MHz		+14		dBm
CT	Amplifier Crosstalk	Receiving Amplifier: R_S = 50Ω to V^+/2; f = 10MHz		–55		dB
SNR	Signal to Noise Ratio	V_O = 1V_{PP}; f = 5MHz		120		dB
AGM	Amplifier Gain Matching	V_O = 1V_{PP} R_L = 2kΩ to V^+/2; f = 5MHz		0.5		dB
Static, DC Performance						
A_{CL}	Small Signal Voltage Gain	V_O = 100mV_{PP} R_L = 100Ω to V^+/2	**0.97**	0.994		V/V
		V_O = 100mV_{PP} R_L = 2kΩ to V^+/2	**0.99**	0.998		
V_{OS}	Input Offset Voltage			2	13 **15**	mV
TC V_{OS}	Temperature Coefficient Input Offset Voltage	(Note 12)		2		μV/˚C
I_B	Input Bias Current	(Note 10)	–5 **–5.5**	–2.5		μA
TC I_B	Temperature Coefficient Input Bias Current	(Note 12)		1.3		nA/˚C
R_{OUT}	Output Resistance	R_L = 100Ω to V^+/2; f = 100kHz		1.7		Ω
		R_L = 100Ω to V^+/2; f = 10MHz		2.0		
PSRR	Power Supply Rejection Ratio	V_S = +5V to V_S = +5.5V; V_{IN} = V_S/2	48 **45**	67		dB
I_S	Supply Current All 4 Buffer	No Load		21	26 **30**	mA
Miscellaneous Performance						
R_{IN}	Input Resistance			16		kΩ
C_{IN}	Input Capacitance			2		pF
V_O	Output Swing Positive	R_L = 100Ω to V^+/2	3.74 **3.70**	3.85		V
		R_L = 2kΩ to V^+/2	3.92 **3.90**	3.96		
	Output Swing Negative	R_L = 100Ω to V^+/2		1.15	1.22 **1.27**	V
		R_L = 2kΩ to V^+/2		1.04	1.08 **1.10**	
I_{SC}	Output Short Circuit Current	Sourcing: V_{IN} = V^+; V_O = V^+/2		–40		mA
		Sinking: V_{IN} = V^-; V_O = V^+/2		22		
I_O	Linear Output Current	Sourcing: V_{IN} - V_O = 0.5V (Note 10)	–50 **–40**	–64		mA
		Sinking: V_{IN} - V_O = –0.5V (Note 10)	30 **20**	45		

3V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, V_O = V_{CM} = $V^+/2$ and R_L = 100Ω to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	V_O < $0.5V_{PP}$		265		MHz
GFN	Gain Flatness < 0.1dB	V_O < $0.5V_{PP}$		40		MHz
FPBW	Full Power Bandwidth (–3dB)	V_O = $1V_{PP}$ (+4.5dBm)		115		MHZ
Time Domain Response						
t_r	Rise Time	1V Step (20-80%)		1.1		ns
t_f	Fall Time			1.3		ns
t_s	Settling Time to 0.1%	1V Step		11		ns
OS	Overshoot	0.5V Step		0		%
SR	Slew Rate	(Note 11)		480		V/µs
Distortion And Noise Performance						
HD2	2nd Harmonic Distortion	V_O = $0.5V_{PP}$; f = 20MHz		–55		dBc
HD3	3rd Harmonic Distortion	V_O = $0.5V_{PP}$; f = 20MHz		–61		dBc
THD	Total Harmonic Distortion	V_O = $0.5V_{PP}$; f = 20MHz		–54		dBc
e_n	Input-Referred Voltage Noise	f = 1MHz		3		$nV/\sqrt{Hz}$
CP	1dB Compression Point	f = 10MHz		+4		dBm
CT	Amplifier Crosstalk	Receiving Amplifier: R_S = 50Ω to $V^+/2$; f = 10MHz		–55		dB
SNR	Signal to Noise Ratio	f = 5MHz; V_O = $1V_{PP}$		120		dB
AGM	Amplifier Gain Matching	R_L = 2kΩ to $V^+/2$; f = 5MHz; V_O = $1V_{PP}$		0.4		dB
Static, DC Performance						
A_{CL}	Small Signal Voltage Gain	V_O = $100mV_{PP}$ R_L = 100Ω to $V^+/2$	**0.97**	0.99		V/V
		V_O = $100mV_{PP}$ R_L = 2kΩ to $V^+/2$	**0.99**	0.997		
V_{OS}	Input Offset Voltage			1.6	8 **10**	mV
TC V_{OS}	Temperature Coefficient Input Offset Voltage	(Note 12)		2.6		µV/°C
I_B	Input Bias Current	(Note 10)	–3 **–3.5**	–1.4		µA
TC I_B	Temperature Coefficient Input Bias Current	(Note 12)		0.3		nA/°C
R_{OUT}	Output Resistance	R_L = 100Ω to $V^+/2$; f = 100kHz		2.1		Ω
		R_L = 100Ω to $V^+/2$; f = 10MHz		2.8		
PSRR	Power Supply Rejection Ratio	V_S = +3V to V_S = +3.5V; V_{IN} = $V_S/2$	48 **46**	65		dB
I_S	Supply Current, All 4 Buffers	No Load		11	15 **18**	mA
Miscellaneous Performance						
R_{IN}	Input Resistance			17		kΩ
C_{IN}	Input Capacitance			2		pF

3V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C$, $V^+ = 3V$, $V^- = 0V$, $V_O = V_{CM} = V^+/2$ and $R_L = 100\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
V_O	Output Swing Positive	$R_L = 100\Omega$ to $V^+/2$	2.0 **1.93**	2.05		V
		$R_L = 2k\Omega$ to $V^+/2$	2.1 **2.0**	2.15		
	Output Swing Negative	$R_L = 100\Omega$ to $V^+/2$		0.95	1.0 **1.07**	V
		$R_L = 2k\Omega$ to $V^+/2$		0.85	0.90 **1.0**	
I_{SC}	Output Short Circuit Current	Sourcing: $V_{IN} = V^+$; $V_O = V^+/2$		–26		mA
		Sinking: $V_{IN} = V^-$; $V_O = V^+/2$		14		
I_O	Linear Output Current	Sourcing: $V_{IN} - V_O = 0.5V$ (Note 10)	–20 **–13**	–30		mA
		Sinking: $V_{IN} - V_O = -0.5V$ (Note 10)	12 **8**	20		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF

Note 3: Machine Model, 0Ω in series with 200pF.

Note 4: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 5: Short circuit test is a momentary test. See next note.

Note 6: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 7: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. There is no guarantee of parametric performance as indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Applications section for information on temperature de-rating of this device.

Note 8: Typical Values represent the most likely parametric norm.

Note 9: All limits are guaranteed by testing or statistical analysis.

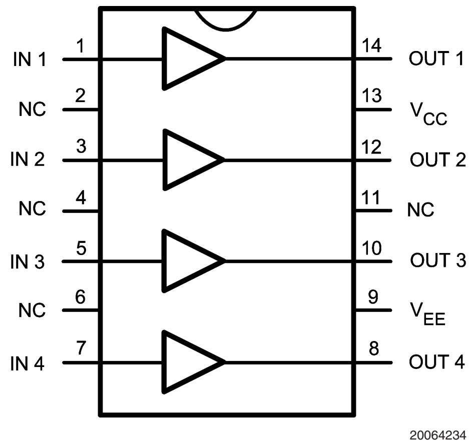
Note 10: Positive current corresponds to current flowing into the device.

Note 11: Slew rate is the average of the positive and negative slew rate. Average Temperature Coefficient is determined by dividing the change in a parameter at temperature extremes by the total temperature change.

Note 12: Average Temperature Coefficient is determined by dividing the change in a parameter at temperature extremes by the total temperature change.

Connection Diagram

14-Pin SOIC/TSSOP



Top View

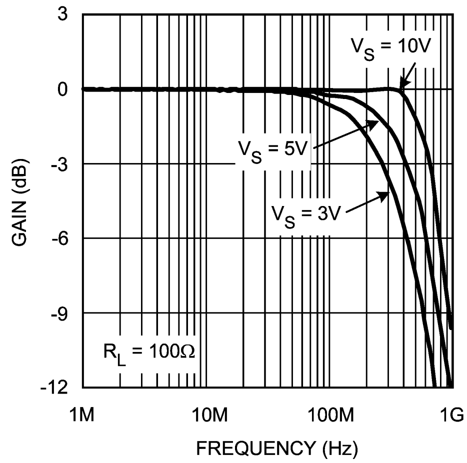
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
14-pin SOIC	LMH6560MA	LMH6560MA	55 Units/Rail	M14A
	LMH6560MAX		2.5k Units Tape and Reel	
14-pin TSSOP	LMH6560MT	LMH6560MT	94 Units/Rail	MTC14
	LMH6560MTX		2.5k Units Tape and Reel	

Typical Performance Characteristics

At T_J = 25˚C, V^+ = +5V, V^- = −5V; unless otherwise specified.

Frequency Response



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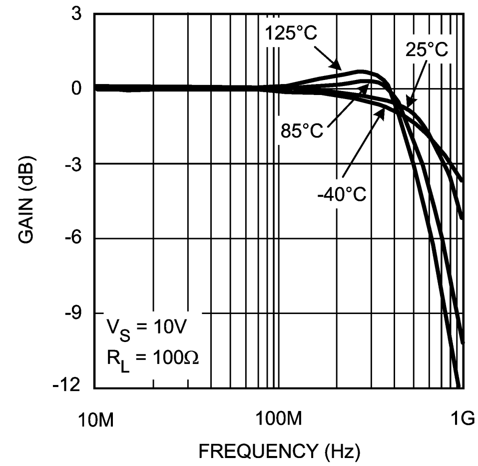
Frequency Response Over Temperature



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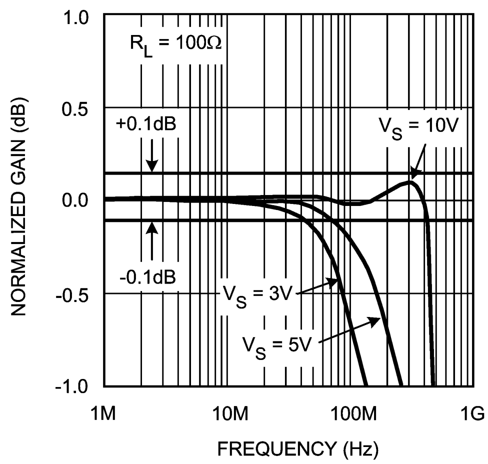
Gain Flatness 0.1dB



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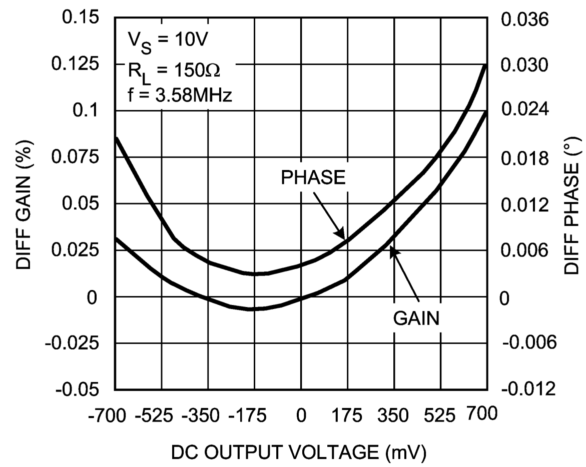
Differential Gain and Phase



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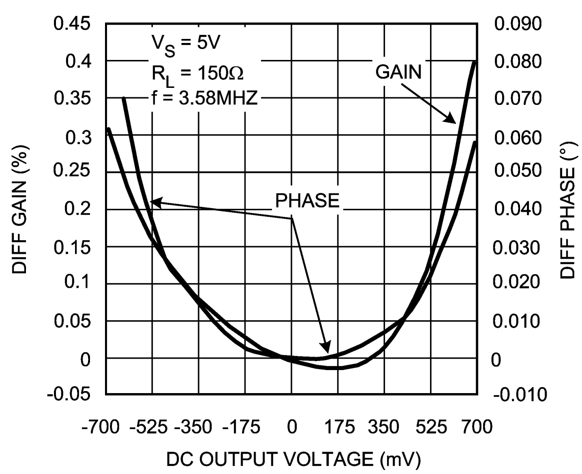
Differential Gain and Phase



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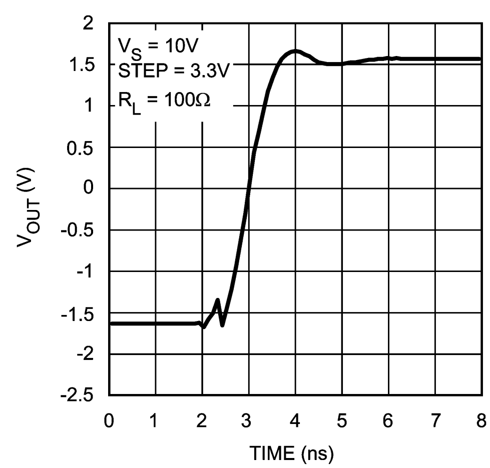
Transient Response Positive



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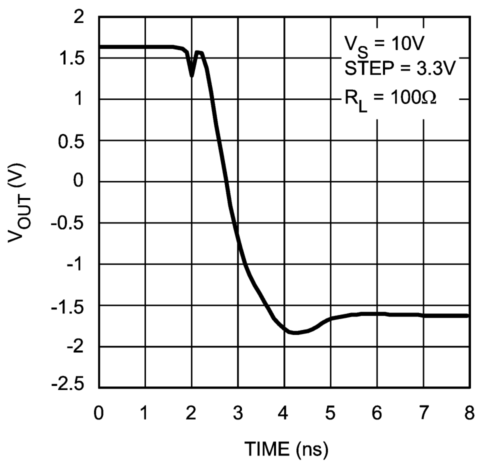
Typical Performance Characteristics At $T_J = 25^\circ C$, $V^+ = +5V$, $V^- = -5V$; unless otherwise specified. (Continued)

Transient Response Negative



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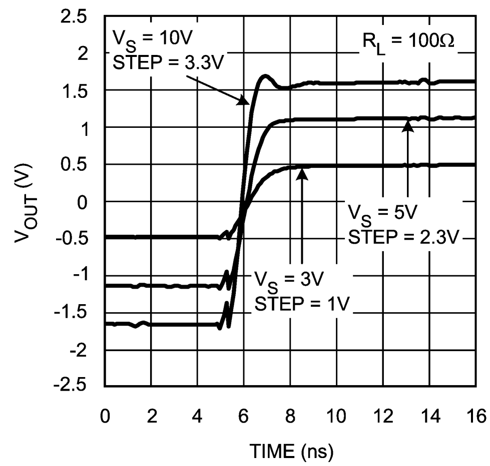
Transient Response Positive for Various V_{SUPPLY}



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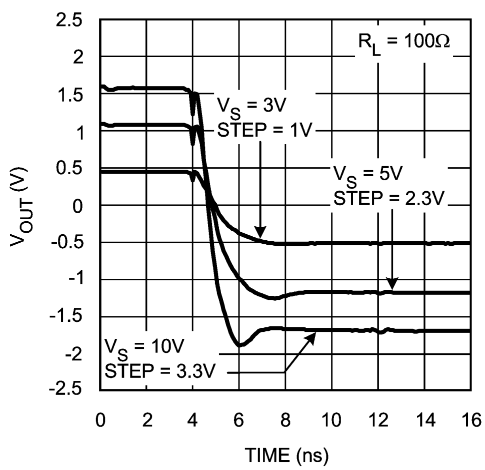
Transient Response Negative for Various V_{SUPPLY}



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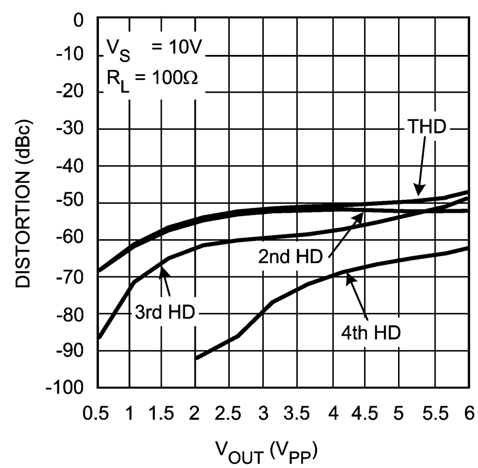
Harmonic Distortion vs. V_{OUT} @ 5MHz



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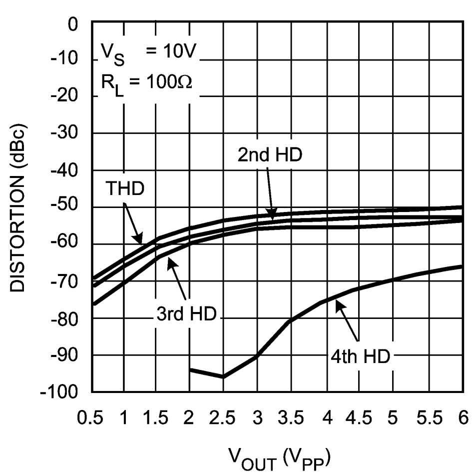
Harmonic Distortion vs. V_{OUT} @ 10MHz



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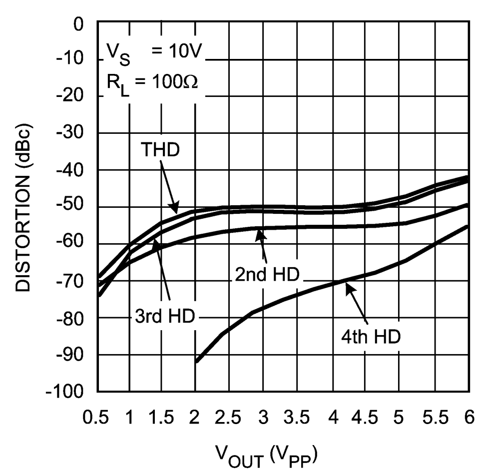
Harmonic Distortion vs. V_{OUT} @ 20MHz



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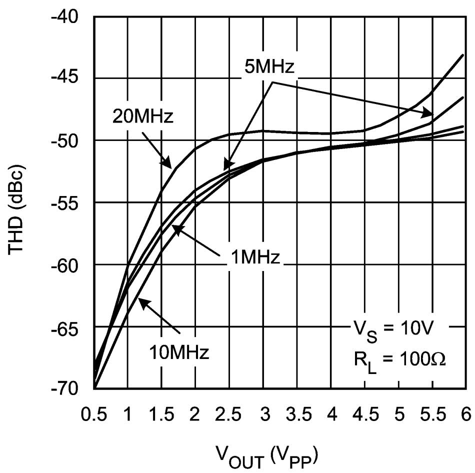
Typical Performance Characteristics At T_J = 25˚C, V^+ = +5V, V^- = −5V; unless otherwise specified. (Continued)

THD vs. V_{OUT} for Various Frequencies



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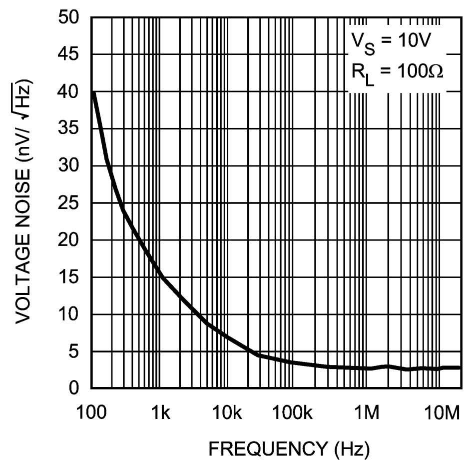
Voltage Noise



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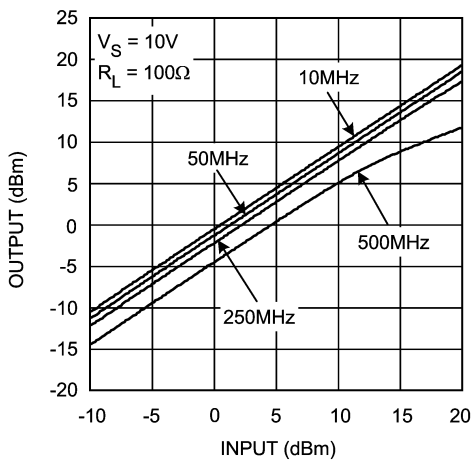
Linearity V_{OUT} vs. V_{IN}



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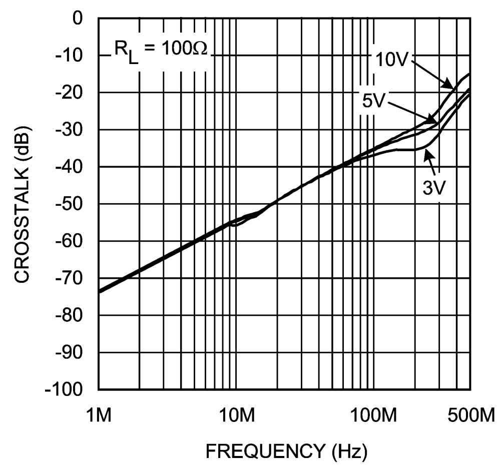
Crosstalk vs. Frequency



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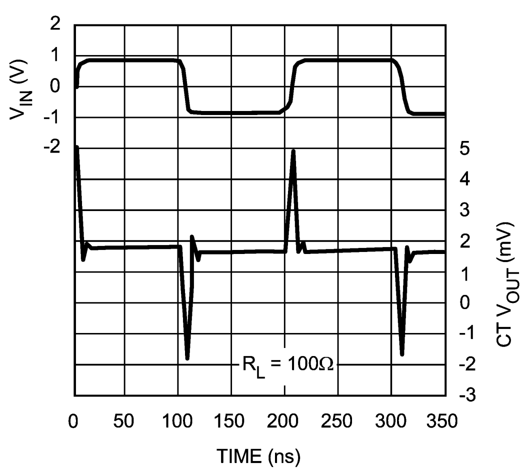
Crosstalk vs. Time



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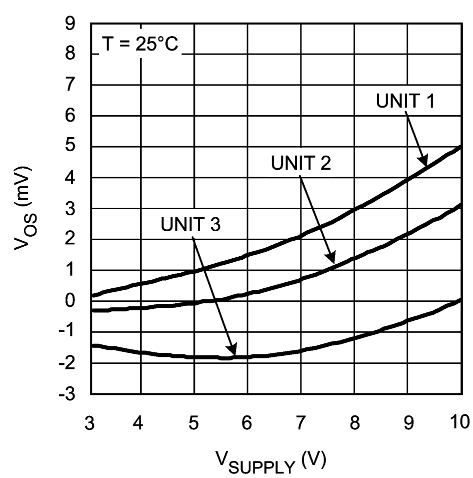
V_{OS} vs. V_{SUPPLY} for 3 Units



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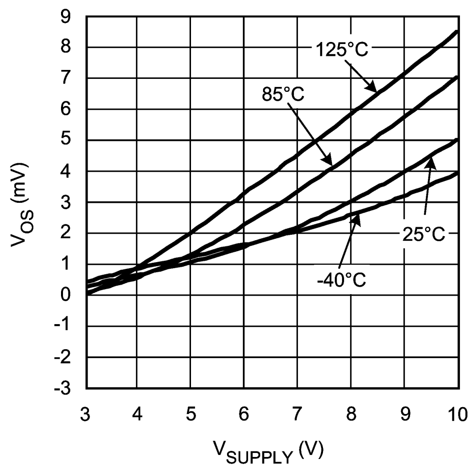
Typical Performance Characteristics
At T_J = 25˚C, V^+ = +5V, V^- = −5V; unless otherwise specified. (Continued)

V_{OS} vs. V_{SUPPLY} for Unit 1



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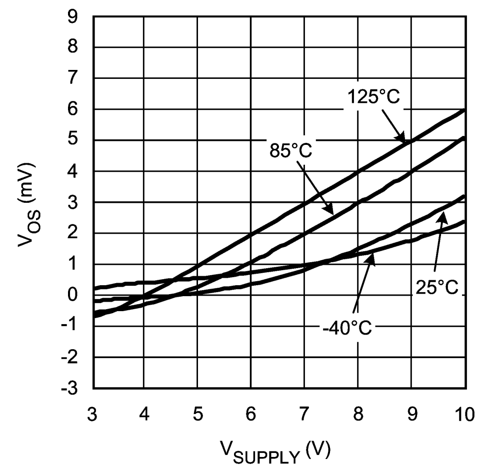
V_{OS} vs. V_{SUPPLY} for Unit 2



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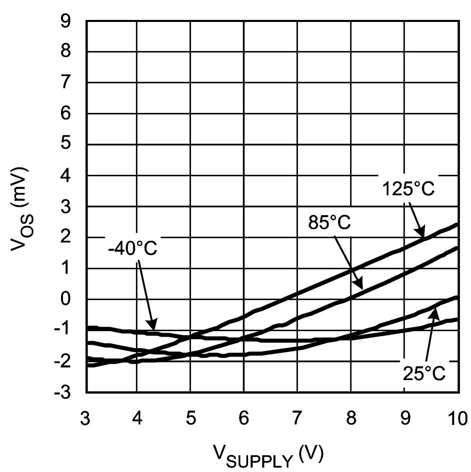
V_{OS} vs. V_{SUPPLY} for Unit 3



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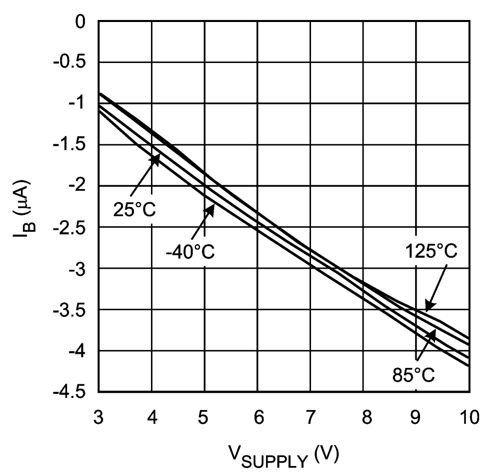
I_B vs. V_{SUPPLY} (Note 10)



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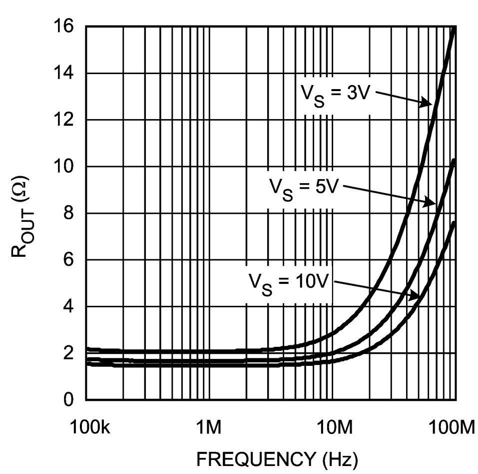
R_{OUT} vs. Frequency



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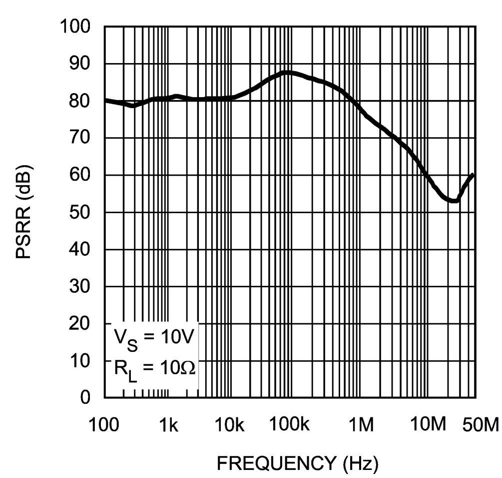
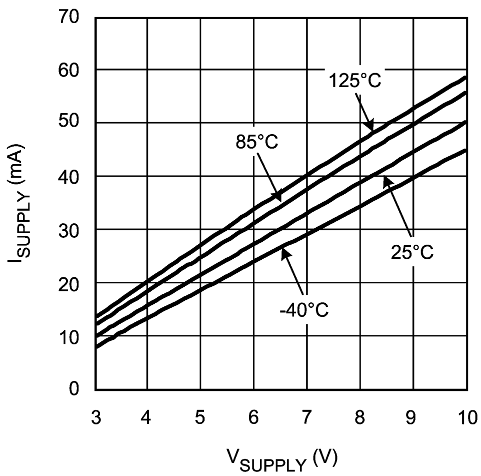
PSRR vs. Frequency



20064222

Typical Performance Characteristics
At T_J = 25˚C, V^+ = +5V, V^- = −5V; unless otherwise specified. (Continued)

I_{SUPPLY} vs. V_{SUPPLY}



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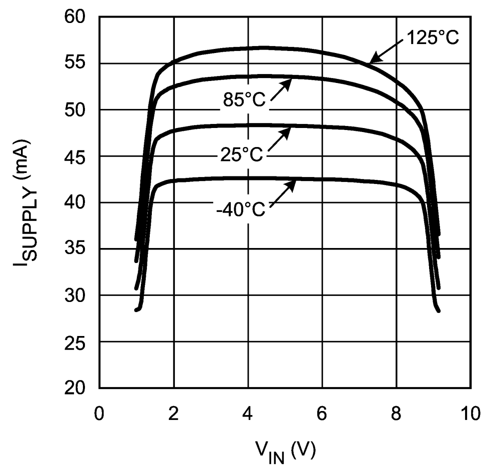
I_{SUPPLY} vs. V_{IN}



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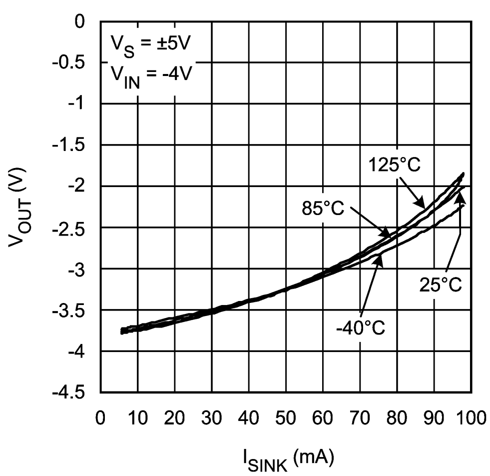
V_{OUT} vs. I_{OUT} (Sinking)



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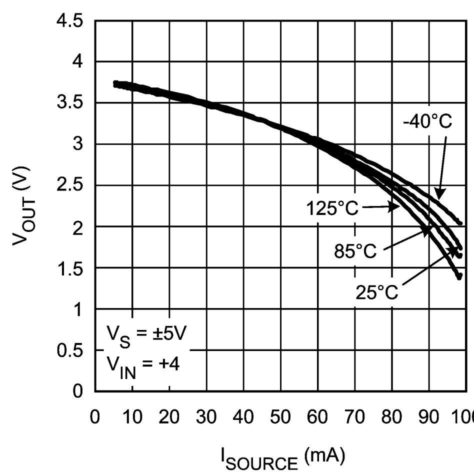
V_{OUT} vs. I_{OUT} (Sourcing)



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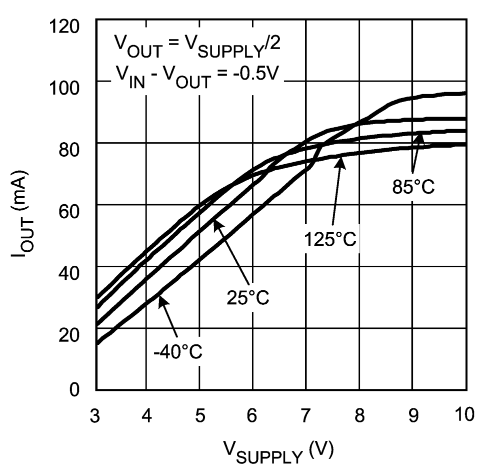
I_{OUT} Sinking vs. V_{SUPPLY}



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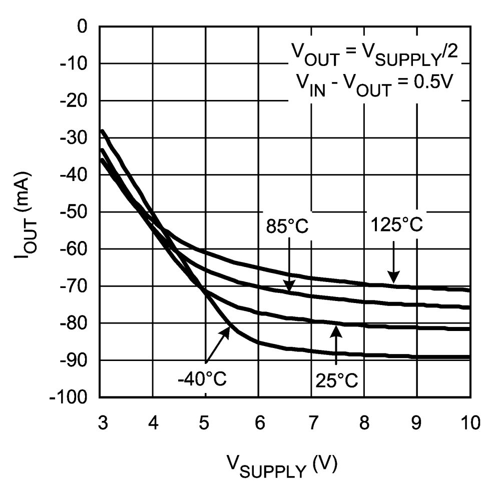
I_{OUT} Sourcing vs. V_{SUPPLY}



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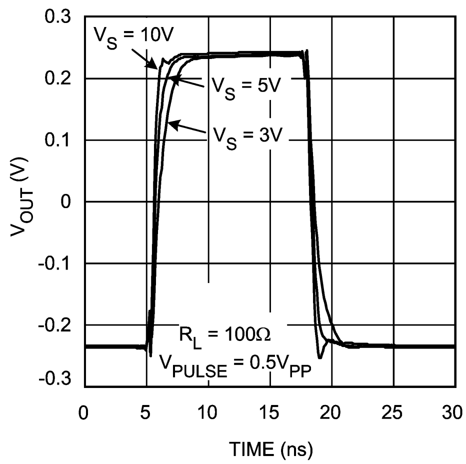
Typical Performance Characteristics At T_J = 25˚C, V^+ = +5V, V^- = −5V; unless otherwise specified. (Continued)

Small Signal Pulse Response



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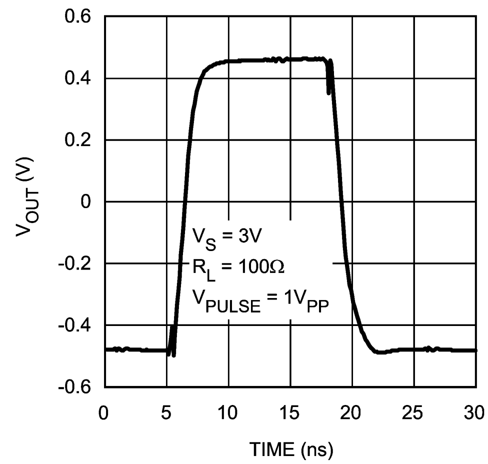
Large Signal Pulse Response @ V_S = 3V



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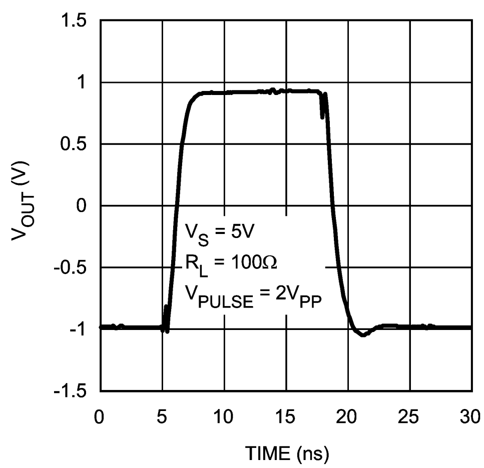
Large Signal Pulse Response @ V_S = 5V



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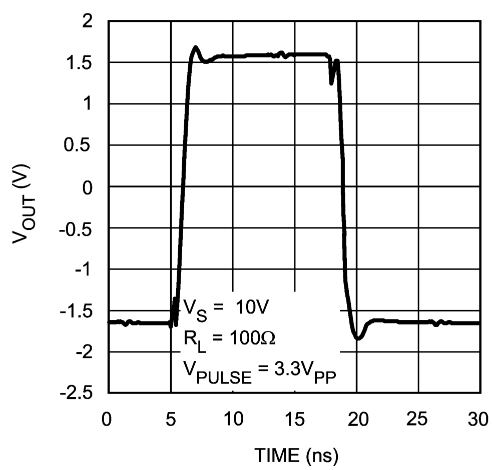
Large Signal Pulse Response @ V_S = 10V



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Application Notes

USING BUFFERS

A buffer is an electronic device delivering current gain but no voltage gain. It is used in cases where low impedances need to be driven and more drive current is required. Buffers need a flat frequency response and small propagation delay. Furthermore, the buffer needs to be stable under resistive, capacitive and inductive loads. High frequency buffer applications require that the buffer be able to drive transmission lines and cables directly.

IN WHAT SITUATION WILL WE USE A BUFFER?

In case of a signal source not having a low output impedance one can increase the output drive capability by using a buffer. For example, an oscillator might stop working or have frequency shift which is unacceptably high when loaded heavily. A buffer should be used in that situation. Also in the case of feeding a signal to an A/D converter it is recommended that the signal source be isolated from the A/D converter. Using a buffer assures a low output impedance, the delivery of a stable signal to the converter, and accommodation of the complex and varying capacitive loads that the A/D converter presents to the Op Amp. Optimum value is often found by experimentation for the particular application.

The use of buffers is strongly recommended for the handling of high frequency signals, for the distribution of signals through transmission lines or on pcb's, or for the driving of external equipment. There are several driving options:

- Use one buffer to drive one transmission line (see *Figure 1*)
- Use one buffer to drive to multiple points on one transmission line (see *Figure 2*)
- Use one buffer to drive several transmission lines each driving a different receiver. (see *Figure 3*)

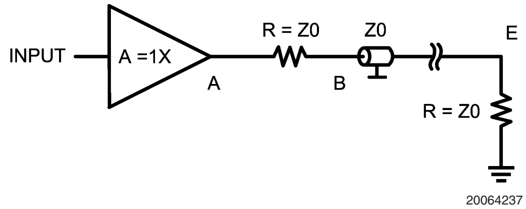


FIGURE 1.

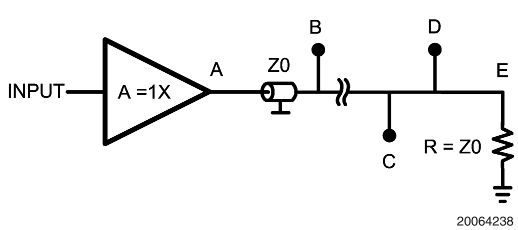


FIGURE 2.

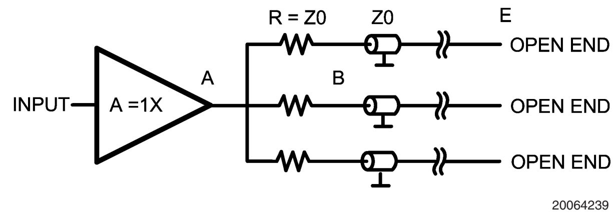


FIGURE 3.

In these three options it is seen that there is more than one preferred method to reach an (end) point on a transmission line. Until a certain point the designer can make his own choice but the designer should keep in mind never to break the rules about high frequency transport of signals. An explanation follows in the text below.

TRANSMISSION LINES

Introduction to transmission lines. The following is an overview of transmission line theory. Transmission lines can be used to send signals from DC to very high frequencies. At all points across the transmission line, Ohm's law must apply. For very high frequencies, parasitic behavior of the PCB or cable comes into play. The type of cable used must match the application. For example an audio cable looks like a coax cable but is unusable for radar frequencies at 10GHz. In this case one have to use special coax cables with lower attenuation and radiation characteristics.

Normally a pcb trace is used to connect components on a pcb board together. An important consideration is the amount of current carried by these pcb traces. Wider pcb traces are required for higher current densities and for applications where very low series resistance is needed. When routed over a ground plane, pcb traces have a defined characteristic impedance. In many design situations characteristic impedance is not utilized. In the case of high frequency transmission, however it is necessary to match the load impedance to the line characteristic impedance (more on this later). Each trace is associated with a certain amount of series resistance and series inductance and also exhibits parallel capacitance to the ground plane. The combination of these parameters defines the line's characteristic impedance. The formula with which we calculate this impedance is as follows:

$Z_0 = \sqrt{(L/C)}$

In this formula L and C are the value/unit length, and R is assumed to be zero. C and L are unknown in many cases so we have to follow other steps to calculate the Z_0. The characteristic impedance is a function of the geometry of the cross section of the line. In (*Figure 4*) we see three cross sections of commonly used transmission lines.

Application Notes (Continued)

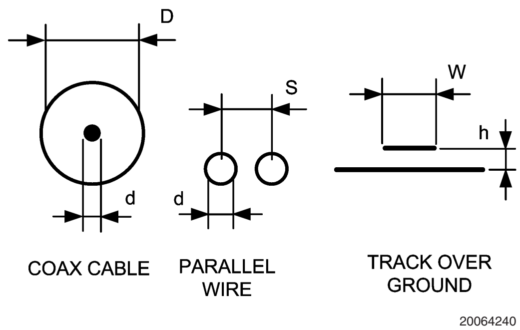


FIGURE 4.

Z_0 can be calculated by knowing some of the physical dimensions of the pcb line, such as pcb thickness, width of the trace and ϵ_r, relative dielectric constant. The formula given in transmission line theory for calculating Z_0 is as follows:

$$Z = \frac{87}{\sqrt{(\varepsilon r + 1.41)}} \times \ln \frac{(5.98 \times h)}{(th + 0.8W)} \quad (1)$$

ϵ_r relative dielectric constant

h pcb height

W trace width

th thickness of the copper

If we ignore the thickness of the copper in comparison to the width of the trace then we have the following equation:

$$Z = \frac{87}{\sqrt{(\varepsilon r + 1.41)}} \times \ln \frac{(5.98 \times h)}{(0.8W)} \quad (2)$$

With this formula it is possible to calculate the line impedance vs. the trace width. *Figure 5* shows the impedance associated with a given line width. Using the same formula it is also possible to calculate what happens when ϵ_r varies over a certain range of values. Varying the ϵ_r over a range of 1 to 10 gives a variation for the Characteristic Impedance of about 40Ω from 80Ω to 38Ω. Most transmission lines are designed to have 50Ω or 75Ω impedance. The reason for that is that in many cases the pcb trace has to connect to a cable whose impedance is either 50Ω or 75Ω. As shown ϵ_r and the line width influence this value.

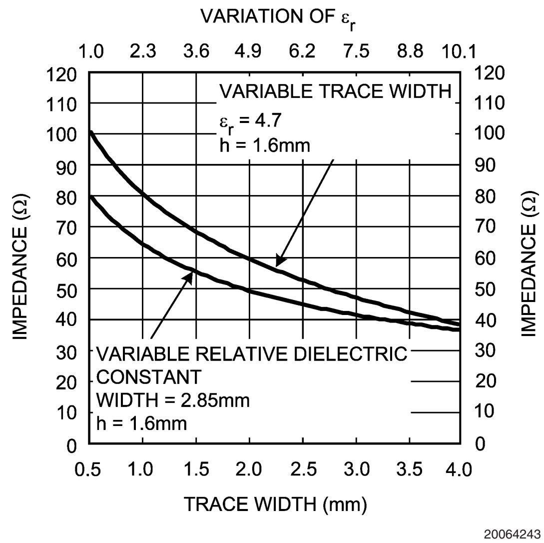


FIGURE 5.

Next, there will be a discussion of some issues associated with the interaction of the transmission line at the source and at the load.

Connecting a Load Using a Transmission Line

In most cases, it is unrealistic to think that we can place a driver or buffer so close to the load that we don't need a transmission line to transport the signal. The pcb trace length between a driver and the load may affect operation depending upon the operating frequency. Sometimes it is possible to do measurements by connecting the DUT directly to the analyzer. As frequencies become higher the short lines from the DUT to the analyzer become long lines. When this happens there is a need to use transmission lines. The next point to examine is what happens when the load is connected to the transmission line. When driving a load, it is important to match the line and load impedance, otherwise reflections will occur and this phenomena will distort the signal. If a transient is applied at T = 0 (*Figure 6*, trace A) the resultant waveform may be observed at the start point of the transmission line. At this point (begin) on the transmission line the voltage increases to (V) and the wave front travels along the transmission line and arrives at the load at T = 10. At any point across along the line I = V/Z_0, where Z_0 is the impedance of the transmission line. For an applied transient of 2V with Z_0 = 50Ω the current from the buffer output stage is 40mA. Many vintage op amps cannot deliver this level of current because of an output current limitation of about 20mA or even less. At T = 10 the wave front arrives at the load. Since the load is perfectly matched to the transmission line all of the current traveling across the line will be absorbed and there will be no reflections. In this case source and load voltages are exactly the same. When the load and the transmission line have unequal values of impedance a different situation results. Remember there is another basic which says that energy cannot be lost. The power in the transmission line is P = V^2/R. In our example the total power is 2^2/50 = 80mW. Assume a load of 75Ω. In that case a power of 80mW arrives at the 75Ωload and causes a voltage of the proper amplitude to maintain the incoming power.

Application Notes (Continued)

$$V = \sqrt{(P \times R)} = \sqrt{(80 \times 10^{-3} \times 75)} = 2.45V \quad (3)$$

The voltage wavefront of 2.45V will now set about traveling back over the transmission line towards the source, thereby resulting in a reflection caused by the mismatch. On the other hand if the load is less then 50Ω the backwards traveling wavefront is subtracted from the incoming voltage of 2V. Assume the load is 40Ω. Then the voltage across the load is:

$$\sqrt{(80 \times 10^{-3} \times 40)} = 1.79V \quad (4)$$

This voltage is now traveling backwards through the line toward the start point. In the case of a sinewave interferences develop between the incoming waveform and the backwards-going reflections, thus distorting the signal. If there is no load at all at the end point the complete transient of 2V is reflected and travels backwards to the beginning of the line. In this case the current at the endpoint is zero and the maximum voltage is reflected. In the case of a short at the end of the line the current is at maximum and the voltage is zero.

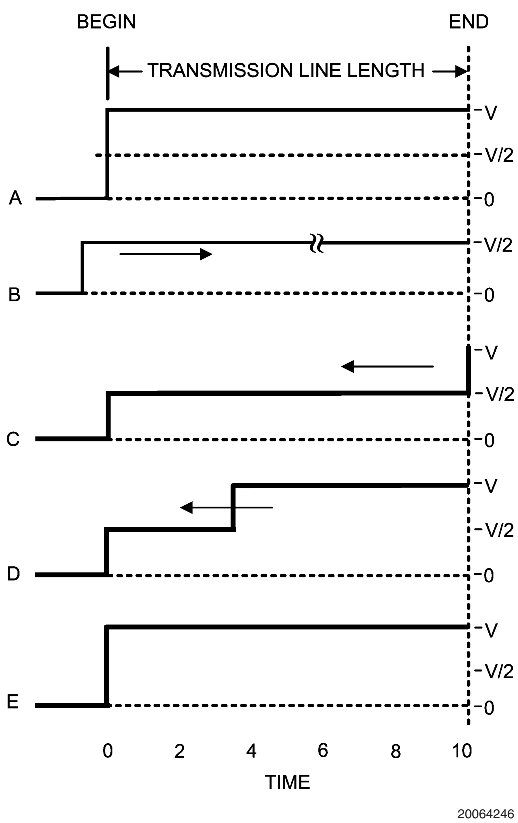


FIGURE 6.

Using Serial and Parallel Termination

Many applications, such as video, use a series resistance between the driver and the transmission line (see *Figure 1*). In this case the transmission line is terminated with the characteristic impedance at both ends of the line. See *Figure 6* trace B. The voltage traveling through the transmission line is half the voltage seen at the output of the buffer, because the series resistor in combination with Z_0 forms a two-to-on voltage divider. The result is a loss of 6dB. For video applications, amplifier gain is set to 2 in order to realize an overall gain of 1. Many operational amplifiers have a relatively flat frequency response when set to a gain of two compared to unity gain. In trace B it is seen that, if the voltage reaches the end of the transmission line, the line is perfectly matched and no reflections will occur. The end point voltage stays at half the output voltage of the opamp or buffer.

Driving More Than One Input

Another transmission line possibility is to route the trace via several points along a transmission line (see *Figure 2*). This is only possible if care is taken to observe certain restrictions. Failure to do so will result in impedance discontinuities that will cause distortion of the signal. In the configuration of *Figure 2* there is a transmission line connected to the buffer output and the end of the line is terminated with Z_0. We have seen in the section 'Connecting a load using a transmission line' that for the condition above, the signal throughout the entire transmission line has the same value, that the value is the nominal value initiated by the opamp output, and no reflections occur at the end point. Because of the lack of reflections no interferences will occur. Consequently the signal has every where on the line the same amplitude. This allows the possibility of feeding this signal to the input port of any device which has high ohmic impedance and low input capacitance. In doing so keep in mind that the transient arrives at different times at the connected points in the transmission line. The speed of light in vacuum, which is about 3 * 10^8m/sec, reduces through a transmission line or a cable down to a value of about 2 * 10^8m/sec. The distance the signal will travel in 1ns is calculated by solving the following formula:

$$S = V*t$$

Where

S = distance
V = speed in the cable
T = time

This calculation gives the following result:

$s = 2*10^8 * 1*10^{-9} = 0.2m$

That is for each nanosecond the wave front shifts 20cm over the length of the transmission line. Keep in mind that in a distance of just 2cm the time displacement is already 100ps.

Using Serial Termination To More Than One Transmission Line

Another way to reach several points via a transmission line is to start several lines from one buffer output (see *Figure 3*). This is possible only if the output can deliver the needed current into the sum of all transmission lines. As can be seen in this figure there is a series termination used at the beginning of the transmission line and the end of the line has no termination. This means that only the signal at the endpoint is usable because at all other points the reflected signal will cause distortion over the line. Only at the endpoint will the measured signal be the same as at the startpoint. Referring to *Figure 6* trace C, the signal at the beginning of the line has a value of V/2 and at T = 0 this voltage starts traveling towards the end of the transmission line. Once at the endpoint the line has no termination and 100% reflection will occur. At T = 10 the reflection causes the signal to jump to 2V and to start traveling back along the line to the buffer (see *Figure 6* trace D). Once the wavefront reaches the series

Application Notes (Continued)

termination resistor, provided the termination value is Z_0, the wavefront undergoes total absorption by the termination. This is only true if the output impedance of the buffer/driver is low in comparison to the characteristic impedance Z_0. At this moment the voltage in the whole transmission line has the nominal value of 2V (see *Figure 6* trace E). If the three transmission lines each have a different length the particular point in time at which the voltage at the series termination resistor jumps to 2V is different for each case. However, this transient is not transferred to the other lines because the output of the buffer is low and this transient is highly attenuated by the combination of the termination resistor and the output impedance of the buffer. A simple calculation illustrates the point. Assume that the output impedance is 5Ω. For the frequency of interest the attenuation is V_B/V_A=55/5 =11, where A and B are the points in *Figure 3*. In this case the voltage caused by the reflection is 2/11 = 0.18V. This voltage is transferred to the remaining transmission lines in sequence and following the same rules as before this voltage is seen at the end points of those lines. The lower the output resistance the higher the decoupling between the different lines. Furthermore one can see that at the endpoint of these transmission lines there is a normal transient equal to the original transient at the beginning point. However at all other points of the transmission line there is a step voltage at different distances from the startpoint depending at what point this is measured (see trace D).

Measuring the Length of a Transmission Line

An open transmission line can be used to measure the length of a particular transmission line. As can be seen in *Figure 7*. The line of interest has a certain length. A transient is applied at T = 0 and at that point in time the wavefront starts traveling with an amplitude of V/2 towards the end of the line where it is reflected back to the startpoint.

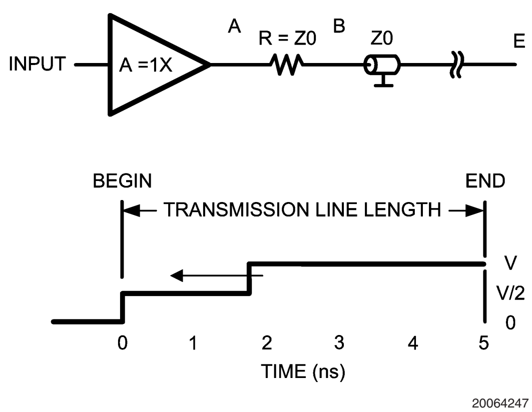


FIGURE 7.

To calculate the length of the line it is necessary to measure immediately after the series termination resistor. The voltage at that point remains at half nominal voltage, thus V/2, until the reflection returns and the voltage jumps to V. During an interval of 5 ns the signal travels to the end of the line where the wave front is reflected and returns to the measurement point. During the time interval when the wavefront is traveling to the end of the transmission line and back the voltage has a value of V/2. This interval is 10ns. The length can be calculated with the following formula: S = (V*T)/2

$$S = \frac{(2 \times 10^8) \times (10 \times 10^{-9})}{2} = 1\text{mtr} \tag{5}$$

As calculated before in the section *'Driving more than one input'* the signal travels 20cm/ns so in 5ns this distance indicated distance is 1m. So this example is easily verified.

APPLYING A CAPACITIVE LOAD

The assumption of pure resistance for the purpose of connecting the output stage of a buffer or opamp to a load is appropriate as a first approximation. Unfortunately that is only a part of the truth. Associated with this resistor is a capacitor in parallel and an inductor in series. Any capacitance such as C1-1 which is connected directly to the output stage is active in the loop gain as see in *Figure 8*. Output capacitance, present also at the minus input in the case of a buffer, causes an increasing phase shift leading to instability or even oscillation in the circuit.

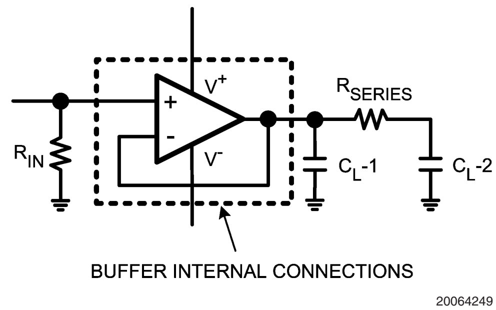


FIGURE 8.

Unfortunately the leads of the output capacitor also contain series inductors which become more and more important at high frequencies. At a certain frequency this series capacitor and inductor forms an LC combination which becomes series resonant. At the resonant frequency the reactive component vanishes leaving only the ohmic resistance (R-1 or R-2) of the series L/C combination. (see *Figure 9*).

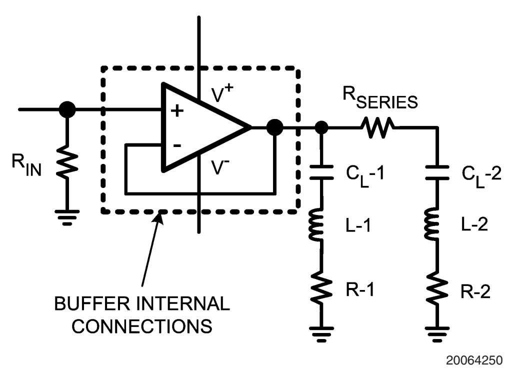


FIGURE 9.

Consider a frequency sweep over the entire spectrum for which the LMH6559 high frequency buffer is active. In the first instance peaking occurs due to the parasitic capacitance connected at the load whereas at higher frequencies the effects of the series combination of L and C become

Application Notes (Continued)

noticeable. This causes a distinctive dip in the output frequency sweep and this dip varies depending upon the particular capacitor as seen in *Figure 10*.

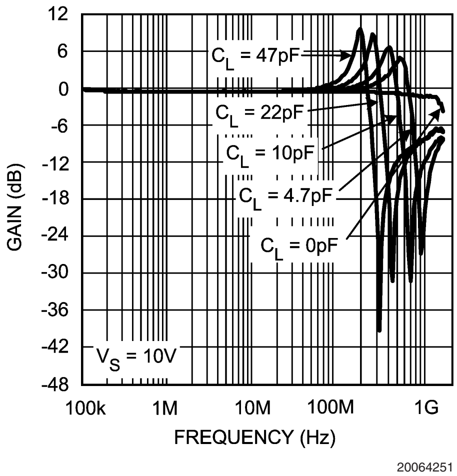


FIGURE 10.

To minimize peaking due to C_L a series resistor for the purpose of isolation from the output stage should be used. A low valued resistor will minimize the influence of such a load capacitor. In a 50Ω system as is common in high frequency circuits a 50Ω series resistor is often used. Usage of the series resistor, as seen in *Figure 11* eliminates the peaking but not the dip. The dip will vary with the particular capacitor. Using a resistor in series with a capacitor creates a rolloff of 6db/octave. Choice of a higher valued resistor, for example 500Ω to 1kΩ, and a capacitor of hundreds of pf's provides the expected response at lower frequencies. However, at high frequencies the internal inductance is appreciable and forms with the capacitor a series LC combination.

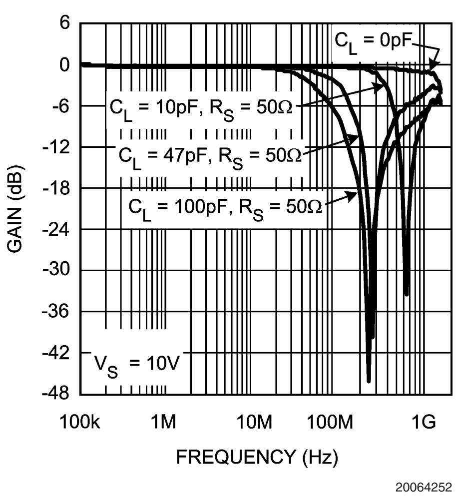


FIGURE 11.

USING GROUND PLANES

A ground plane on a printed circuit board provides for a low ohmic connection everywhere on the board for use in connecting supply voltages or grounds. Multilayer boards often make use of inner conductive layers for routing supply voltages. These supply voltage layers form a complete plane rather than using discrete traces to connect the different points together for the specified supply. Signal traces on the other hand are routed on outside layers both top and bottom. This allows for easy access for measurement purposes. Fortunately, only very high density boards have signal layers in the middle of the board. In an earlier section, the formula for Z was derived as:

$$Z = \frac{87}{\sqrt{(\varepsilon r + 1.41)}} \times \ln \frac{(5.98 \times h)}{(0.8W)} \tag{6}$$

The width of a trace is determined by the thickness of the board. In the case of a multilayer board the thickness is the space between the trace and the first supply plane under this trace layer. By common practice, layers do not have to be evenly divided in the construction of a pcb. Refer to *Figure 12*. The design of a transmission line design over a pcb is based upon the thickness of the different internal layers and the εr of the board material. The pcb manufacturer can supply information about important specifications. For example, a nominal 1.6mm thick pcb produces a 50Ω trace for a calculated width of 2.9mm. If this layer has a thickness of 0.35mm and for the same εr, the trace width for 50Ω should be of 0.63mm, as calculated from Equation 7, a derivation from Equation 6.

$$w = \frac{5.98 \times h}{e^A}$$

$$\text{where } A = \frac{\left[Z_O \times \sqrt{(\varepsilon_r + 1.41)}\right]}{87} \tag{7}$$

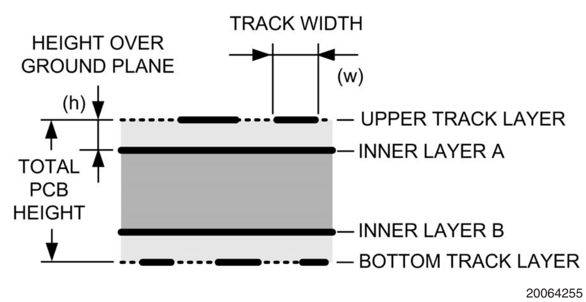


FIGURE 12.

Using a trace over a ground plane has big advantages over the use of a standard single or double sided board. The main advantage is that the electric field generated by the signal transported over this trace is fixed between the trace and the ground plane e.g. there is almost no possibility of radiation.

Application Notes (Continued)

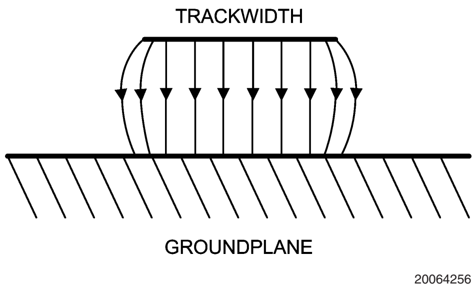


FIGURE 13.

This effect works to both sides because the circuit will not generate radiation but the circuit is also not sensible if exposed to a certain radiation level. The same is also noticeable when placing components flat on the printed circuit board. Standard through hole components when placed upright can act as antennae causing electric fields which can be picked up by a nearby upright component. If placed directly at the surface of the pcb this influence is much lower.

The Effect of Variation For ϵ_r

When using pcb material the ϵ_r has a certain shift over the used frequency spectrum, so if it is necessary to work with very accurate trace impedances, one must take into account the frequency region for which the design is to be functional. *Figure 14* http://www.isola.de gives an example of what the drift in ϵ_r will be when using the pcb material produced by Isola. If working at frequencies of 100MHz then a 50Ω trace has a width of 3.04mm for standard 1.6mm FR4 pcb material, and the same trace needs a width of 3.14mm. for frequencies around 10GHz.

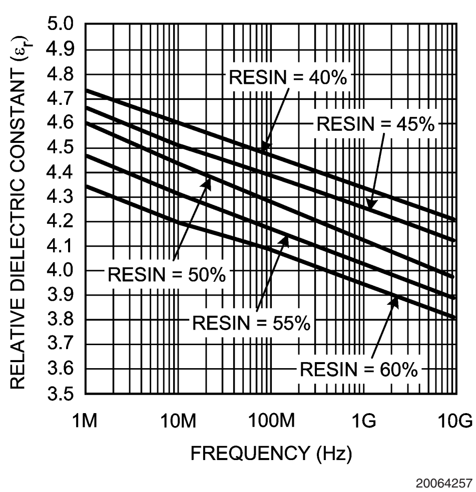


FIGURE 14.

Routing Power Traces

Power line traces routed over a pcb should be kept together for best practice. If not a ground loop will occur which may cause more sensitivity to radiation. Also additional ground trace length may lead to more ringing on digital signals. Careful attention to power line distribution leads to improved overall circuit performance. This is especially valid for analog circuits which are more sensitive to spurious noise and other unwanted signals.

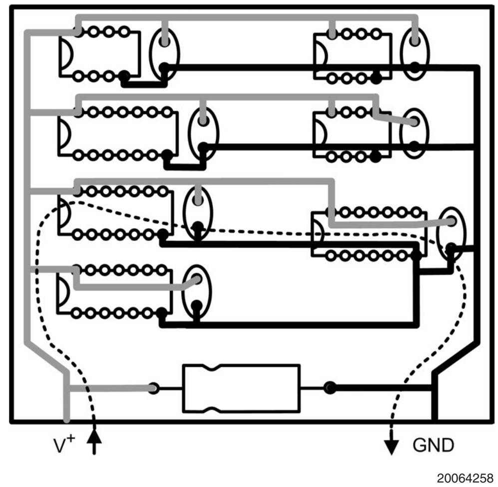


FIGURE 15.

As demonstrated in *Figure 15* the power lines are routed from both sides on the pcb. In this case a current loop is created as indicated by the dotted line. This loop can act as an antenna for high frequency signals which makes the circuit sensitive to R_F radiation. A better way to route the power traces can be seen in the following setup. (see *Figure 16*).

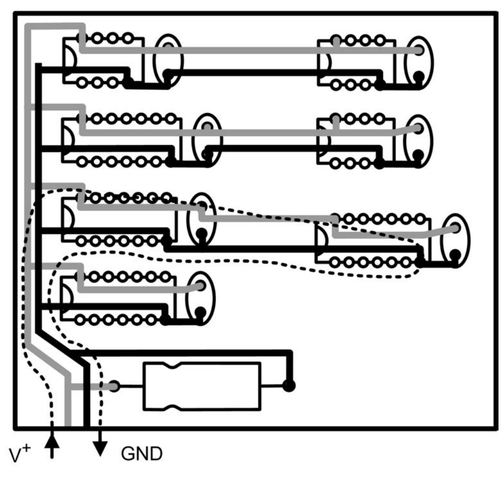


FIGURE 16.

In this arrangement the power lines have been routed in order to avoid ground loops and to minimize sensitivity to noise etc. The same technique is valid when routing a high frequent signal over a board which has no ground plane. In that case is it good practice to route the high frequency signal alongside a ground trace. A still better way to create a pcb carrying high frequency signals is to use a pcb with ground a ground plane or planes.

Application Notes (Continued)

Discontinuities in a Ground Plane

A ground plane with traces routed over this plane results in the build up of an electric field between the trace and the ground plane as seen in *Figure 13*. This field is build up over the entire routing of the trace. For the highest performance the ground plane should not be interrupted because to do so will cause the field lines to follow a roundabout path. In *Figure 17* it was necessary to interrupt the ground plane with the blue crossing trace. This interruption causes the return current to follow a longer route than the signal path follows to overcome the discontinuity.

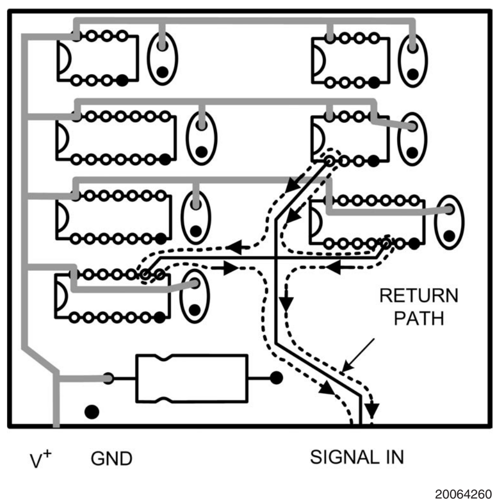


FIGURE 17.

If needed it is possible to bypass the interruption with traces that are parallel to the signal trace in order to reduce the negative effects of the discontinuity in the ground plane. In doing so, the current in the ground plane closely follows the signal trace on the return path as can be seen in *Figure 18*. Care must be taken not to place too many traces in the ground plane or the ground plane effectively vanishes such that even bypasses are unsuccessful in reducing negative effects.

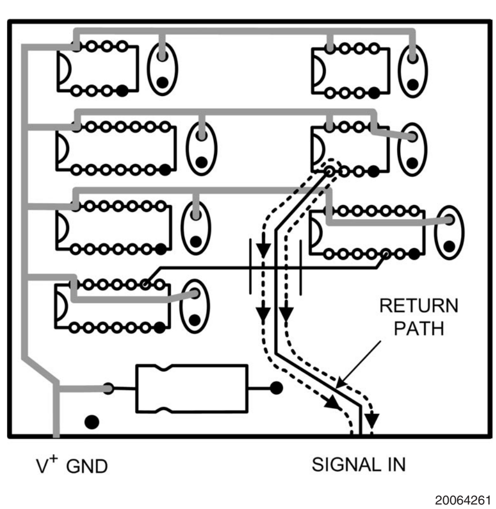


FIGURE 18.

If the overall density becomes too high it is better to make a design which contains additional metal layers such that the ground planes actually function as ground planes. The costs for such a pcb are increased but the payoff is in overall effectiveness and ease of design.

Ground Planes at Top and Bottom Layer of a PCB

In addition to the bottom layer ground plane another useful practice is to leave as much copper as possible at the top layer. This is done to reduce the amount of copper to be removed from the top layer in the chemical process. This causes less pollution of the chemical baths allowing the manufacturer to make more pcb's with a certain amount of chemicals. Connecting this upper copper to ground provides additional shielding and signal performance is enhanced. For lower frequencies this is specifically true. However, at higher frequencies other effects become more and more important such that unwanted coupling may result in a reduction in the bandwidth of a circuit. In the design of a test circuit for the LMH6559 this effect was clearly noticeable and the useful bandwidth was reduced from 1500MHz to around 850MHz.

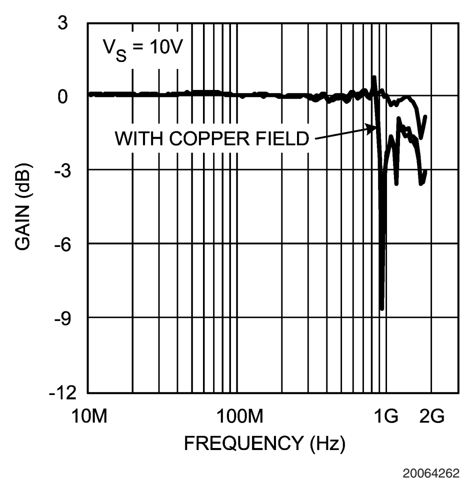


FIGURE 19.

As can be seen in *Figure 19* the presence of a copper field close to the transmission line to and from the buffer causes unwanted coupling effects which can be seen in the dip at about 850MHz. This dip has a depth of about 5dB for the case when all of the unused space is filled with copper. In case of only one area being filled with copper this dip is about 9dB.

PCB BOARD LAYOUT AND COMPONENT SELECTION

Sound practice in the area of high frequency design requires that both active and passive components be used for the purposes for which they were designed. It is possible to amplify signals at frequencies of several hundreds of MHz using standard through hole resistors. Surface mount devices, however, are better suited for this purpose. Surface mount resistors and capacitors are smaller and therefore parasitics are of lower value and therefore have less influence on the properties of the amplifier. Another important issue is the pcb itself, which is no longer a simple carrier for all the parts and a medium to interconnect them. The pcb board becomes a real component itself and consequently contributes its own high frequency properties to the overall performance of the circuit. Sound practice dictates that a

Application Notes (Continued)

design have at least one ground plane on a pcb which provides a low impedance path for all decoupling capacitors and other ground connections. Care should be taken especially that on board transmission lines have the same impedance as the cables to which they are connected - 50Ω for most applications and 75Ω in case of video and cable TV applications. Such transmission lines usually require much wider traces on a standard double sided PCB board than needed for a 'normal' trace. Another important issue is that inputs and outputs must not 'see' each other. This occurs if inputs and outputs are routed together over the pcb with only a small amount of physical separation, particularly when there is a high differential in signal level between them. If routed close together crosstalk will occur and in that case a small amount of the original signal will appear at the other trace. The same effect will occur internally in the device. This means that signal is jumping over from one buffer to the other producing a part of the signal of buffer one in the other buffers. To improve crosstalk performance it is recommended to use a grounded guard-trace between signal lines and to ground unused pins from the device package. Crosstalk becomes more and more noticeable for the higher frequencies. For frequencies below 1MHz crosstalk has a signal level as low as −70dB below the incoming signal. For higher frequencies crosstalk will degrade until about −35dB at 100MHz. (see typical performance characteristics) The best way to see this, is applying a pulse to one of the buffers and looking at the output of one of the others. The flat portion of such a pulse represents the lowest frequencies which are highly suppressed and the edge of the incoming pulse representing the highest frequencies will appear at the output. For reducing the effect of crosstalk it is recommended to terminate unused inputs and outputs with a low ohmic resistor such as 50Ω for an input or 100Ω for an output to ground. While measuring the crosstalk, signal was applied to buffer 2 which output was terminated with 100Ω, while measuring the crosstalk output signal at buffer 3, which input was terminated with a resistor of 50Ω.

Furthermore components should be placed as flat and low as possible on the surface of the PCB. For higher frequencies a long lead can act as a coil, a capacitor or an antenna. A pair of leads can even form a transformer. Careful design of the pcb avoids oscillations or other unwanted behaviors. For ultra high frequency designs only surface mount components will give acceptable results. (for more information see OA-15).

NSC suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization.

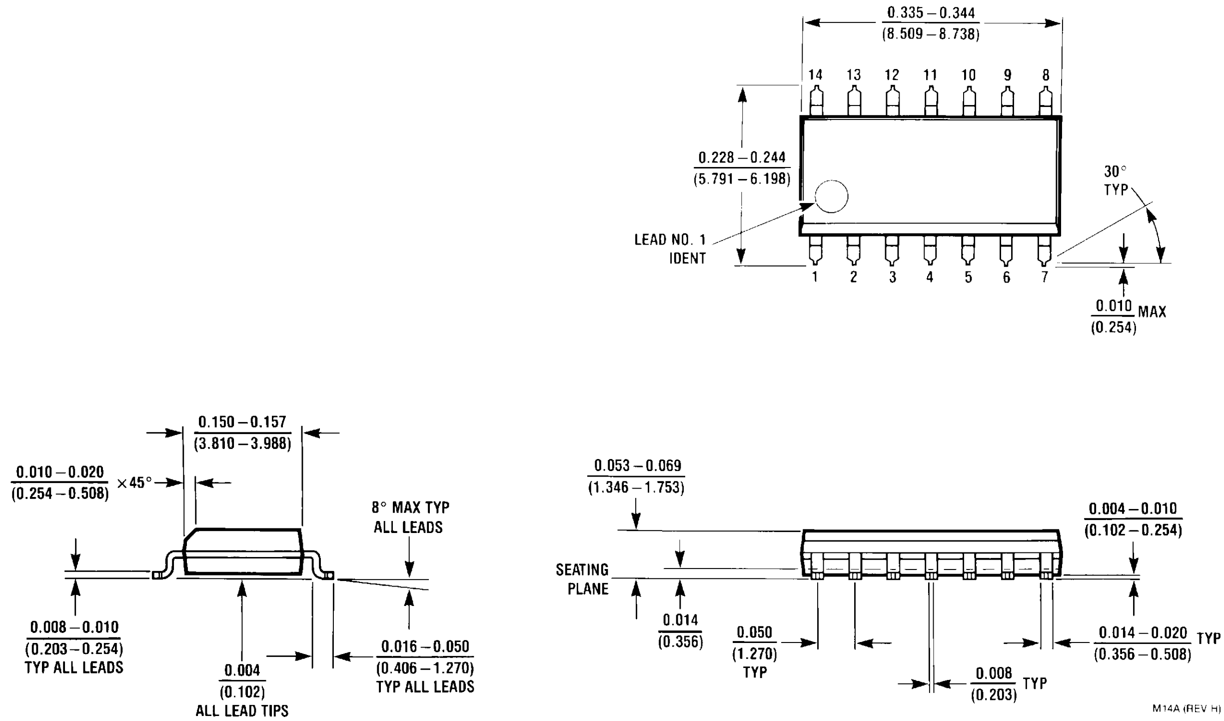
Device	**Package**	**Evaluation board Part Number**
LMH6560MA	SOIC-14	CLC730145
LMH6560MT	TSSOP-14	CLC730132

These free evaluation boards are shipped when a device sample request is placed with National Semiconductor.

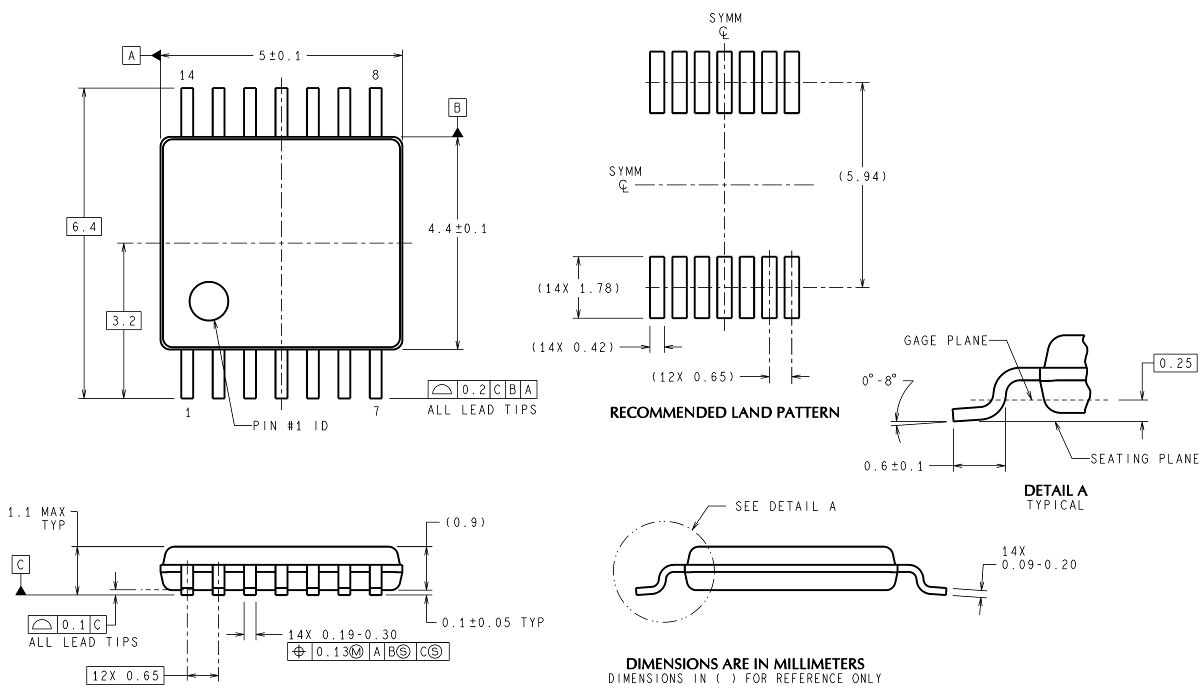
POWER SEQUENCING OF THE LMH6560

Caution should be used in applying power to the LMH6560. When the negative power supply pin is left floating it is recommended that other pins, such as positive supply and signal input should also be left unconnected. If the ground is floating while other pins are connected the input circuitry is effectively biased to ground, with a mostly low ohmic resistor, while the positive power supply is capable of delivering significant current through the circuit. This causes a high input bias current to flow which degrades the input junction. The result is an input bias current which is out of specification. When using inductive relays in an application care should be taken to connect first both power connections before connecting the bias resistor to the input.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Pin SOIC
NS Package Number M14A



14-Pin TSSOP
NS Package Number MTC14

Notes

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