Low Noise, 90 MHz Variable-Gain Amplifier Evaluation Board

AD603-EB

GENERAL CONSIDERATIONS

The AD603 Evaluation Board is designed to enable rapid evaluation of the major features of the AD603. Built-in flexibility allows convenient reconfiguration to accommodate most of the intended operating configurations.

The power supplies as indicated on the silkscreen should be ±5 V. The part has an absolute maximum supply voltage rating of ±7.5 V, so care should be exercised not to overvoltage the part. The part draws about 20 mA of quiescent current from each supply.

The input is terminated with 100 Ω (R101). This along with the internal input resistance of 100 Ω provides a 50 Ω input impedance looking into the input port for proper match to a 50 Ω source. The input is ac coupled by C101.

The output has a series resistor (R103) of 49.9 Ω that serves as a back termination for driving 50 Ω transmission lines. It is also ac coupled.

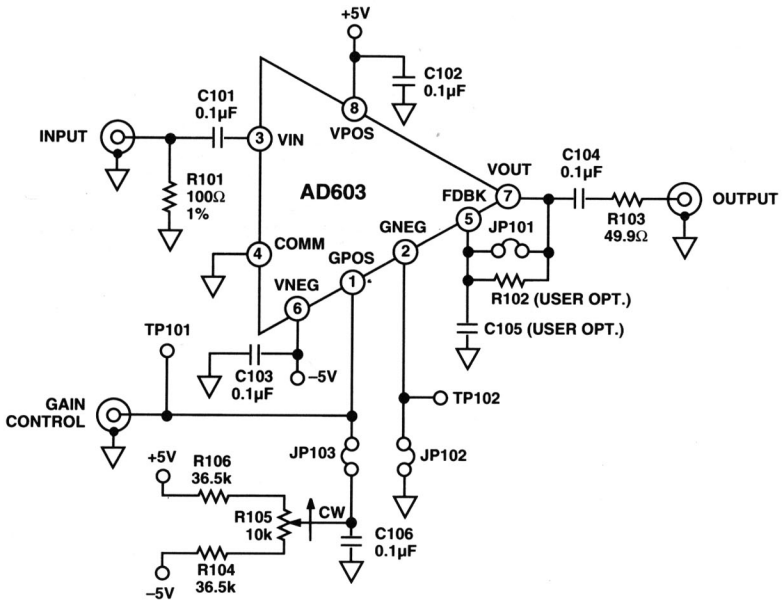
An uncommitted field of holes on a 0.1 in. grid is provided for generic breadboarding purposes. All of the individual holes are floating except for the three columns that are labeled as power supplies.

GAIN CONTROL

The gain of the AD603 Evaluation Board can be controlled in several ways. For static gain control, the on-board potentiometer R105 can be used to conveniently vary the gain over the entire range. R105 can provide a single-ended control voltage from about –650 mV to +650 mV when the supplies are set at ±5 V. This provides about 150 mV of overdrive in each direction.

To use R105 to control the gain, JP102 and JP103 must be installed. JP102 ties GNEG to ground, while JP103 connects GPOS to the wiper of R105. There should be no active connection to J103, but this can provide a convenient connection to monitor the control voltage. Turning R105 clockwise increases the gain.

The GAIN CONTROL input can be dynamically driven single-ended, ground-referenced through the gain control BNC connector (J103) by leaving the short across JP102 installed and removing JP103. In this configuration, a higher voltage on the gain control input corresponds to higher gain. Minimum (specified) gain is realized when V_{GC} = –500 mV, while maximum gain corresponds to a V_{GC} of +500 mV.



Evaluation Board Schematic

REV. B

One Technology Way, P.O. Box 9106, Norwood. MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

The gain control can be operated in an inverted sense (to the magnitude of the gain) or operated at a different common mode voltage. Connections to TP101 and TP102 can be used for access to the differential inputs of the Gain Control port for a more generalized configuration.

The short across JP102 should be removed if GNEG is not to be tied to ground. JP103 can be left connected to use R105 to dc bias GPOS. Otherwise JP103 should be removed and GPOS can be controlled by means of another connection. The differential Gain Control inputs are high impedance and can be operated at any voltage within the common-mode range of –1.2 V to +2.0 V.

GAIN RANGES

The AD603 has built-in features for configuration of two specific gain ranges without the use of external parts. As these gain ranges are determined by the ratios of on-chip resistors, gain accuracy is closely controlled.

Installing the short across JP101 (Pin 5 FDBK, and Pin 7, VOUT) sets the device in its minimum gain configuration with the widest bandwidth. The gain range in this configuration is from –10 dB to +30 dB, and the 3 dB bandwidth is 90 MHz. (See AD603 data sheet Figure 2a.)

Removing the short across JP101 sets the AD603 in its maximum (practical) gain configuration with the minimum band width. The gain range in this configuration is from +10 dB to+50 dB, and the –3 dB bandwidth is 9 MHz. (See AD603 data sheet Figure 2c.) A capacitor can be installed in position C105 to improve the frequency response.

Intermediate gain ranges can be programmed by a resistor between Pins 5 and 7 (FDBK and VOUT) at position R102 on the AD603 Evaluation Board. The AD603 data sheet instructs in the proper selection of this resistor and the gain accuracy that can be expected. Note, however, that a misprint in Figure 2b in the Rev. 0 version of the data sheet indicates that the bandwidth in the 0 dB to +40 dB configuration is 45 MHz. The correct value is 25 MHz.

C1986–3–12/94

PRINTED IN U.S.A.