LP38852MR-ADJ Evaluation Board

National Semiconductor
Application Note 1560
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Introduction

This board is designed to allow the evaluation of the LP38852MR-ADJ Voltage Regulator. Each board is assembled and tested in the factory. This evaluation board has the PSOP-8 package mounted, and the output voltage is set to 1.20V.

General Description

The LP38852 is a dual-rail adjustable LDO linear regulator capable of suppling up to 1.5A of output current, and incorporates an Enable function as well as a Soft-Start function.

The device has been designed to work with 10 µF input and output ceramic capacitors, and 1µF bias capacitor. Footprints areas for C_{IN} and C_{OUT} will allow for a variety of sizes.

Operation

The input voltage, applied between V_{IN} and GND, should be at least 1.0V greater than V_{OUT} and no greater than the applied V_{BIAS} voltage.

The bias voltage, applied between V_{BIAS} and GND should be above the minimum bias voltage of 3.0V, and no more than the maximum of 5.5V.

Loads can be connected to V_{OUT} with reference to GND.

V_{OUT} and V_{IN} test points are provided on the board to allow accurate measurements directly onto the input and output pins of the device, eliminating any voltage drop on the PCB traces or connecting wires to the load.

Setting V_{OUT}

The output voltage is set using the external resistive divider R1 and R2. The output voltage is given by the formula:

$$V_{OUT} = V_{ADJ} \times (1 + (R1 / R2)) \quad (1)$$

It is recommended that the values selected for R1 and R2 are such that the parallel value is less than 10 kΩ. This is to prevent internal parasitic capacitances on the ADJ pin from interfering with the F_Z pole set by R1 and C_{FF}.

The LP38852MR-ADJ Evaluation board is assembled with a 1.40 kΩ ±1% resistor for R1, and a 1.00 kΩ ±1% resistor for R2. This sets V_{OUT} to 1.20V.

Selecting C_{FF}

A capacitor placed across the gain resistor R1 will provide additional phase margin to improve load transient response of the device. This capacitor, C_{FF}, in parallel with R1, will form a zero in the loop response given by the formula:

$$F_Z = (1 / (2 \times \pi \times C_{FF} \times R1)) \quad (2)$$

The value for C_{FF} should be selected to set a zero frequency (F_Z) between 10 kHz and 15 kHz using the formula:

$$C_{FF} = 1 / (2 \times \pi \times F_Z \times R1) \quad (3)$$

The closest standard 10% value is usually adequate for C_{FF}.

The LP38853-ADJ Evaluation board is assembled with a 0.01 µF capacitor for C_{FF}. This sets F_Z to approximately 11.4 kHz.

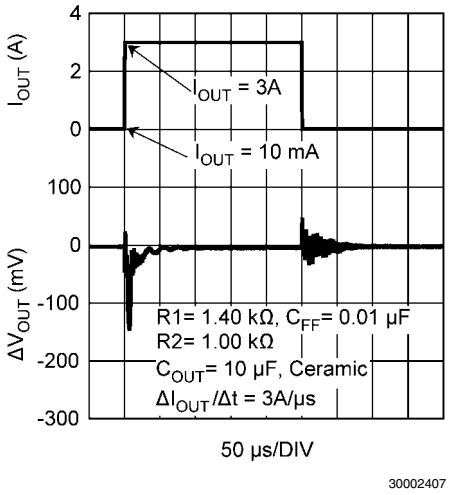


FIGURE 1. 10mA to 3A Load Transient Response

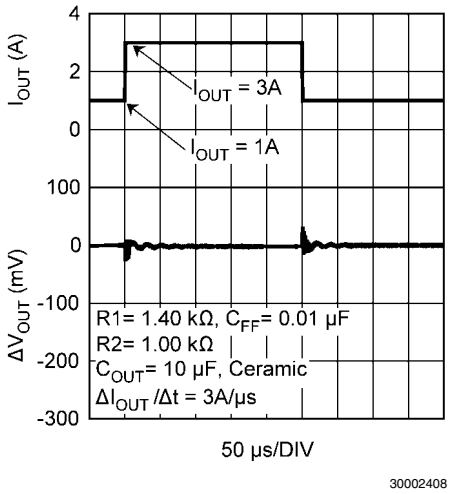


FIGURE 2. 1A to 3A Load Transient Response

Enable Function

ON/OFF control is provided by supplying a logic level signal to the Enable pin. A minimum V_{EN} value of 1.3V is typically required at this pin to enable the LDO output. The LDO output will be shutdown when the V_{EN} value is typically 1.0V or less. The V_{EN} threshold incorporates approximately 100mV of hysteresis.

In applications were the LP38852 is operated continuously the Enable pin can be connected directly to V_{BIAS}, or left open.

The Enable pin has a 200 kΩ internal resistor to V_{BIAS}. If the Enable pin is left open, care should be taken to minimize any capacitance on the Enable pin, as any capacitance will introduce an RC delay time on the Enable function.

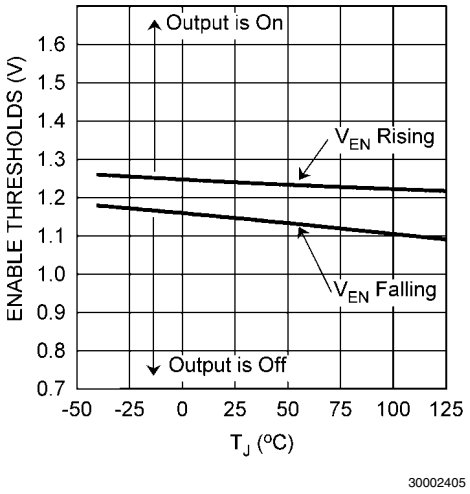


FIGURE 3. Enable Thresholds

Soft-Start Function

V_{REF} will rise at an RC rate defined by the internal resistance of the SS pin (r_{SS}), and the external capacitor (C_{SS}) connected to the SS pin. This allows the output voltage to rise in a controlled manner until steady-state regulation is achieved. Typically, five time constants are recommended to assure that the output voltage is sufficiently close to the final steady-state value. During the soft-start time the output current can rise to the built-in current limit.

The LP38852MR-ADJ Evaluation board is assembled with a 0.01 µF capacitor for C_{SS}. This sets the soft-start time to approximately 750 µs.

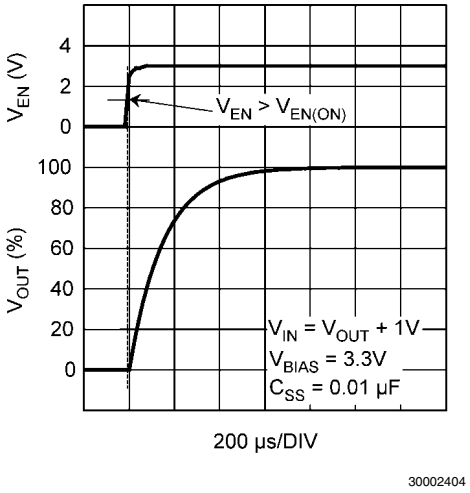


FIGURE 4. V_{OUT} Soft-Start

Power Dissipation

The LP38852MR PSOP-8 package alone has a junction to ambient thermal resistance (θ_{JA}) rating of 168°C/W. When mounted on the LP38852MR evaluation board the θ_{JA} rating is approximately 62°C/W.

Although there is only approximately 0.03 square inches (0.1 x 0.3) 1 ounce copper area immediately under the DAP, the top copper surface area is extended to additional copper area on the bottom of the board by four thermal vias.

With the 62°C/W thermal rating the LP38852MR-ADJ evaluation board will dissipate a maximum of 1.6W with T_A = 25°C.

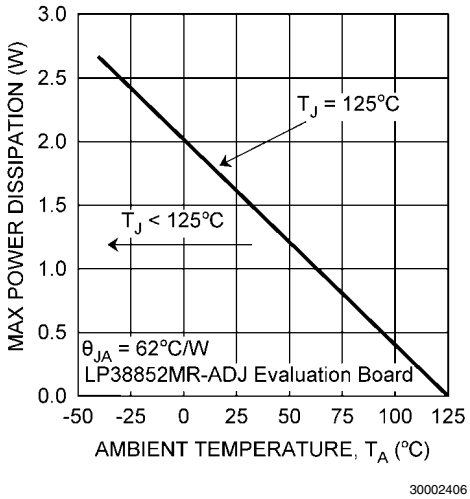
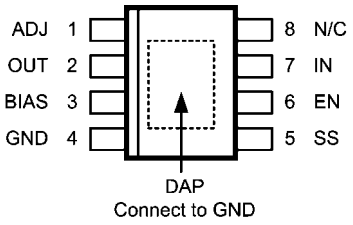
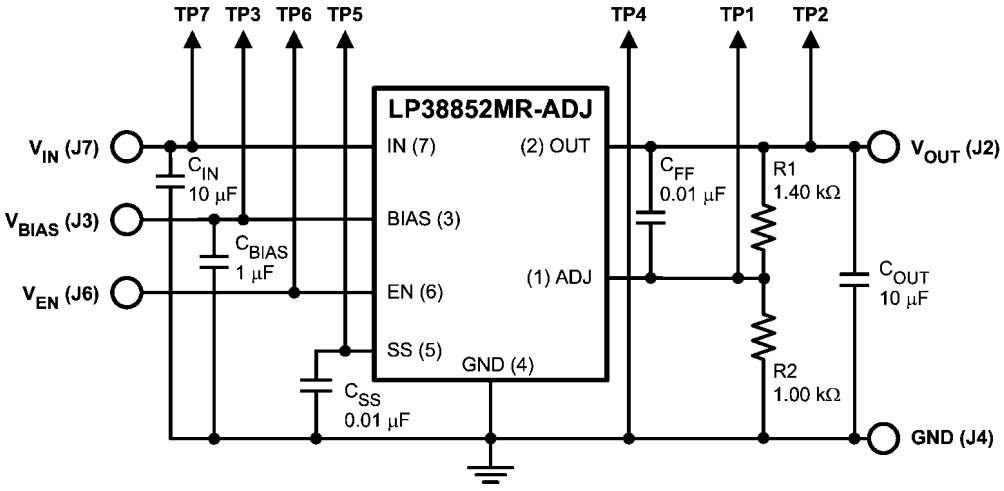


FIGURE 5. Maximum Power Dissipation vs Ambient Temperature

Connection Diagram

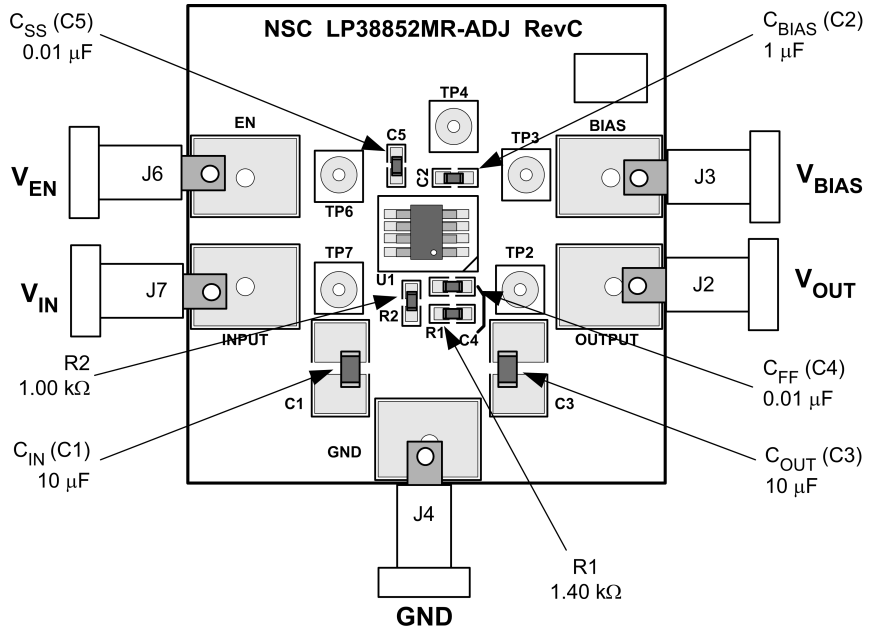


Schematic Diagram



Evaluation Board Schematic.

PCB Layout



Evaluation Board Component and Pin Layout

Bill of Materials

ID	Name	Description	Manufacturer	Part Number
U1	U1	LP38852MR-ADJ NOPB	National Semiconductor Corporation	LP38852MR-ADJ NOPB
C1	C_{IN}	Capacitor: 10 µF; ±10%; MLCC; 10V; X7R; 1210	AVX	1210ZC106KAT2A
C2	C_{BIAS}	Capacitor: 1 µF;, ±10%; MLCC; 10V; X7R; 0805		0805ZC105KAT2A
C3	C_{OUT}	Capacitor: 10 µF;, ±10%; MLCC; 10V; X7R; 1210		1210ZC106KAT2A
C4	C_{FF}	Capacitor: 0.01 µF;, ±10%; MLCC; 10V; X7R; 0805		0805YC103KAT2A
C5	C_{SS}	Capacitor: 0.01 µF; ±10%;, MLCC; 10V; X7R; 0805		0805YC103KAT2A
J2	V_{EN}	Banana Jack : Insulated Solder Terminal; White	Johnson Components	108-0901-001
J3	V_{IN}	Banana Jack : Insulated Solder Terminal; Red		108-0902-001
J4	GND	Banana Jack : Insulated Solder Terminal; Black		108-0903-001
J6	V_{OUT}	Banana Jack : Insulated Solder Terminal; Orange		108-0906-001
J7	V_{BIAS}	Banana Jack : Insulated Solder Terminal; Blue		108-0910-001
R1	R1	Resistor: 1.40 kΩ, ±1%; Thick Film; 250 mW; ±100 ppm; 0805	VISHAY DALE	CRCW 0805 1401 F
R2	R2	Resistor: 1.00 kΩ, ±1%; Thick Film; 250 mW; ±100 ppm; 0805		CRCW 0805 1001 F
TP2	TP_{EN}	Turret Terminal : Mounting Hole Diameter = 0.062”	Keystone	1593–2
TP2	TP_{SS}			
TP3	TP_{IN}			
TP4	TP_{GND}			
TP5	TP_{ADJ}			
TP6	TP_{OUT}			
TP7	TP_{BIAS}			

Notes

Notes

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