LP3996 / LP5996 Application Board Information

National Semiconductor
Application Note 1377
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General Information

This board is designed to allow the evaluation of either the LP3996 or the LP5996 Dual Voltage Regulator. Each board is pre-assembled and tested in the factory. The board contains the LP3996 / LP5996 in a 10 lead LLP package with all the associated passive components to enable all features of either device to be tested.

The LP3996 / LP5996 are Dual, Low Drop-out Voltage Regulators with independent enable pins. LDO1 can deliver a maximum current of 150mA. while LDO2 can deliver up to 300mA. The LP3996 has an $\overline{\text{ERROR}}$ Flag associated with LDO2. The flag is set to Low if LDO2 is out of regulation and by adding a capacitor between the SET pin and GND, the flag may also be used as a delayed Power-On-reset (POR), see below.

1µF ceramic capacitors are fitted from V_{IN}, V_{OUT1} and V_{OUT2} to GND.

The POR feature is not included in the LP5996. Both devices also have a Bypass pin and by connecting a capacitor (10nF typ.) to GND, the output noise can be reduced substantially.

Operation

The input voltage, applied between V_{IN} and GND, should be at least 0.5V greater than the highest V_{OUT} and no more than 6.0V. The minimum operating voltage is 2.0V. Loads can be connected to V_{O1} and V_{O2} pins with reference to GND. Internal short circuit protection is provided for each LDO. Additional sense pins, V_{INS}, V_{O1S} and V_{O2S} are provided on the board to allow accurate measurements directly on the input and output pins of the device, eliminating any voltage drop on the PCB traces or connecting wires to the loads. Input leads should be kept reasonably short to minimize inductance. If longer input leads (>1m) are required it may be necessary to increase the value of the input capacitor to 2.2µF to ensure stability.

ON/OFF control is provided by logic signals on EN1 and EN2. A minimum of 0.95V is required on these pins to enable the corresponding LDO. The LDOs will be shutdown with the enable pins set to 0.4V or less. If ON/OFF control is not required, then either or both enable pins may be connected to V_{IN}. The device has 1MΩ internal resistors from EN1 and EN2 to GND.

On the LP3996 only, the active low POR flag on LDO2 is asserted when the output of LDO2 drops below 90% (typical) of its regulated value indicating that LDO2 is out of regulation due to an overload or fault condition. During start-up, or following the removal of a fault condition, the flag will remain in the Low state until the output of LDO2 reaches 92% (typical) of its maximum value. By adding, a capacitor between the SET pin and GND, a delay can be programmed to the rising state of the POR output which may then be used as a Power-On-Reset for a micro controller within the user's application, for example. The Delay time is set by the following formula.

$$t_{DELAY} = \frac{V_{TH(SET)} \times C_{SET}}{I_{SET}}$$

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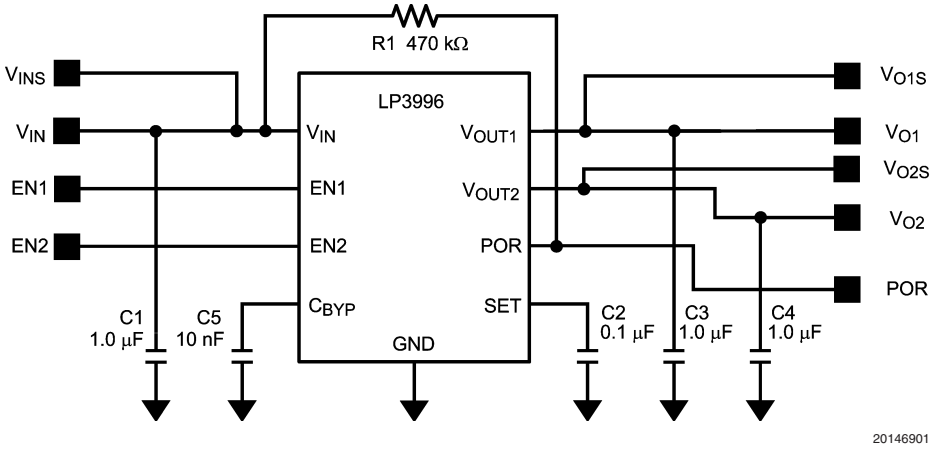
Typically, $V_{TH(DELAY)}$ is 1.25V and I_{DELAY} is 1µA. So for the 0.1µF capacitor (C2) fitted, the delay time will be around 125ms.

The POR output is an open drain NMOS transistor. It is pulled up to to V_{IN} by a 470kΩ resistor (R1) fitted to the evaluation board. Note that when the POR is in the HIGH state, any significant loading, a 1MΩ Oscilloscope input, for example, will cause the voltage to drop due the 470kΩ pull-up. A 10X probe should be used. In the LOW state, with a sink current of 250µA, the POR pin will have a level of 20mV (typical).

Output noise is minimized by the inclusion of a 10nF bypass capacitor (C5). Together with an internal resistor, this forms a low-pass filter for the internal reference voltage which reduces the noise on both V_{OUT1} and V_{OUT2}.

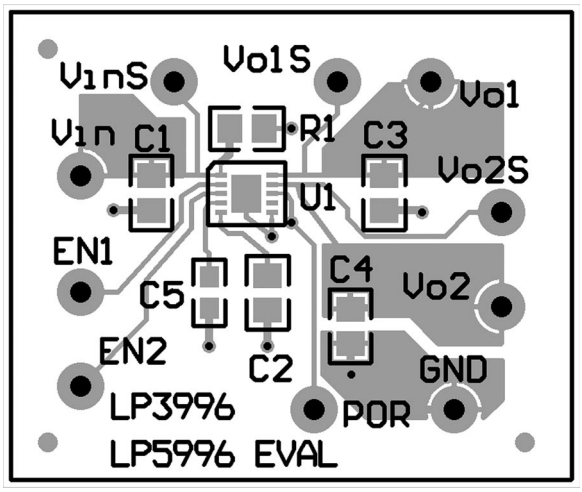
The schematic and board layout are shown below:

Schematic Diagram



Evaluation Board Schematic

PCB Layout



Evaluation Board Component and Pin Layout
Board Size:- 1.200" x 1.000"

Bill of Materials for LP3996 / LP5996 LLP Evaluation Board

Item	Manufacturer	Part #	Description
C1 (V_{IN} to GND)	Murata	GRM188R61A105K	1.0µF, 10V, X5R, 0603, 10%
C2 (V_{SET} to GND)	Murata	GRM188R61C104K	0.1µF, 16V, X5R, 0603, 10% LP3996 only.
C3 (V_{OUT1} to GND)	Murata	GRM188R61A105K	1.0µF, 10V, X5R, 0603, 10%
C4 (V_{OUT2} to GND	Murata	GRM188R61A105K	1.0µF, 10V, X5R, 0603, 10%
C5 (Bypass Capacitor)	Murata	GRM1887U1H103J	10 nF, 50V, U2J, 0603, 5%
R1 (POR Pull-up)	Vishay	CRCW06034703F	470kΩ, 0603, 1% LP3996 only.
Test Pins			

Notes

For the most current product information visit us at www.national.com.

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