

# LP38859S-1.2 Evaluation Board

National Semiconductor  
Application Note 1480  
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## Introduction

This board is designed to enable the evaluation of the LP38859 Voltage Regulator. Each board is assembled and tested in the factory. This evaluation board has the TO-263 5-lead package mounted.

## General Description

The LP38859 is a dual-rail LDO linear regulator capable of supplying up to 3A of output current, and incorporates a Soft-Start feature.

The device has been designed to work with 10  $\mu\text{F}$  input and output ceramic capacitors, and 1 $\mu\text{F}$  bias capacitors. Footprints areas for  $C_{\text{IN}}$  and  $C_{\text{OUT}}$  will allow for a variety of sizes.

## Operation

The input voltage, applied between  $V_{\text{IN}}$  and GND, should be at least 1.0V greater than  $V_{\text{OUT}}$ , and no higher than the applied  $V_{\text{BIAS}}$  voltage.

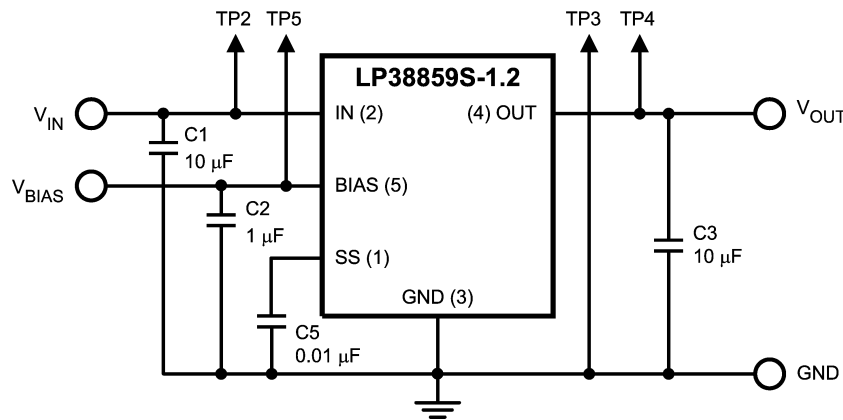
The bias voltage, applied between  $V_{\text{BIAS}}$  and GND should be above the minimum bias voltage of 3.0V, and no higher than the maximum of 5.5V.

Loads can be connected to  $V_{\text{OUT}}$  with reference to GND.

$V_{\text{OUT}}$  and  $V_{\text{IN}}$  test points are provided on the board to allow accurate measurements directly on the evaluation board, eliminating any voltage drop on the PCB traces or connecting wires to the load.

The Soft-Start time for  $V_{\text{OUT}}$  is an exponential function, and is adjusted by changing the Soft-Start capacitor ( $C_{\text{SS}}$ ) on device pin one. An internal resistor ( $r_{\text{SS}}$ ) and the external capacitor ( $C_{\text{SS}}$ ) form an RC circuit. Five RC time constants is considered to be the Soft-Start time.

## Schematic Diagram

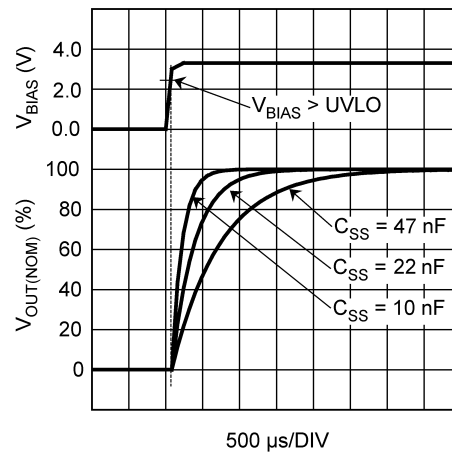


Evaluation Board Schematic

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$$\text{Soft-Start Time} = 5 \times r_{\text{SS}} \times C_{\text{SS}}$$

The installed soft-start capacitor ( $C_{\text{SS}}$ ) is 10 nF (0.01  $\mu\text{F}$ ), and the internal  $r_{\text{SS}}$  is typically 16 k $\Omega$ .



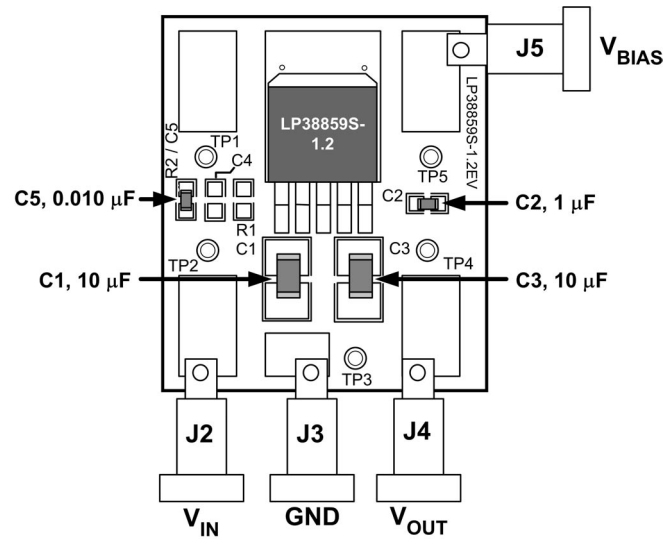
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FIGURE 1.  $V_{\text{OUT}}$  vs  $C_{\text{SS}}$

## Hardware

The schematic and layout of the evaluation board are given below:

## PCB Layout



Evaluation Board Component and Pin Layout

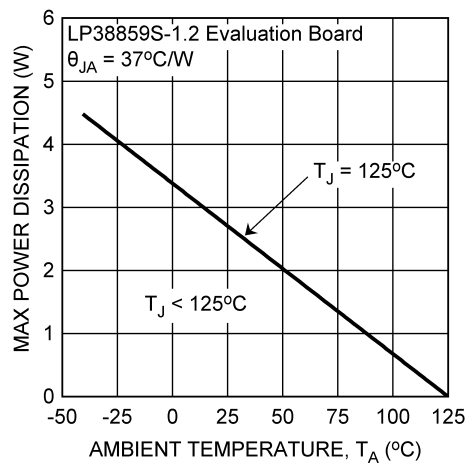
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## Power Dissipation

The TO-263 package alone has a junction to ambient thermal resistance ( $\theta_{JA}$ ) rating of  $60^{\circ}\text{C/W}$ . When mounted on the LP38859S evaluation board the  $\theta_{JA}$  rating is approximately  $37^{\circ}\text{C/W}$ .

Although there is only approximately 0.28 square inches of copper area immediately under the tab, the top copper surface area is extended to additional copper area on the bottom of the board by five thermal vias.

With the  $37^{\circ}\text{C/W}$  thermal rating the LP38859S evaluation board will dissipate a maximum of 2.75W with  $T_A = 25^{\circ}\text{C}$ .



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FIGURE 2. Maximum Power Dissipation vs Ambient Temperature

## Bill of Materials

ID	Name	Description	Manufacturer	Part Number
U1	U1	LP38859S-1.2 NOPB	National Semiconductor Corporation	LP38859S-1.2 NOPB
C1	C <sub>IN</sub>	10 $\mu$ F, 10%, MLCC, 10V, X7R, 1210	AVX	1210ZC106KAT2A
C2	C <sub>BIAS</sub>	1 $\mu$ F, 10%, MLCC, 10V, X7R, 0805	AXV	0805ZC105KAT2A
C3	C <sub>OUT</sub>	10 $\mu$ F, 10%, MLCC, 10V, X7R, 1210	AVX	1210ZC106KAT2A
C4	—	Not Installed	—	—
C5	C <sub>SS</sub>	0.010 $\mu$ F, 10%, MLCC, 16V, X7R, 0805	AVX	0805YC103KAT2A
J1	—	Not Installed	Johnson Components	—
J2	V <sub>IN</sub>	Banana Jack : Insulated Solder Terminal - RED		108-0902-001
J3	GND	Banana Jack : Insulated Solder Terminal - BLACK		108-0903-001
J4	V <sub>OUT</sub>	Banana Jack : Insulated Solder Terminal - ORANGE		108-0906-001
J5	V <sub>BIAS</sub>	Banana Jack : Insulated Solder Terminal - BLUE		108-0910-001
R1	—	Not Installed	—	—
R2	—	Not Installed	—	—
TP1	—	Not Installed	—	—
TP2	TP <sub>IN</sub>	Turret Terminal : Mounting Hole Diameter = 0.062"	Keystone	1593-2
TP3	TP <sub>GND</sub>			
TP4	TP <sub>OUT</sub>			
TP5	TP <sub>BIAS</sub>			

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