AND8172/D

Understanding the Noise Issue Out of Inductor Based DC-DC Converter

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APPLICATION NOTE

Abstract

Portable applications, such as cellular phones and hand−held computers, have sensitive electronic functions, making any electromagnetic noise a real issue. Even a low power converter can generate noise during transients since the converters operate in the megahertz range. The high frequency switching can interact with the parasitic circuit elements to create uncontrolled noise. In addition, the associated voltage spikes might be difficult to filter out, a detailed analysis of the converter operation being necessary to properly design the system. Of course, the mechanical layout is a key parameter to minimize the EMI perturbation. The main purpose of this document is to clarify the source of such a noise, and assess the risk of system's EMI pollution. The NCP5007 device, together with a PWM based structure, will be used as vehicles to perform the associated engineering test in a real application, but the same may apply to other Boost converters, such as the NCP5005.

NCP5007/NCP5005 Basic Analysis

The NCP5007/NCP5005 are dc−dc converters dedicated to the supply of High Efficiency White LEDs used as an LCD back light or photo flash light source. Generally speaking, with a typical 3.8 V Vf drop during normal operation, these LEDs are not capable to operate from a standard 3.6 V battery pack. A boost circuit must be provided to raise the voltage up to the bias called by such a diode. Moreover, these LEDs are commonly connected in series to get a constant current through the diodes, assuring smooth and consistent light across the LCD panel.

The basic application, depicted in Figure 1, drives the back light of a standard LCD display, the command bit EN being provided by an external CPU or other digital controller.

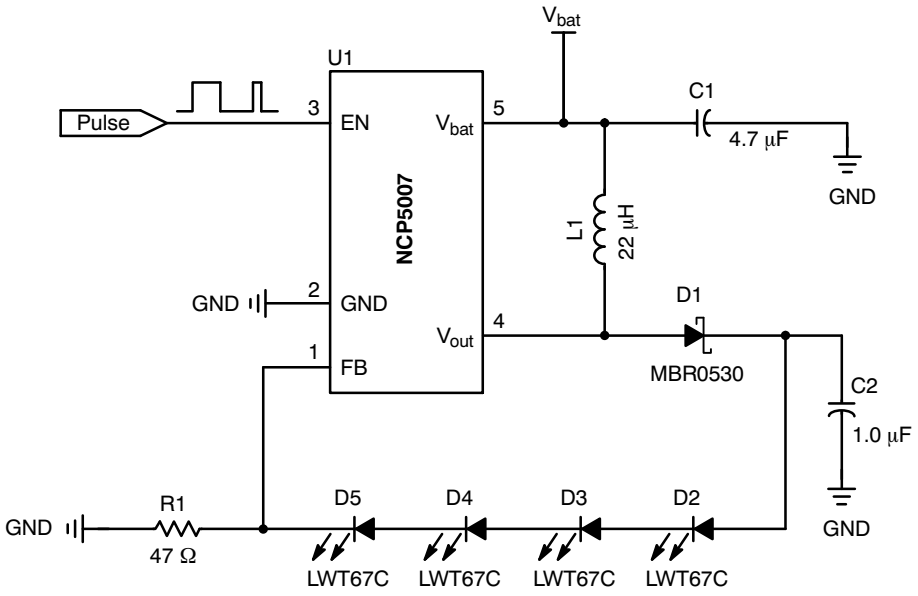


Figure 1. Typical Back Light Application

With a 10 Ω sense resistor, the dc current through the LEDs is 20 mA with a ±10% tolerance over the temperature range. The output voltage will be 19 V (typical) and the 1.0 μF capacitor must be sized accordingly. Using ceramic type X5R is mandatory for both C1 and C2.

The EN signal (Enable, pin 3) is useful to power ON/OFF the diodes, the chip providing a constant current to the LEDs when EN = V_{bat}. On the other hand, the EN signal can also be used to control the brightness of the back light by means of a PWM signal applied to pin 3.

Basically, the chip operates with two cycles in a PFM mode:

Cycle #1: the energy is stored into the inductor
Cycle #2: the energy is dumped to the load

Of course, from a practical standpoint, the inductor must be sized to cope with the peak current present in the circuit to avoid saturation of the core. On top of that, the ferrite material shall be capable to operate at high frequency (>1.0 MHz) to minimize the Foucault's losses developed during the cycles.

The waveforms captured on the NCP5007 Demo Board, V3.10, show two voltage spikes VSPK#1 and VSPK#2 across the output voltage (Figure 2). The VSPK#1 signal is synchronized with the positive going slope of the output voltage, the VSPK#2 signal being synchronized with the negative slope of the same voltage. Both of these signals come on top of the voltage ripple. Generally speaking, such spikes will be named "noise'', but we do not know what is the energy content and what could be the influence of the electrical environment. At this point, let us consider the switching operation only since there are no spikes outside the transients as demonstrated by the waveforms.

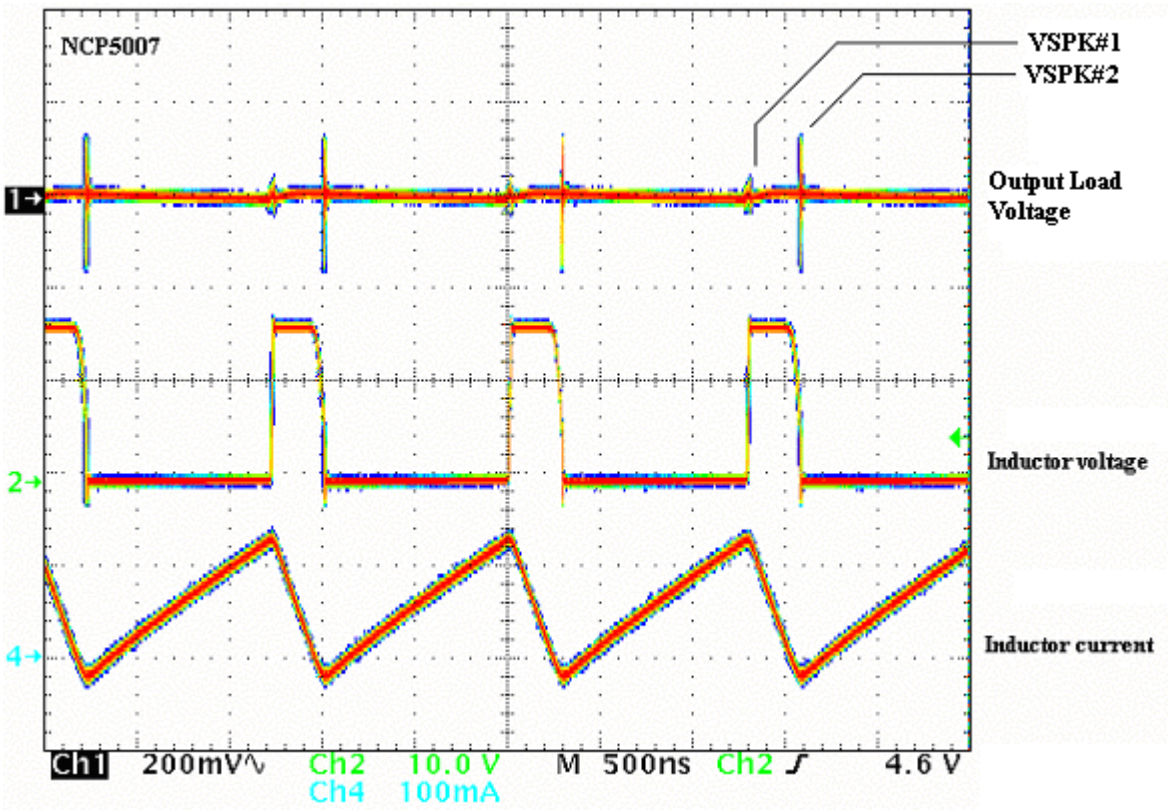


Figure 2. NCP5007 Normal Operation

The silicon chip is connected to the external world by means of bonding wires attached to the internal pads. The bonding wires have finite inductance and stray capacitance. In addition, the internal overvoltage protection circuits and PCB trace leads contribute to such parasitic elements.

The simplified PSPICE model (Figure 3), includes the parasitic inductances associated with the NCP5007 internal bonding, and the stray capacitance between the output pin and ground. The load is built with the White LED LWT67C model (courtesy: OSRAM GmbH) with a 1.0 μF reservoir capacitor in parallel. The inductor includes the ESR and stray capacitance developed by the wiring. The ESR of the printed circuit tracks and wiring is neglected as it is not a first order importance, unless the layout is really poor.

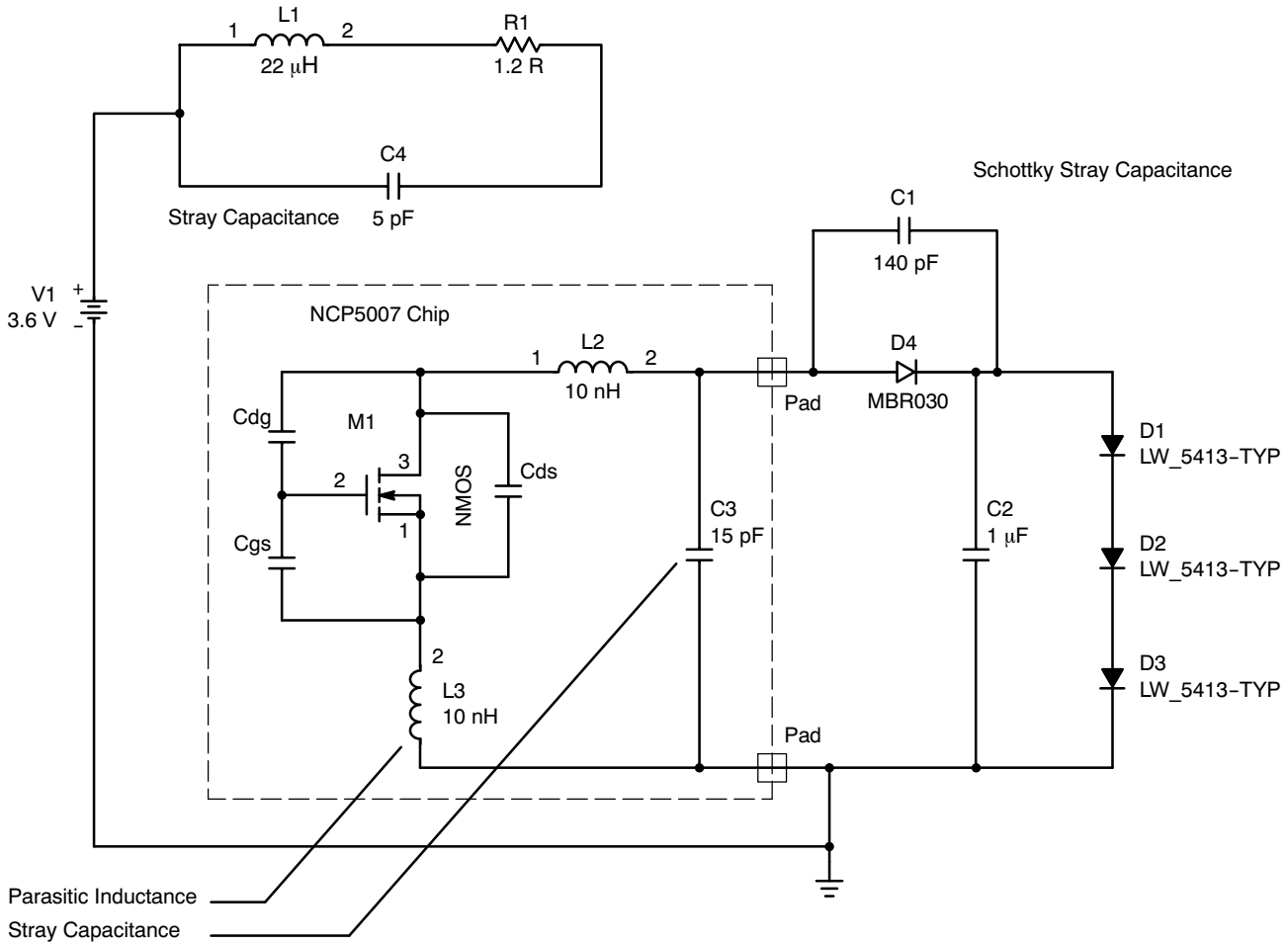


Figure 3. PSPICE Output Circuit Model

SPIKE VSPK#1

Assuming the system operates in steady state, let us consider the noise VSPK#1. The current flowing into the NMOS is abruptly switched off and the voltage rises (according to the Lenz's law) until the Schottky diode is forward biased. The inductor current will be diverted to the load when the output voltage will be higher than V_{out} + Vf. During the positive going of the output voltage slope, the stray capacitances and the parasitic inductances create an LC network, yielding an oscillation as the NMOS device is switched off. According to the MBR0530 data sheet, the intrinsic stray capacitance varies from 170 pF (when Vr = 0 V) to 40 pF when Vr = 12 V.

Let us consider Vr = 10 V since $V_{out} = \Sigma$ Vf*LED, then:

$$F = \frac{1}{2 * \Pi * \sqrt{LC}}$$

$$F = \frac{1}{2 * \Pi * \sqrt{20 * 10^{-9} * 40 * 10^{-12}}} = 178 \text{ MHz} \quad \text{(eq. 1)}$$

The period T is derived from:

$$T = \frac{1}{F} = \frac{1}{178 * 10^{6}} = 5.6 \text{ ns.} \quad \text{(eq. 2)}$$

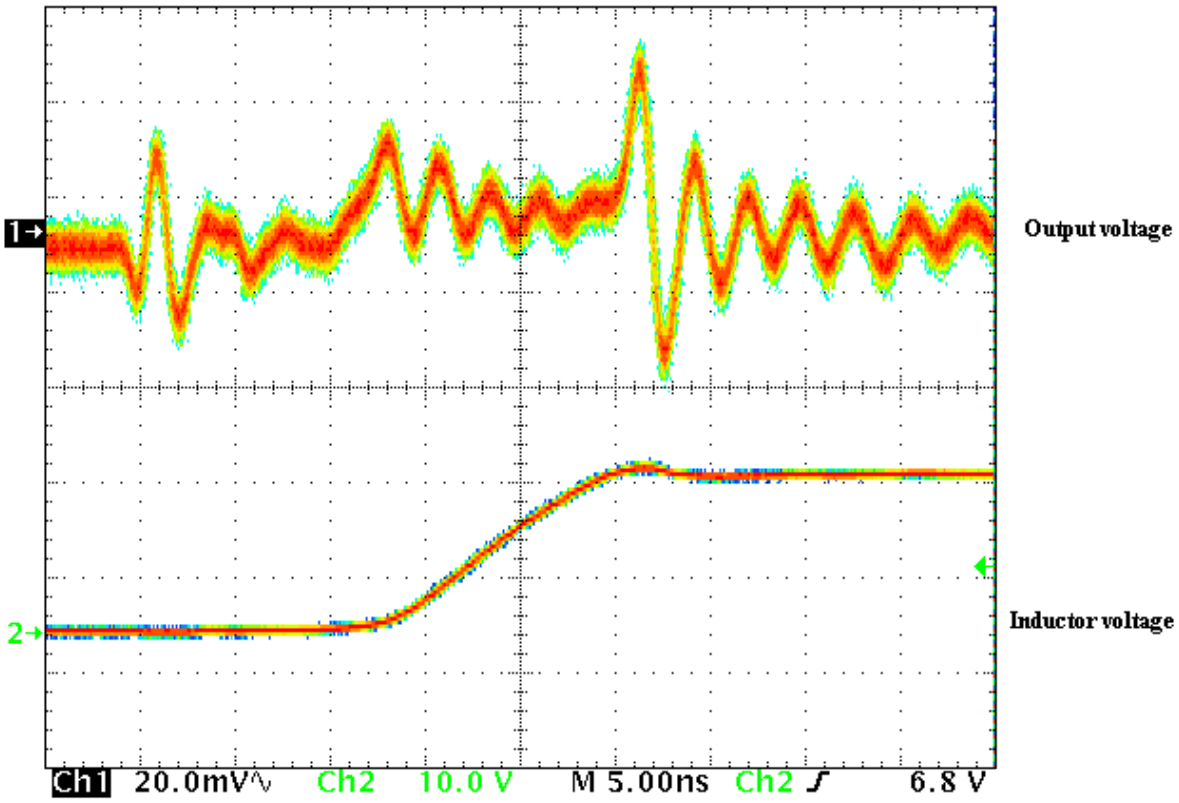
This value is well within the signal given Figure 4, captured during the test performed with the NCP5007 demo board. Of course, the frequency varies along the output voltage slope since all the semiconductor based capacitance varies as the voltage varies across the junctions.

Beside the voltage effect, one must consider the level of energy radiated by such a spike. In this application, the energy is transferred from the parasitic inductance to the stray capacitance, as depicted by the waveforms (oscillations). Consequently, we can calculate the amount of energy stored into the parasitic inductor:

$$Ej = \frac{1}{2} * L * I^2$$

$$Ej = \frac{1}{2} * 20 * 10^{-9} * 0.06^2 = 36 \text{ pJ} \quad \text{(eq. 3)}$$

Such level of energy is extremely low and will not pollute the environment.



Note: The dI/dt of the NCP5007 internal NMOS is 10 mA/ns, a very fast transient.

Figure 4. NCP5007 Output Voltage Noise at NMOS Turn Off

SPIKE VSPK#2

The spike is developed during the negative going slope of the output voltage, when the current transfer to the load is completed and the NMOS switch turns on (Figure 5).

At this point, the voltage across the Schottky diode reverses and the same parasitic structures are activated, yielding the oscillation depicted by the top trace (Figure 5).

The energy is now transferred from the charged stray capacitance to the parasitic inductor, yielding the oscillations. Assuming the total stray capacitance is 80 pF (NCP5007 pad, PCB, Schottky), we get:

$$Ej = \frac{1}{2} * C * V^2$$

(V = sum of the white LED Vf)

(C = total stray capacitance, first order only)

$$Ej = \frac{1}{2} * 80 * 10^{-12} * 12^2 = 5.7\ nJ \qquad \text{(eq. 4)}$$

This energy is partially dissipated into the ohmic resistance, partially into the $R_{DS(on)}$ of the internal NMOS device (1.7 Ω typical for the NCP5007), yielding a 1000 mVpp spike as depicted in Figure 5.

Although visible, a 5.7 nJ amount of energy is likely too low to pollute the environment of the power device. Moreover, the energy is not radiated by an external inductance element, but is limited to the parasitic structures only, thus less prone to trouble the rest of the application.

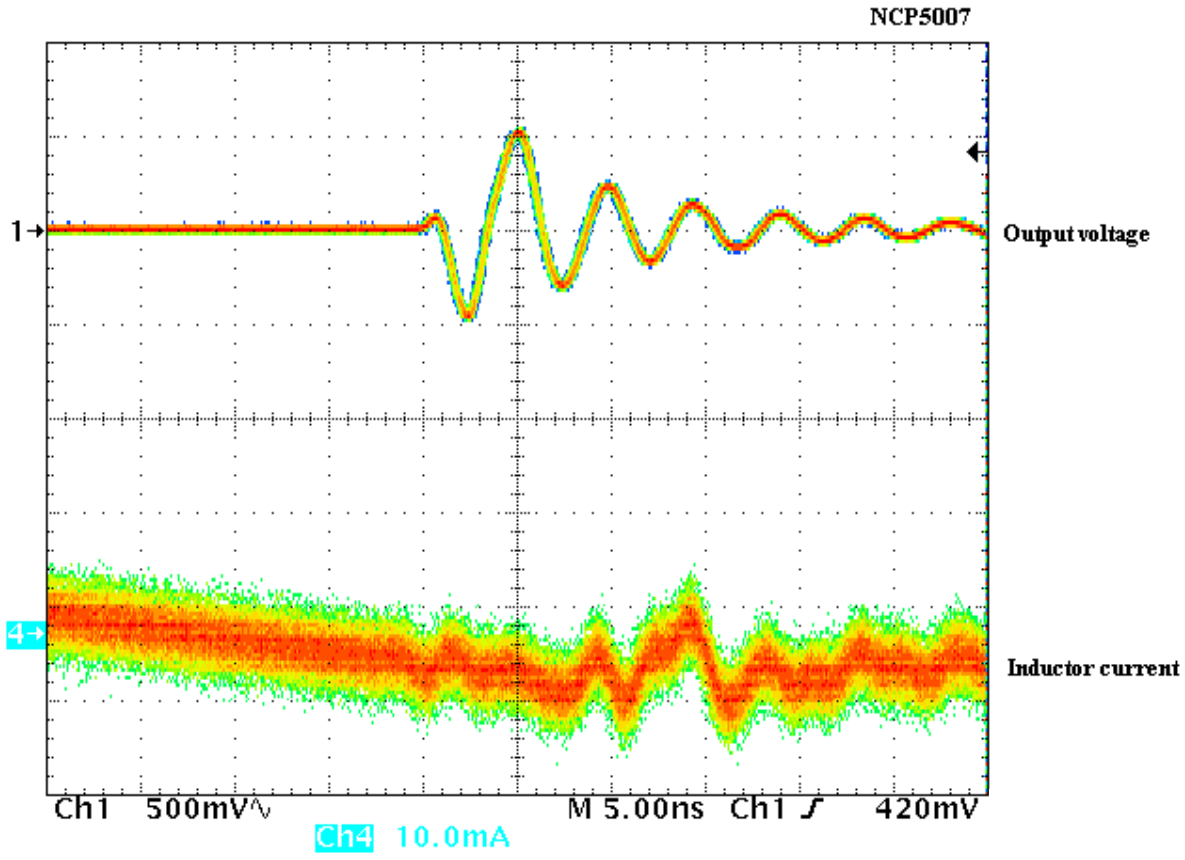


Figure 5. NCP5007 Output Voltage Noise at NMOS Turn On

Discontinuous Mode of Operation Analysis

When a chip operates in a fully discontinuous mode, a large peak current takes place in the inductor as depicted in Figure 6. The PWM mode is prone to such a discontinuous cycle. The output voltage is largely different, in comparison with the NCP5007, as one expects from a discontinuous mode of operation. The main consequence is the large oscillations developed when the transfer of the current between the inductor and the load is completed. Of course, internal circuit can be implemented to avoid such oscillation (so−called ring killer), but all ICs might not have such features. The oscillations are no longer the only consequence of the Schottky diode, but come from the main inductor (22 μH) associated with the stray capacitances. Assuming we have a 30 pF stray capacitance (the Schottky diode as a minimum parasitic capacitance since the reverse voltage is maximum), the frequency is 6.2 MHz, yielding a 161 ns period. The calculated values are well within the evaluation tests carried out with a PWM based white LED driver used as a reference (Figure 6, top trace).

At this point, one can derive the level of energy radiated during this period:

$$Ej = \frac{1}{2} * L * I^2 \quad (I = \text{level of the current during the oscillation first order only})$$

$$Ej = \frac{1}{2} * 22 * 10^{-6} * 0.04^2 = 4.4\ nJ \qquad \text{(eq. 5)}$$

Although such a level is low, is it generated by the main inductor and this element is prone to radiate most of this energy out of the core, unless a shielding magnetic core is used.

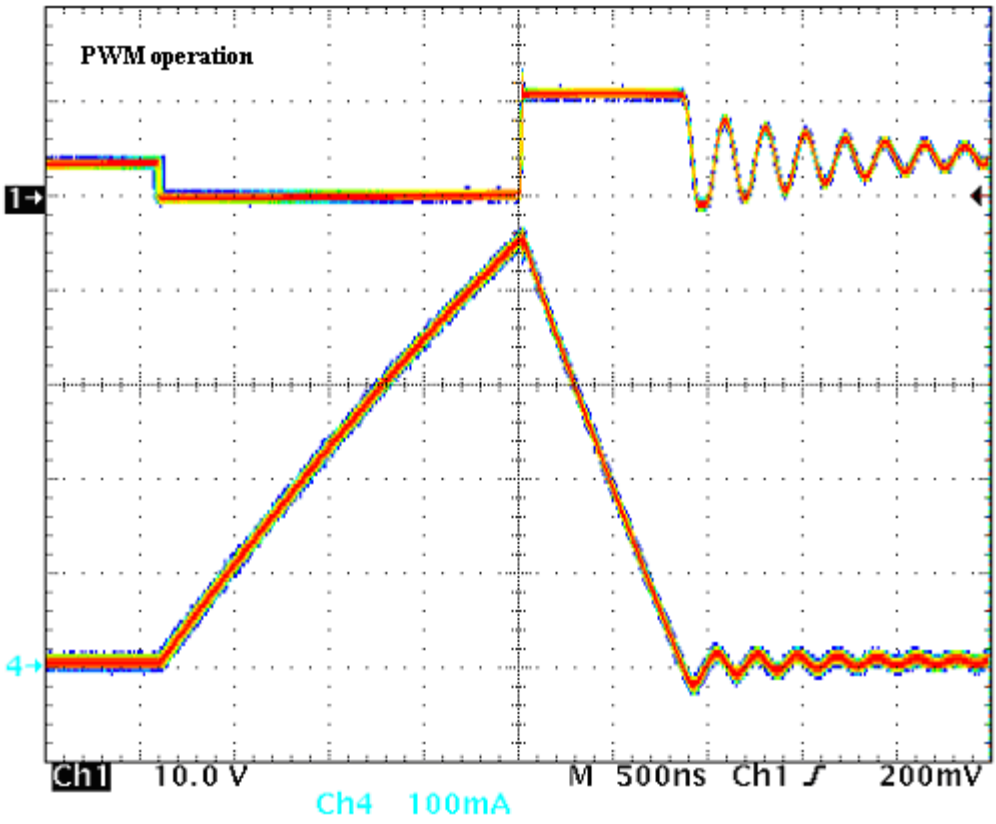


Figure 6. Typical PWM Normal Operation

A detailed view of the PWM based chip output voltage shows a non−negligible spike when the inductor current hits the maximum peak value (Figure 7).

Basically, this is the same mechanism as the one depicted for the NCP5007 application, and a similar voltage spike is developed with 800 mVpp amplitude.

Leaving aside the structure, the main difference between the PWM mode and the NCP5007 from a power device standpoint, is the $R_{DS(on)}$ of the internal NMOS. We have 1.7 Ω, compared to 0.5 Ω for the PWM chip. The consequence is twofold:

1. With a lower $R_{DS(on)}$, the PWM based chip has probably larger Cdg, Cgs and Cds capacitances, thus slower dI/dt. Consequently, slower dI/dt minimizes the effect of the parasitic inductance.
2. Similarly, lower $R_{DS(on)}$ generates lower voltage spike for the same amount of energy transferred from the stray capacitance.

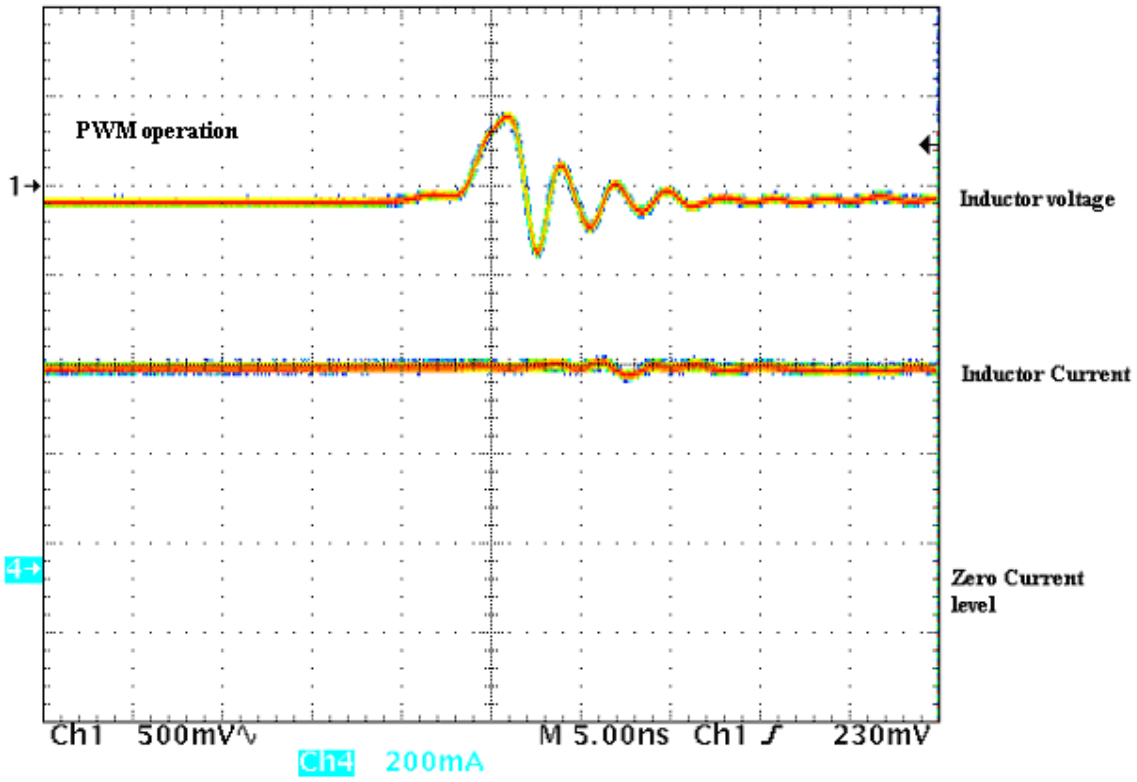


Figure 7. PWM Chip Output Voltage Noise as the NMOS is Switched Off

SPECTRUM ANALYSIS

The waveforms captured by an oscilloscope are very useful to evaluate the behavior of a given product, but they don't give information about the EMI performance. At this point, a spectrum analyzer is necessary to characterize the device over the considered bandwidth.

The spectrum analysis has been performed with the same demo board, the antenna being located 10 mm above the inductor. Although the tests have not been performed in a shielded cage, the results provide a good understanding of the situation in terms of EMI. The waveforms are provided in Figures 8 and 9.

It is clear that, although the apparent voltage spikes are higher for the NCP5007, the net result, in terms of real noise, is much better for the NCP5007 in comparison with the PWM circuit as depicted by the records.

In order to better analyze the spikes coming from the chips, the noise return to battery has been measured and recorded (Figure 10). The spectral density, mathematical integration of the two curves, yields 0.826 mVrms for the NCP5007, and 238 mVrms for the PWM based chip, both over the 100 kHz to 30 MHz bandwidth.

Once again, the behavior of the NCP5007 is far better than the PWM based white LED driver, particularly in the 100 kHz to 1.0 MHz frequency band.

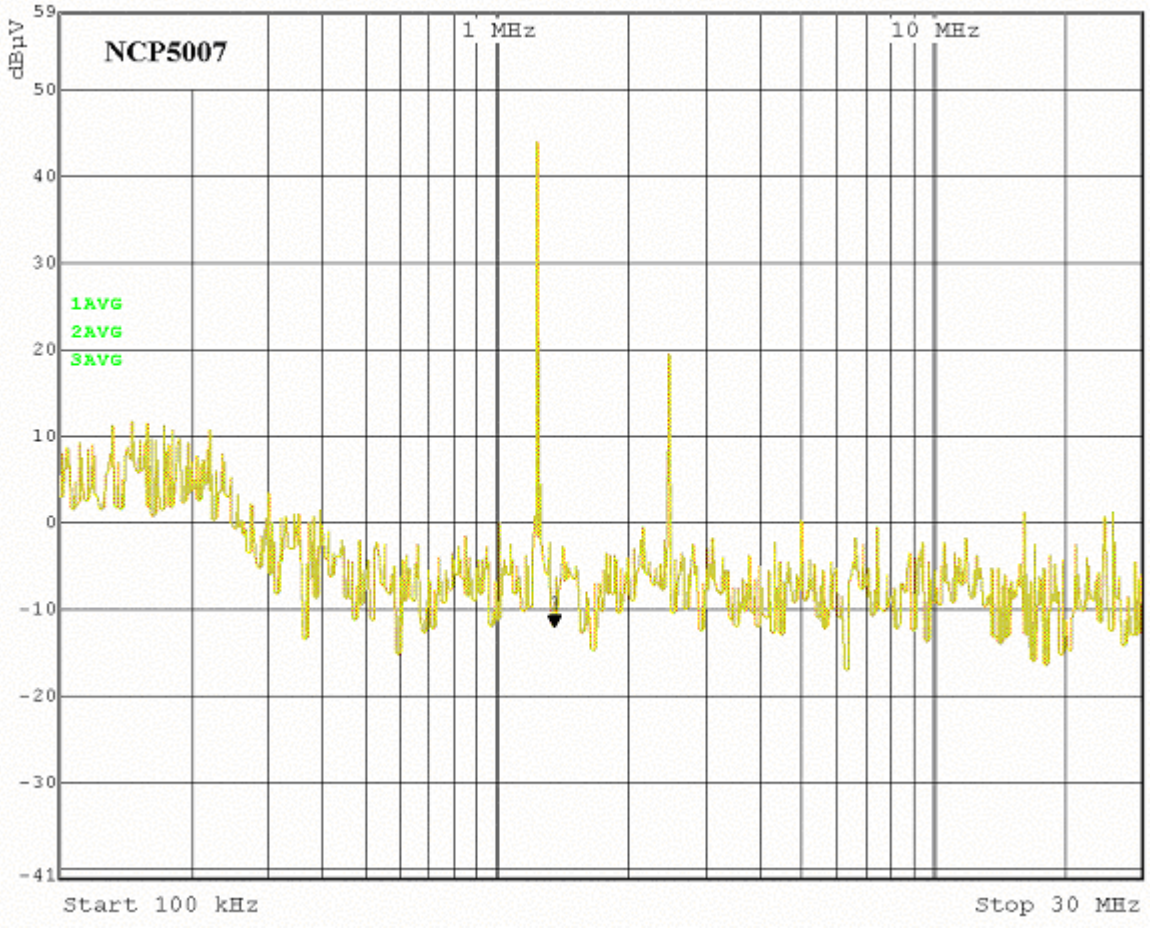


Figure 8. NCP5007 Spectrum Analysis (Unit: dB µV): Relative EMI

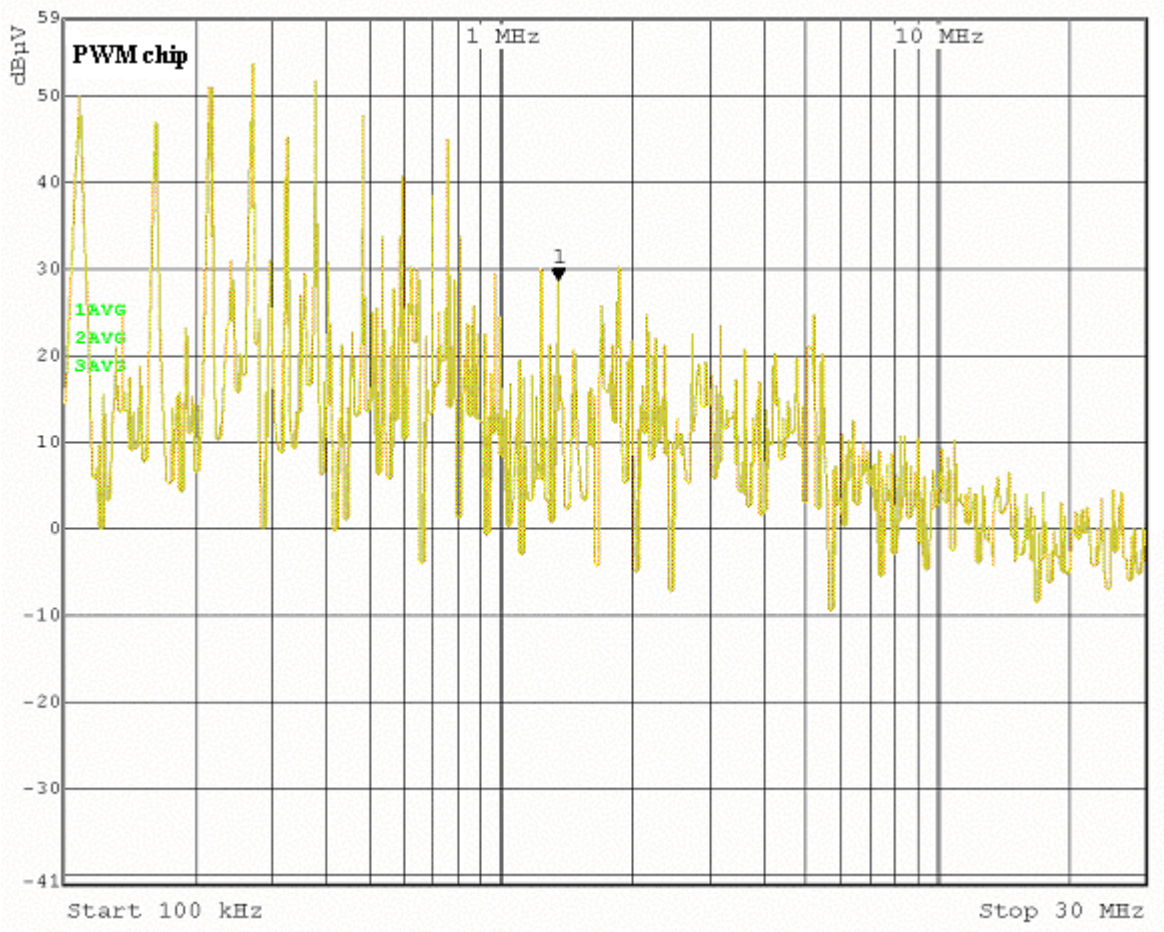


Figure 9. PWM Circuit Spectrum Analysis

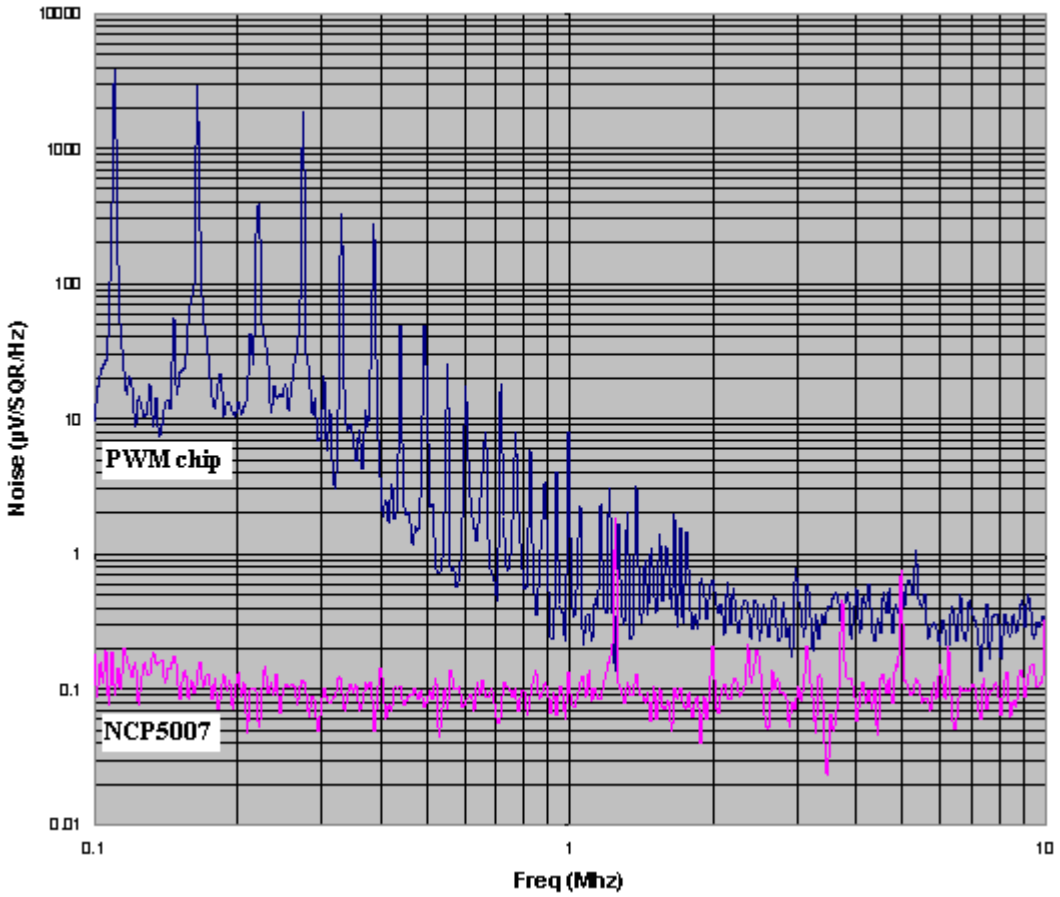


Figure 10. Reflected Noise to Battery

CONCLUSION

Since it is not possible to reduce the parasitic inductance to zero (using the micro bump technique could improve but not reduce the inductance to zero nH), and since fast dI/dt is necessary to lower the switching losses into the chip, spikes voltage might exist.

However, it is mandatory to consider the behavior of the power device in the real environment, keeping into account all the parasitic effects. The spectrum analysis, provided in Figures 8 and 9, demonstrates the excellent EMI behavior of the NCP5007 with much lower noise, in comparison with the PWM based white LED driver operation. The same comment applies for the reflected noise to battery.

The waveforms are very useful to fully characterize the system, but it is of prime importance to identify and quantify the risks, in terms of noise and reliability, of the voltage spikes when a detailed analysis is requested.

PSPICE SIMULATIONS

The circuit has been simulated prior to run the analysis in the laboratory. The same schematic (Figure 11) has been used to evaluate the configurations.

Using a lower $R_{DS(on)}$ yields the expected lower spike and a low stray capacitance diode provides a much lower noise during the transients, as expected.

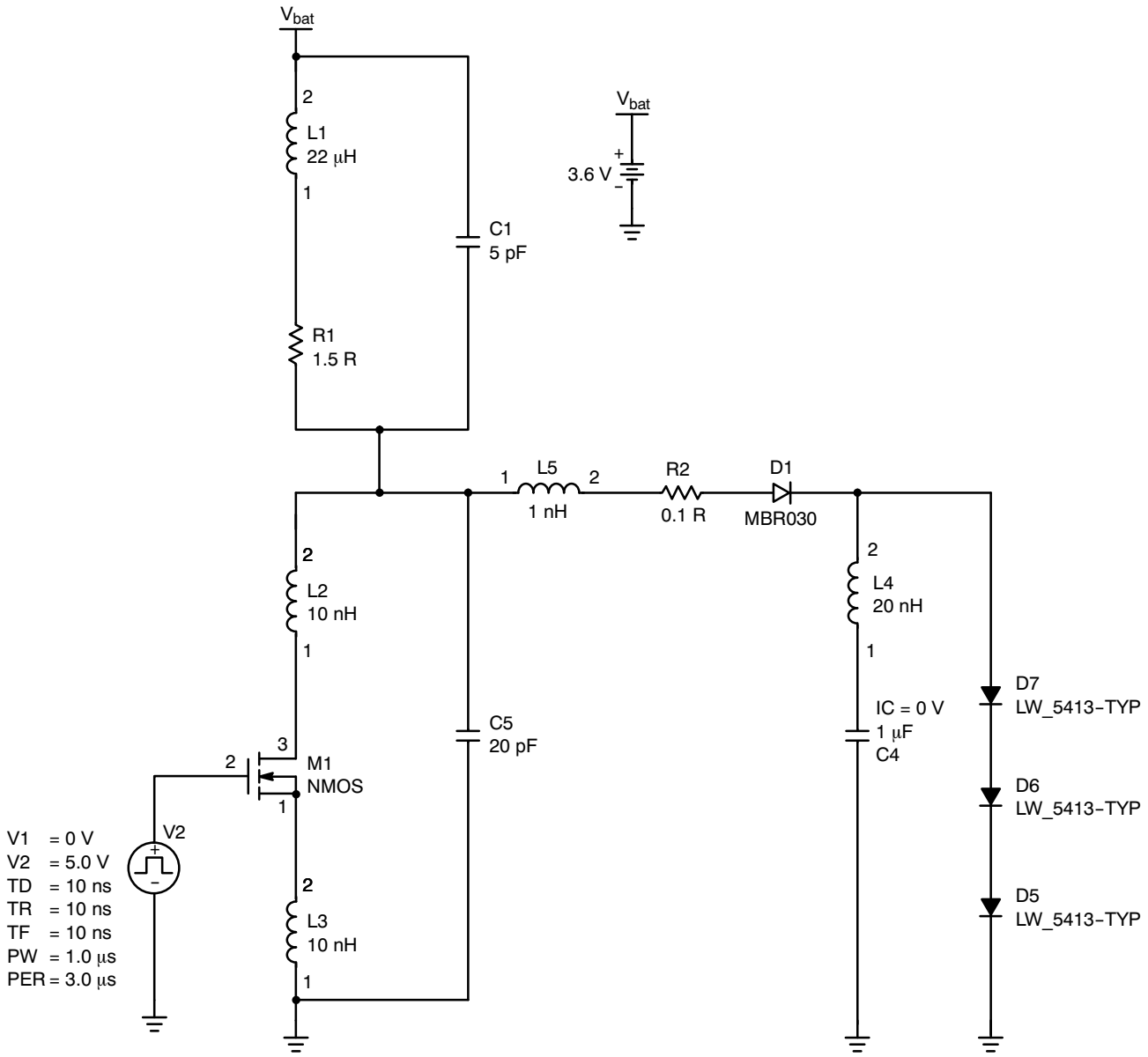


Figure 11. PSPICE Schematic Diagram

The parasitic elements are based on the existing package and silicon designs. The value of the stray capacitance (C5) depends, besides the internal structure, upon the PCB layout.

Test Conditions

1. Temperature :Room, +20°C
2. Oscilloscope :Tektronix, TDA754/D, operating in the DPO mode
3. Voltage Probes :Tektronix P6139A
4. Current Probe :Tektronix TCP202
5. Input Power Supply :Tektronix PS2520G
6. Input Power Supply Bias :3.60 V
7. Output Load :3 White LED
8. Output DC Current :NCP5007 = 10 mA, PWM based chip = 18 mA (R_{sense} = 22 Ω)
9. Inductor :22 μH
10. Spectrum Analyzer :ROHDE & SCHWARZ, FSIQ 7
11. Spectrum Analyzer :HP4195A
12. EMI probe :HP11941A
13. HF probe :HP41800A

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