LM3409HV Evaluation Board

National Semiconductor
Application Note 1953
James Patterson
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Introduction

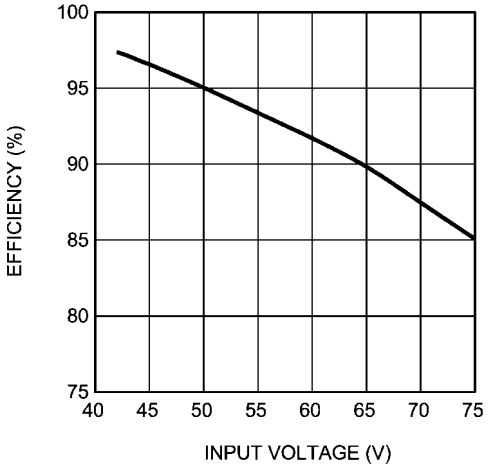
This evaluation board showcases the LM3409HV PFET controller for a buck current regulator. It is designed to drive 12 LEDs (V_O = 42V) at a maximum average LED current (I_{LED} = 1.5A) from a DC input voltage (V_{IN} = 48V). The switching frequency (f_{SW} = 400 kHz) is targeted for the nominal operating point, however f_{SW} varies across the entire operating range. The circuit can accept an input voltage of 6V-75V. However, if the input voltage drops below the regulated LED string voltage, the converter goes into dropout and $V_O = V_{IN}$ ideally.

The PCB is made using 4 layers of 2 oz. copper with FR4 dieletric. The evaluation board showcases all features of the LM3409HV including analog dimming using the IADJ pin and internal PWM dimming using the EN pin. High frequency external parallel FET shunt PWM dimming can also be evaluated. The board has a header (J1) with a removable jumper, which is used to select the PWM dimming method.

The evaluation board has a right angle connector (J2) which can mate with an external LED load board allowing for the LEDs to be mounted close to the driver. This reduces potential ringing when there is no output capacitor. Alternatively, the LED+ and LED- turrets can be used to connect the LED load.

This board can be easily modified to demonstrate other operating points as shown in the *Alternate Designs* section. The LM3409/09HV datasheet *Design Procedure* can be used to design for any set of specifications.

EFFICIENCY WITH 12 SERIES LEDS AT 1.5A



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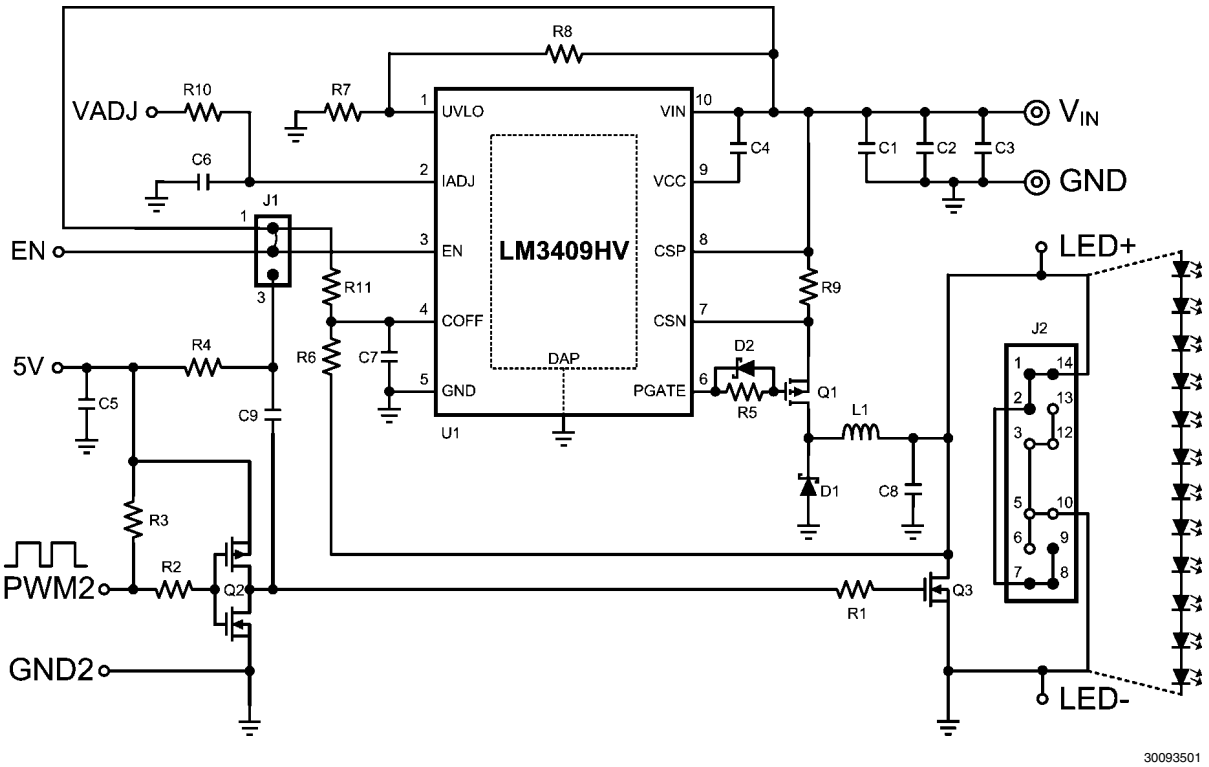
Since the board contains a buck regulator designed for 48V input, the efficiency is very high at input voltages near or less than 48V. The switching frequency increases as input voltage increases, yielding lower efficiency at higher input voltages. Note that increasing the off-time resistor (R6) will increase the efficiency at high input voltage.

Schematic



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Pin Descriptions

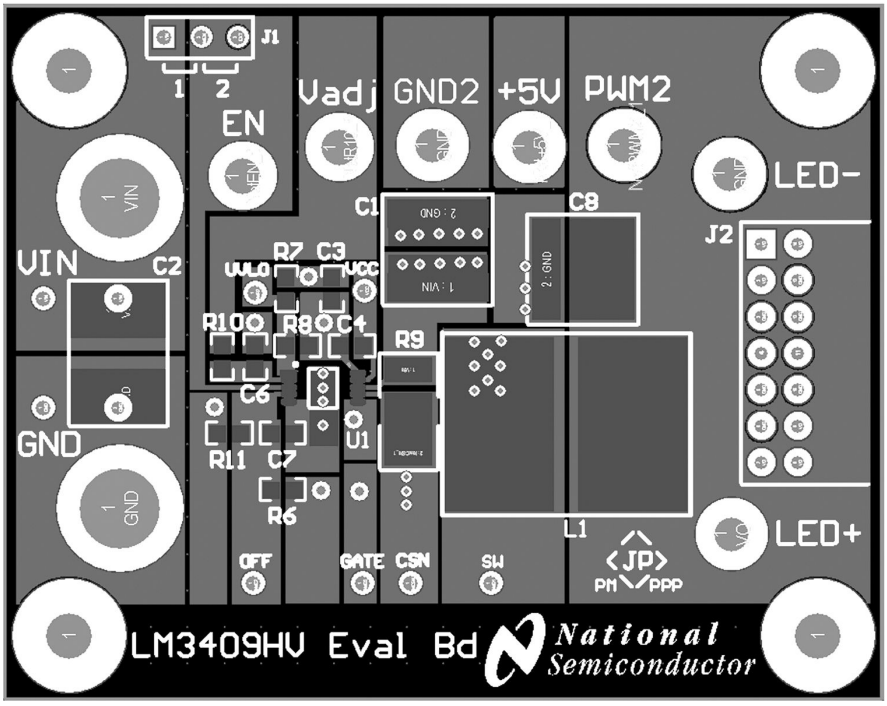
Pin(s)	Name	Description	Application Information
1	UVLO	Input under-voltage lockout	Connect to a resistor divider from V_{IN} and GND. Turn-on threshold is 1.24V and hysteresis for turn-off is provided by a 22µA current source.
2	IADJ	Analog LED current adjust	Apply a voltage between 0 - 1.24V, connect a resistor to GND, or leave open to set the current sense threshold voltage.
3	EN	Logic level enable / PWM dimming	Apply a voltage >1.74V to enable device, a PWM signal to dim, or a voltage <0.5V for low power shutdown.
4	COFF	Off-time programming	Connect resistor to V_O, and capacitor to GND to set the off-time.
5	GND	Ground	Connect to the system ground.
6	PGATE	Gate drive	Connect to the gate of the external PFET.
7	CSN	Negative current sense	Connect to the negative side of the sense resistor.
8	CSP	Positive current sense	Connect to the positive side of the sense resistor (V_{IN}).
9	VCC	V_{IN}- referenced linear regulator output	Connect at least a 1µF ceramic capacitor to V_{IN}. The regulator provides power for the PFET drive.
10	VIN	Input voltage	Connect to the input voltage.
DAP	DAP	Thermal pad on bottom of IC	Connect to pin 5 (GND). Place 4-6 vias from DAP to bottom GND plane.

Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	U1	Buck controller	NSC	LM3409HVMY
2	C1, C2	2.2µF X7R 10% 100V	MURATA	GRM43ER72A225KA01L
1	C3	0.1µF X7R 10% 100V	MURATA	GRM188R72A104KA35D
1	C4	1.0µF X7R 10% 16V	TDK	C1608X7R1C105K
1	C5	0.1µF X7R 10% 50V	MURATA	GRM319R71H104KA01D
1	C6	0.1µF X7R 10% 50V	MURATA	GCM188R71H104KA57D
1	C7	470pF X7R 10% 50V	TDK	C1608X7R1H471K
3	C8, D2, R11	No Load		
1	C9	2200pF X7R 10% 50V	MURATA	GRM188R71H222KA01D
1	Q1	PMOS 100V 3.8A	ZETEX	ZXMP10A18KTC
1	Q2	CMOS 30V 2A	FAIRCHILD	FDC6333C
1	Q3	NMOS 100V 7.5A	FAIRCHILD	FDS3672
1	D1	Schottky 100V 3A	VISHAY	SS3H10-E3/57T
1	L1	33 µH 20% 3.2A	TDK	SLF12575T-330M3R2
2	R1, R2	1Ω 1%	VISHAY	CRCW06031R00FNEA
1	R3	10kΩ 1%	VISHAY	CRCW060310K0FKEA
1	R4	100Ω 1%	VISHAY	CRCW0603100RFKEA
1	R5	0Ω 1%	VISHAY	CRCW06030000Z0EA
1	R6	16.5kΩ 1%	VISHAY	CRCW060316K5FKEA
1	R7	6.98kΩ 1%	VISHAY	CRCW06036K98FKEA
1	R8	49.9kΩ 1%	VISHAY	CRCW060349K9FKEA
1	R9	0.15Ω 1% 1W	VISHAY	WSL2512R1500FEA
1	R10	1kΩ 1%	VISHAY	CRCW06031K00FKEA
1	J1	3 pin header	MOLEX	22-28-4033
1	J2	2x7 pin RA shrouded	SAMTEC	TSSH-107-01-S-D-RA
2	VIN, GND	banana jack	KEYSTONE	575-8
7	EN, Vadj, +5V, GND2, PWM2, LED+, LED-	turret	KEYSTONE	1502-2

PCB Layout

The 2 inner planes are GND and V_{IN}.



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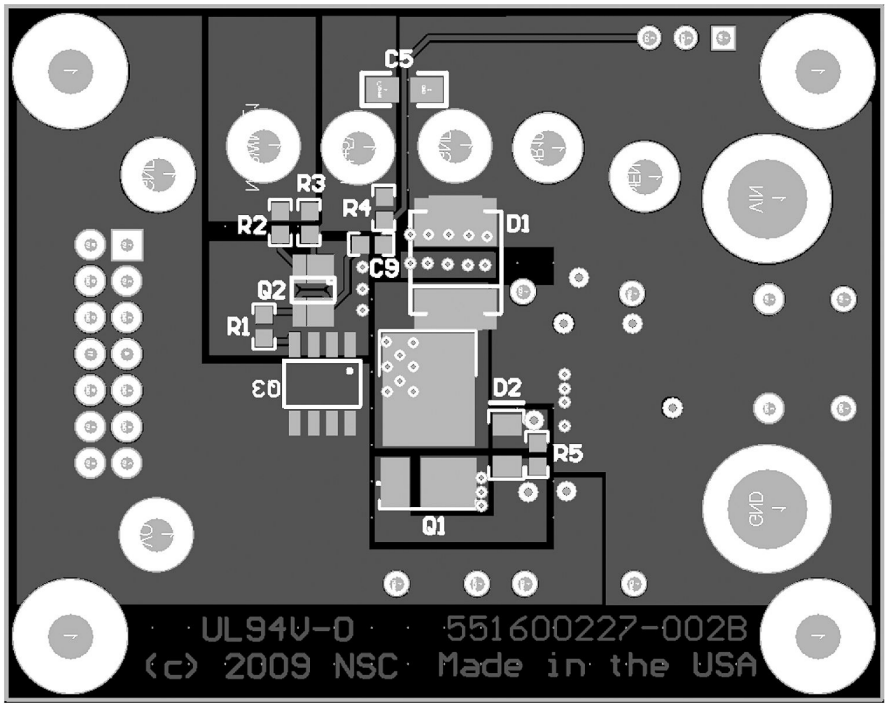
Top Layer



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Bottom Layer

Design Procedure

SPECIFICATIONS

V_{IN} = 48V; V_{IN-MAX} = 75V
V_O = 42V
f_{SW} = 400kHz
I_{LED} = 1.5A
$\Delta i_{LED-PP} = \Delta i_{L-PP}$ = 300mA
Δv_{IN-PP} = 1.44V
$V_{TURN-ON}$ = 10V; V_{HYS} = 1.1V
η = 0.97

1. NOMINAL SWITCHING FREQUENCY

Assume C7 = 470pF and η = 0.97. Solve for R6:

$$R6 = \frac{-\left(1-\frac{V_O}{\eta \times V_{IN}}\right)}{(C7 + 20\ pF)\ \times f_{SW} \times \ln\left(1-\frac{1.24V}{V_O}\right)}$$

$$R6 = \frac{-\left(1-\frac{42V}{0.97 \times 48V}\right)}{490\ pF \times 400\ kHz \times \ln\left(1-\frac{1.24V}{42V}\right)} = 16.7\ k\Omega$$

The closest 1% tolerance resistor is 16.5 kΩ therefore the actual t_{OFF} and target f_{SW} are:

$$t_{OFF} = -(C7+20pF) \times R6 \times \ln\left(1-\frac{1.24V}{V_O}\right)$$

$$t_{OFF} = -490\ pF \times 16.5\ k\Omega \times \ln\left(1-\frac{1.24V}{42V}\right) = 242\ ns$$

$$f_{SW} = \frac{1-\left(\frac{V_O}{\eta \times V_{IN}}\right)}{t_{OFF}} = \frac{1-\left(\frac{42V}{0.97 \times 48V}\right)}{242\ ns} = 404\ kHz$$

The chosen components from step 1 are:

C7 = 470 pF
R6 = 16.5 kΩ

2. INDUCTOR RIPPLE CURRENT

Solve for L1:

$$L1 = \frac{V_O \times t_{OFF}}{\Delta i_{L-PP}} = \frac{42V \times 242\ ns}{300\ mA} = 33.9\ \mu H$$

The closest standard inductor value is 33 µH therefore the actual Δi_{L-PP} is:

$$\Delta i_{L-PP} = \frac{V_O \times t_{OFF}}{L1} = \frac{42V \times 242\ ns}{33\ \mu H} = 308\ mA$$

The chosen component from step 2 is:

L1 = 33 µH

3. AVERAGE LED CURRENT

Determine I_{L-MAX}:

$$I_{L-MAX} = I_{LED} + \frac{\Delta i_{L-PP}}{2} = 1.5A + \frac{308\ mA}{2} = 1.65A$$

Assume V_{ADJ} = 1.24V and solve for R9:

$$R9 = \frac{V_{ADJ}}{5 \times I_{L-MAX}} = \frac{1.24V}{5 \times 1.65A} = 0.15\ \Omega$$

The closest 1% tolerance resistor is 0.15 Ω therefore the I_{LED} is:

$$I_{LED} = \frac{V_{ADJ}}{5 \times R9} - \frac{\Delta i_{L-PP}}{2}$$

$$I_{LED} = \frac{1.24V}{5 \times 0.15\ \Omega} - \frac{308\ mA}{2} = 1.5\ A$$

The chosen component from step 3 is:

R9 = 0.15Ω

4. OUTPUT CAPACITANCE

No output capacitance is necessary.

5. INPUT CAPACITANCE

Determine t_{ON}:

$$t_{ON} = \frac{1}{f_{SW}} - t_{OFF} = \frac{1}{404\ kHz} - 242\ ns = 2.23\ \mu s$$

Solve for C_{IN-MIN}:

$$C_{IN-MIN} = \frac{I_{LED} \times t_{ON}}{\Delta v_{IN-PP}} = \frac{1.5\ A \times 2.23\ \mu s}{1.44V} = 2.32\ \mu F$$

Choose C_{IN}:

$$C_{IN} = C_{IN-MIN} \times 1.75 = 4.07\ \mu F$$

Determine I_{IN-RMS}:

$$I_{IN-RMS} = I_{LED} \times f_{SW} \times \sqrt{t_{ON} \times t_{OFF}}$$

$$I_{IN-RMS} = 1.5\ A \times 404\ kHz \times \sqrt{2.32\ \mu s \times 242\ ns} = 446\ mA$$

The chosen components from step 5 are:

C1 = C2 = 2.2 µF
C3 = 0.1 µF

6. P-CHANNEL MOSFET

Determine minimum Q1 voltage rating and current rating:

$$V_{T\text{-}MAX} = V_{IN\text{-}MAX} = 75V$$

$$I_T = D \times I_{LED} = \frac{V_O \times I_{LED}}{V_{IN} \times \eta} = \frac{42V \times 1.5\,A}{48V \times 0.97} = 1.35A$$

A 100V 3.8A PFET is chosen with $R_{DS\text{-}ON}$ = 190mΩ and Q_g = 20nC. Determine $I_{T\text{-}RMS}$ and P_T:

$$I_{T\text{-}RMS} = I_{LED} \times \sqrt{D \times \left(1 + \frac{1}{12} \times \left(\frac{\Delta i_{L\text{-}PP}}{I_{LED}}\right)^2\right)}$$

$$I_{T\text{-}RMS} = 1.5A \times \sqrt{\frac{42V}{48V \times 0.97} \times \left(1 + \frac{1}{12} \times \left(\frac{308mA}{1.5A}\right)^2\right)}$$

$$I_{T\text{-}RMS} = 1.43A$$

$$P_T = I_{T\text{-}RMS}{}^2 \times R_{DSON} = 1.43A^2 \times 190\,m\Omega = 387\,mW$$

The chosen component from step 6 is:

Q1 → 3.8A,100V, DPAK

7. RE-CIRCULATING DIODE

Determine minimum D1 voltage rating and current rating:

$$V_{D\text{-}MAX} = V_{IN\text{-}MAX} = 75V$$

$$I_D = (1\text{-}D) \times I_{LED} = \left(1 - \frac{V_O}{V_{IN} \times \eta}\right) \times I_{LED}$$

$$I_D = \left(1 - \frac{42V}{48V \times 0.97}\right) \times 1.5\,A = 147\,mA$$

A 100V 3A diode is chosen with V_D = 750mV. Determine P_D:

$$P_D = I_D \times V_D = 147\,mA \times 750\,mV = 110\,mW$$

The chosen component from step 7 is:

D1 → 3A,100V, SMC

8. INPUT UNDER-VOLTAGE LOCKOUT (UVLO)

Solve for R8:

$$R8 = \frac{V_{HYS}}{22\,\mu A} = \frac{1.1V}{22\,\mu A} = 50\,k\Omega$$

The closest 1% tolerance resistor is 49.9 kΩ so V_{HYS} is:

$$V_{HYS} = R8 \times 22\,\mu A = 49.9\,k\Omega \times 22\,\mu A = 1.1V$$

Solve for R7:

$$R7 = \frac{1.24V \times R8}{V_{TURN\text{-}ON} - 1.24V} = \frac{1.24V \times 49.9\,k\Omega}{10V - 1.24V} = 7.06\,k\Omega$$

The closest 1% tolerance resistor is 6.98 kΩ so $V_{TURN\text{-}ON}$ is:

$$V_{TURN\text{-}ON} = \frac{1.24V \times (R7 + R8)}{R7}$$

$$V_{TURN\text{-}ON} = \frac{1.24V \times (6.98\,k\Omega + 49.9\,k\Omega)}{6.98\,k\Omega} = 10.1V$$

The chosen components from step 8 are:

R7 = 6.98 kΩ
R8 = 49.9 kΩ

9. IADJ CONNECTION METHOD

The IADJ pin controls the high-side current sense threshold in three ways outlined in the datasheet. The LM3409HV evaluation board allows for all three methods to be evaluated using C6, R10, and the VADJ terminal.

Method #1: If the VADJ terminal is not connected to the power supply, then the internal Zener diode biases the pin to 1.24V and the current sense threshold is nominally 248mV.

Method #2: Applying an external voltage to the VADJ terminal between 0 and 1.24V linearly scales the current sense threshold between 0 and 248mV nominally. It can be necessary to have an RC filter when using an external power supply in order to remove any high frequency noise or oscillations created by the power supply and the connecting cables. The filter is chosen by assuming a standard value of C6 = 0.1µF and solving for a cut-off frequency f_C < 2kHz:

$$R10 > \frac{1}{2\pi \times f_C \times C6} = \frac{1}{2\pi \times 2\,kHz \times 0.1\mu F} = 796\Omega$$

Since an exact f_C is not critical, a standard value of 1kΩ is used. The *Typical Waveforms* section shows a typical LED current waveform when analog dimming using an external voltage source.

Method #3: (This method requires modification of the received evaluation board). The internal 5µA current source can be used to bias the voltage across an external resistor to ground (R_{EXT}) across C6 on the evaluation board. The resistor is sized knowing the desired average LED current I_{LED} (must be < 1.5A which is default using method #1):

$$R_{EXT} = \frac{\left(I_{LED} + \frac{\Delta i_{L\text{-}PP}}{2}\right) \times R9}{1\,\mu A} = \frac{\left(I_{LED} + \frac{308\,mA}{2}\right) \times 150\,m\Omega}{1\,\mu A}$$

The chosen components from step 9 are:

C6 = 0.1 µF
R10 = 1 kΩ

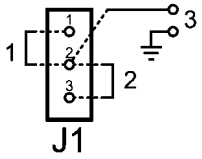
10. PWM DIMMING METHOD

The LM3409HV evaluation board allows for PWM dimming to be evaluated as follows:

1: No PWM, EN = V_{IN}

2: External PWM, EN coupled

3: Internal PWM, using EN



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Method #1: If no PWM dimming is desired, a jumper should be placed in position 1 (shorts pins 1 and 2) on header J1. This shorts VIN and EN which ensures the controller is always enabled if an input voltage greater than 1.74V is applied.

Method #2: External parallel FET shunt dimming can be evaluated by placing the jumper in position 2 (shorts pins 2 and 3) on header J1. This connects the capacitive coupling circuit to the EN pin as suggested in the datasheet. The resistor (R4) can be solved for assuming a standard capacitor value C9 = 2.2nF and a desired time constant (t_C = 220ns < t_{OFF}) as follows:

$$R4 = \frac{t_C}{C9} = \frac{220\,ns}{2.2\,nF} = 100\Omega$$

The external shunt FET dimming circuit shown below is designed using an N-channel MosFET (Q3), a CMOS FET (Q2), two gate current limiting resistors (R1 and R2), a pull-up resistor (R3), and a bypass capacitor (C5). With an external 5V power supply attached to the 5V terminal and an external PWM signal attached to the PWM2 terminal, the shunt dimming circuit is complete. Q3 is the shunt dimFET which conducts the LED current when turned on and blocks the LED voltage when turned off. Q3 needs to be fast and rated for V_O and I_{LED}. For design flexibility, a fast 100V, 7.5A NFET is chosen. Q2 is necessary to invert the PWM signal so it properly translates the duty cycle to the shunt dimming FET. Q2 also needs to be fast and rated for 5V and fairly small current, therefore a 30V, 2A fast CMOS FET was chosen. R1 and R2 are 1Ω resistors to slow down the rising edge of the FETs slightly to prevent the gate from ringing. R3 is a 10kΩ pull-up resistor to ensure the CMOS gate is pulled all the way to 5V if a sub-5V PWM signal is applied to PWM2. The bypass capacitor (C5) for the 5V power supply is chosen to be 0.1µF. See the *Shunt FET Circuit Modification* section for an improvement that can be made to this circuit.

Method #3: Internal PWM dimming using the EN pin can be evaluated by removing the jumper from header J1. An external PWM signal can then be applied to the EN terminal to provide PWM dimming.

The *Typical Waveforms* section shows typical LED current waveforms during both types of PWM dimming.

The chosen components from step 10 are:

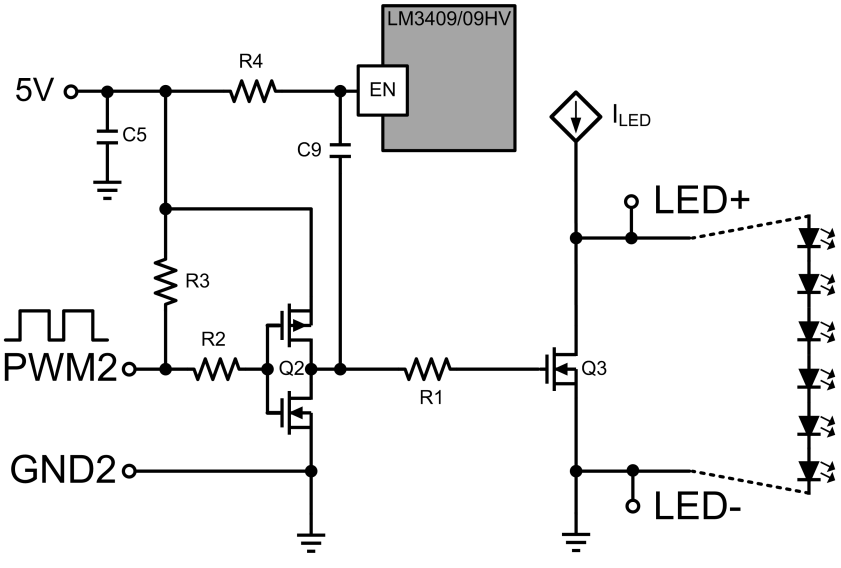
C6 = 0.1 µF
C9 = 2.2 nF
R1 = R2 = 1Ω
R3 = 10 kΩ
R4 = 100Ω
Q2 → 30V, 20A, SOT - 6, CMOS
Q3 → 100V,7.5A, SOIC - 8, NMOS

11. BYPASS CAPACITOR

The internal regulator requires at least 1µF of ceramic capacitance with a voltage rating of 16V.

The chosen component from step 11 is:

C4 = 1.0 µF



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External shunt FET dimming circuit with EN pin coupling

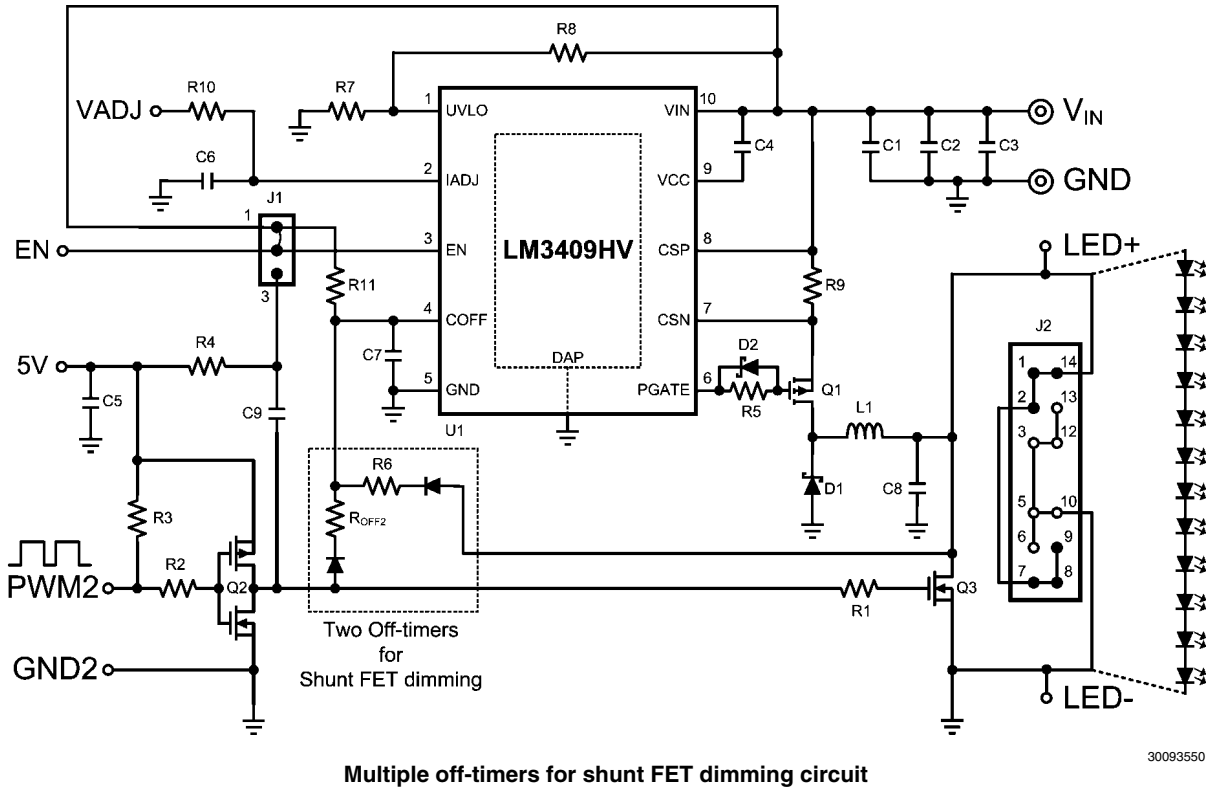
Shunt FET Circuit Modification

When the shunt FET (Q3) is on, the LM3409 is driving current into a short, therefore a maximum off-time (typical 300 µs) occurs followed by a minimum on-time. Maximum off-time followed by minimum on-time continues until Q3 is turned off. At low dimming frequencies and depending on the duty cycle, the inductor current may be at a very low level when the Q3 turns off. This will eliminate the benefits of using the shunt FET over the EN pin because the inductor will have to slew the current back to the nominal value anyways.

A simple modification to the external parallel FET dimming circuit will keep the inductor current close to its nominal value when Q3 is turned off. This modification will ensure that the rise time of the LED current is only limited by the turn-off time of the shunt FET as desired. The following circuit additions allow for two different off-times to occur. When Q3 is off, the standard off-timer referenced from V_O is set. However when the Q3 is on, a second off-timer referenced to the gate signal of the Q3 is enabled and a controlled (non-maximum) off-time is set.

This modification includes 2 extra diodes (i.e. BAT54H) and one resistor (R_{OFF2}) and is only relevant when shunt FET PWM dimming below 10 kHz or so. In general, this second off-timer should be set to allow the inductor current to fall no more than 10% of its nominal value. A simple approximation can be used to find R_{OFF2}:

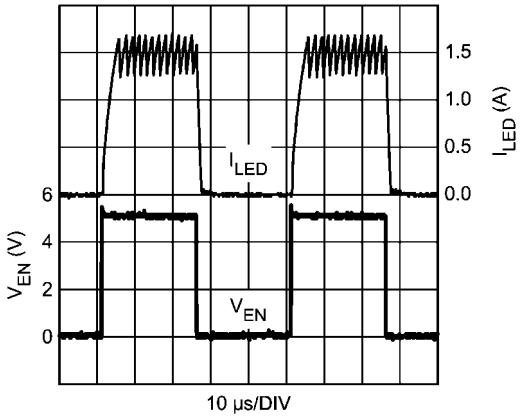
$$R_{OFF2} < \frac{0.1 \times L \times I_{LED}}{C7 \times V_O}$$



Multiple off-timers for shunt FET dimming circuit

Typical Waveforms

T_A = +25°C, V_{IN} = 48V and V_O = 42V.



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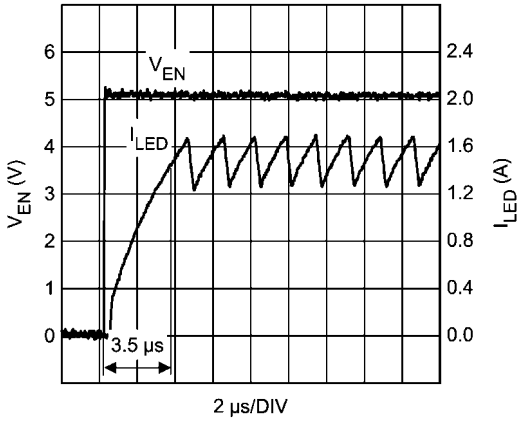
20kHz 50% EN pin PWM dimming



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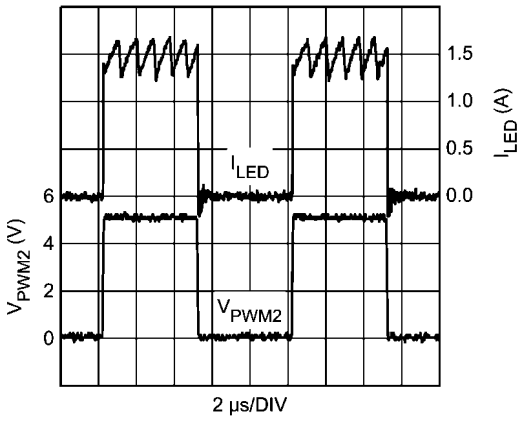
20kHz 50% EN pin PWM dimming (rising edge)



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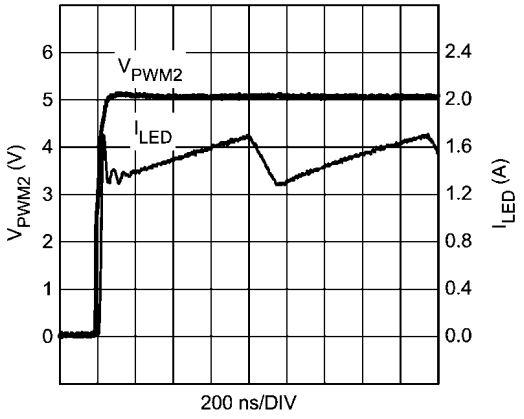
100kHz 50% External FET PWM dimming



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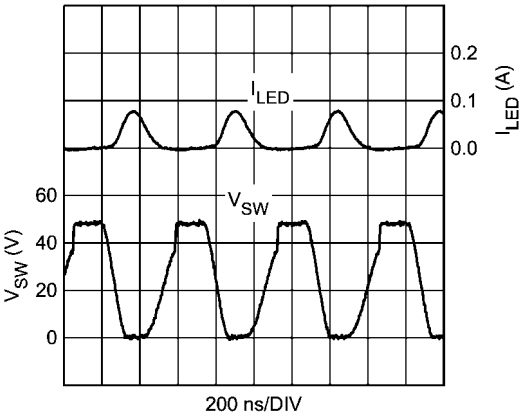
100kHz 50% External FET PWM dimming (rising edge)



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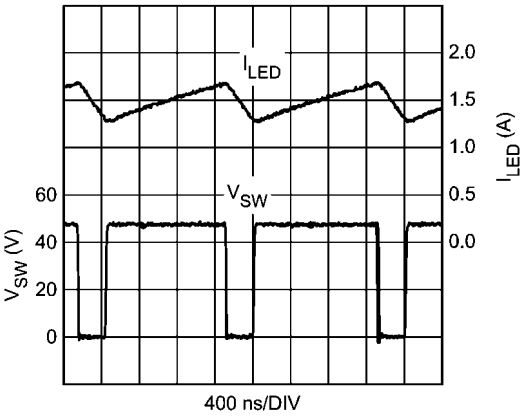
Analog dimming minimum (V_{ADJ} = 0V)



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Analog dimming maximum (V_{ADJ} open)

Alternate Designs

Alternate designs with the LM3409HV evaluation board are possible with very few changes to the existing hardware. The evaluation board FETs and diodes are already rated higher than necessary for design flexibility. The input UVLO can remain the same and the input capacitance is sufficient for most designs, though the input voltage ripple will change. Other designs can evaluated by changing R6, R9, L1, and C8.

The table below gives the main specifications for five different designs and the corresponding values for R6, R9, L1 and C8. The RMS current rating of L1 should be at least 50% higher than the specified I_{LED}. Designs 3 and 5 are optimized for best analog dimming range, while designs 1, 2, and 4 are optimized for best PWM dimming range. These are just examples, however any combination of specifications can be achieved by following the *Design Procedure* in the LM3409/09HV datasheet.

Specification / Component	**Design 1**	**Design 2**	**Design 3**	**Design 4**	**Design 5**
Dimming Method	PWM	PWM	Analog	PWM	Analog
V_{IN}	24V	36V	48V	65V	75V
V_O	14V	24V	35V	56V	42V
f_{SW}	500 kHz	450 kHz	300 kHz	350 kHz	300 kHz
I_{LED}	1A	700 mA	2A	3A	1.5A
Δi_{LED}	450 mA	250 mA	70 mA	1A	80 mA
R6	15.4 kΩ	25.5 kΩ	46.4 kΩ	24.9 kΩ	95.3 kΩ
R9	0.2Ω	0.3Ω	0.12Ω	0.07Ω	0.15Ω
L1	22 µH	68 µH	150 µH	15 µH	330 µH
C8	None	None	2.2 µF	None	2.2 µF

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Data Converters	www.national.com/adc	Samples	www.national.com/samples
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