Title	***Reference Design Report for a High Efficiency (≥81%), High Power Factor (>0.9) TRIAC Dimmable 7 W$_{TYP}$ LED Driver Using LinkSwitch®-PH LNK403EG***
Specification	90 VAC – 265 VAC Input; 21 V$_{TYP}$, 0.33 A Output
Application	LED Driver
Author	Applications Engineering Department
Document Number	RDR-193
Date	June 9, 2010
Revision	1.0

Summary and Features

- Superior performance and end user experience
  - TRIAC dimmer compatible (including low cost leading edge type)
    - No output flicker
    - >1000:1 dimming range
  - Clean monotonic start-up – no output blinking
  - Fast start-up (<100 ms) – no perceptible delay
  - Consistent dimming performance unit to unit
- Highly energy efficient
  - ≥81% at 115 VAC, ≥82% at 230 VAC
- Low cost, low component count and small printed circuit board footprint solution
  - No current sensing required
  - Frequency jitter for smaller, lower cost EMI filter components
- Integrated protection and reliability features
  - Output open circuit / output short-circuit protected with auto-recovery
  - Line input overvoltage shutdown extends voltage withstand during line faults.
  - Auto-recovering thermal shutdown with large hysteresis protects both components and printed circuit board
  - No damage during brown-out or brown-in conditions
- Meets IEC 61000-4-5 ringwave, IEC 61000-3-2 Class C harmonics and EN55015 B conducted EMI

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

The document describes a high power-factor corrected dimmable LED driver designed to drive 21 V at 0.33 A from an input voltage range of 90 VAC to 265 VAC. The LED driver utilizes the LNK403EG from Power Integrations.

LinkSwitch-PH ICs allow the implementation of cost effective and low component count LED drivers which both meet power factor and harmonics limits but also offer enhanced end user experience. This includes ultra-wide dimming range, flicker free operation (even with low cost with AC line TRIAC dimmers) and fast, clean turn on.

The topology used is an isolated Flyback operating in continuous conduction mode. Output current regulation is sensed entirely from the primary side eliminating the need for secondary side feedback components. No external current sensing is required on the primary side either as this is performed inside the IC further reducing components and losses. The internal controller adjusts the MOSFET duty cycle to maintain a sinusoidal input current and therefore high power factor and low harmonic currents.

The LNK403EG also provides a sophisticated range of protection features including auto-restart for open control loop and output short-circuit conditions. Line overvoltage provides extended line fault and surge withstand, output overvoltage protects the supply should the load be disconnect and accurate hysteretic thermal shutdown ensures safe average PCB temperatures under all conditions.

In any LED luminaire the driver determines many of the performance attributes experienced by the end customer (user) including startup time, dimming, flicker and unit to unit consistency. For this design a focus was given to compatibility with as wider range of dimmers and as large of a dimming range as possible, at both 115 VAC and 230 VAC. However simplification of the design is possible for both single input voltage operation, no dimming or operation with a limited range of (higher quality) dimmers.

This document contains the LED driver specification, schematic, PCB diagram, bill of materials, transformer documentation and typical performance characteristics.

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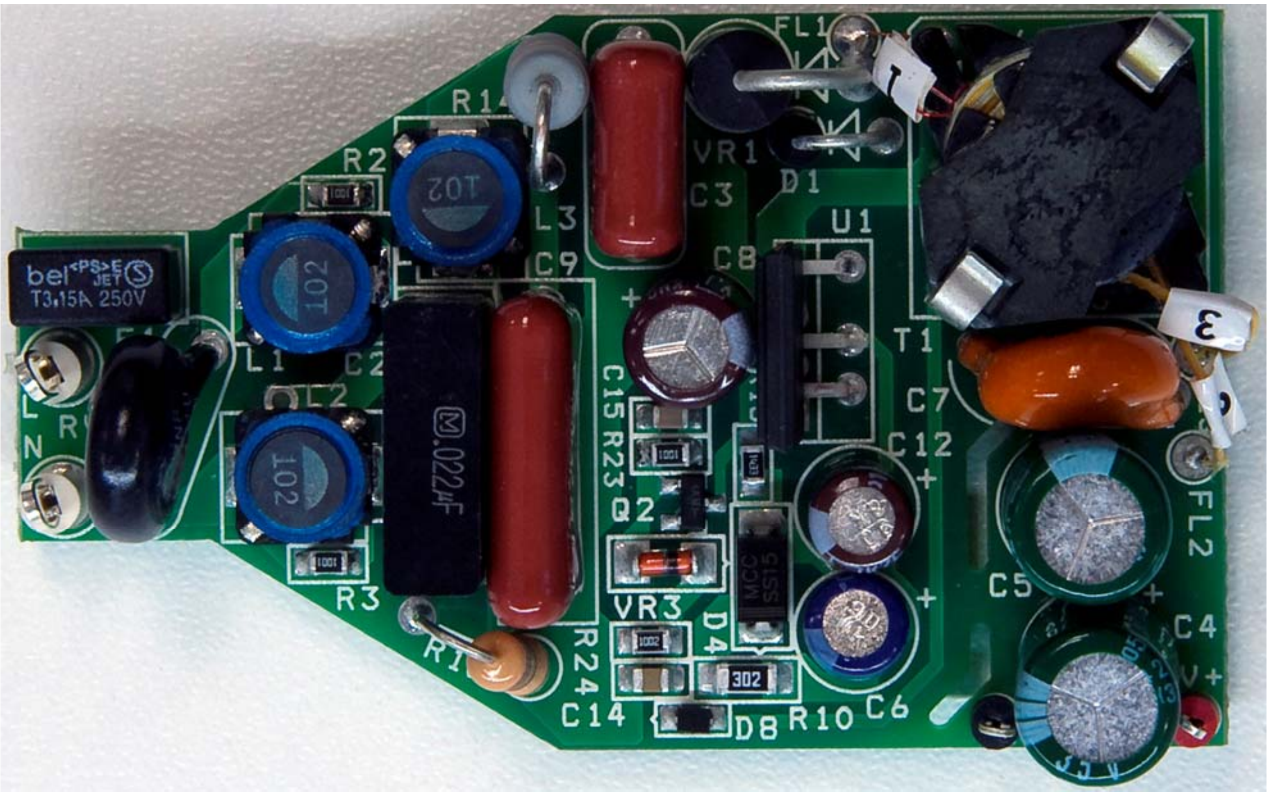

Figure 1 – Populated Circuit Board Photograph (Top View).
PCB Outline Designed to Fit Inside PAR20 Enclosure.

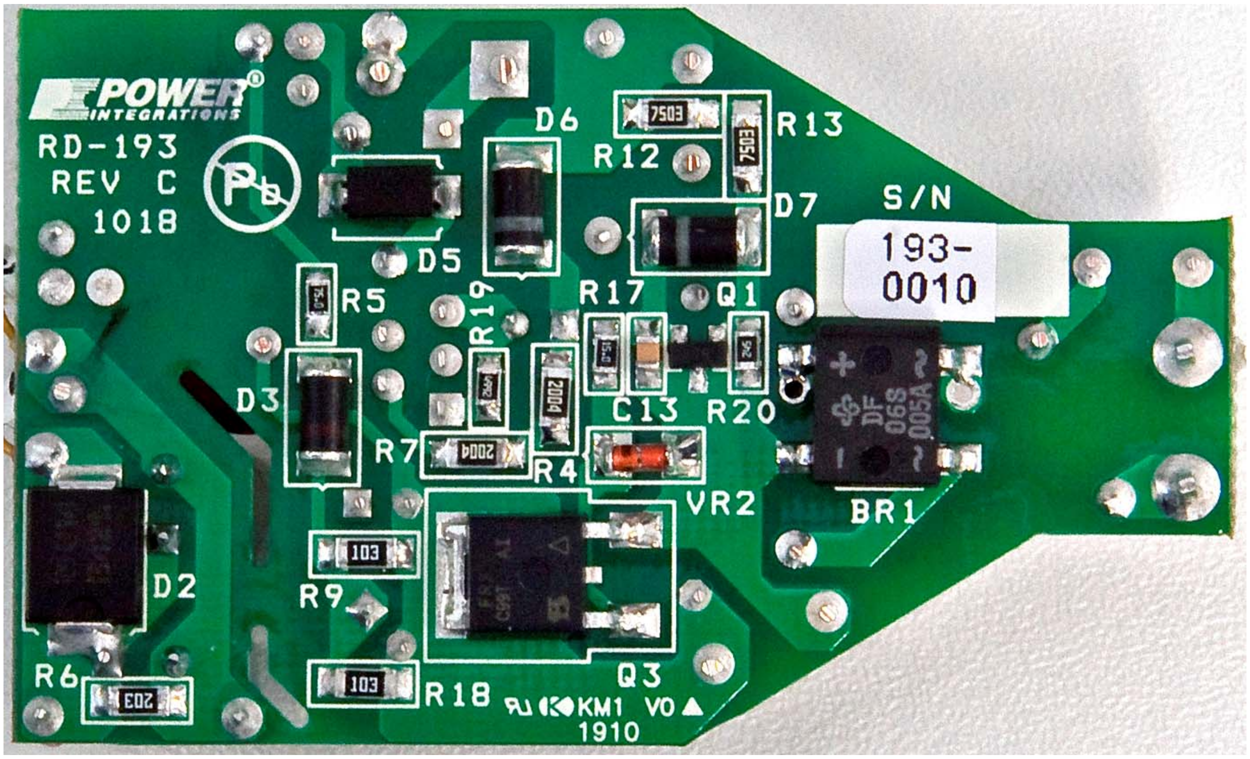

Figure 2 – Populated Circuit Board Photograph (Bottom View).

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage [a]	V_{IN}	90	115	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage	V_{OUT}	18	21	24	V	
Output Current [a]	I_{OUT}		0.33		A	V_{OUT} = 21, V_{IN} = 115 VAC, 25°C
Total Output Power						
Continuous Output Power	P_{OUT}		7		W	
Efficiency						
Full Load	η	80			%	Measured at P_{OUT} 25 °C
Environmental						
Conducted EMI		Meets CISPR 15B / EN55015B				
Safety		Designed to meet IEC950 / UL1950 Class II				
Ring Wave (100 kHz)						
Differential Mode (L1-L2)			2.5		kV	IEC 61000-4-5 , 200 A
Common mode (L1/L2-PE)						
Power Factor		0.9				Measured at $V_{OUT(TYP)}$, $I_{OUT(TYP)}$ and 115/230 VAC
Harmonics		EN 61000-3-2 Class D				
Ambient Temperature [b]	T_{AMB}		40		°C	Free convection, sea level

Notes:

[a] When configured for phase controlled (TRIAC) dimming, in order to give the widest dimming range, the output current for a LinkSwitch-PH design varies with line voltage. Therefore the output current specification is defined at a single line voltage only. For this design a line voltage of 115 VAC was selected. At higher line voltages the output current will increase and reduce with lower line voltages. The typical output current variation is +30% for +200% increase in line voltage. A single resistor value change can be used to center the nominal output current for a given nominal line voltage. See Table 1 for the feedback resistor value vs. nominal line voltage.

[b] Maximum ambient temperature specification may be increased by adding a small heatsink to the LinkSwitch-PH device.

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3 Schematic

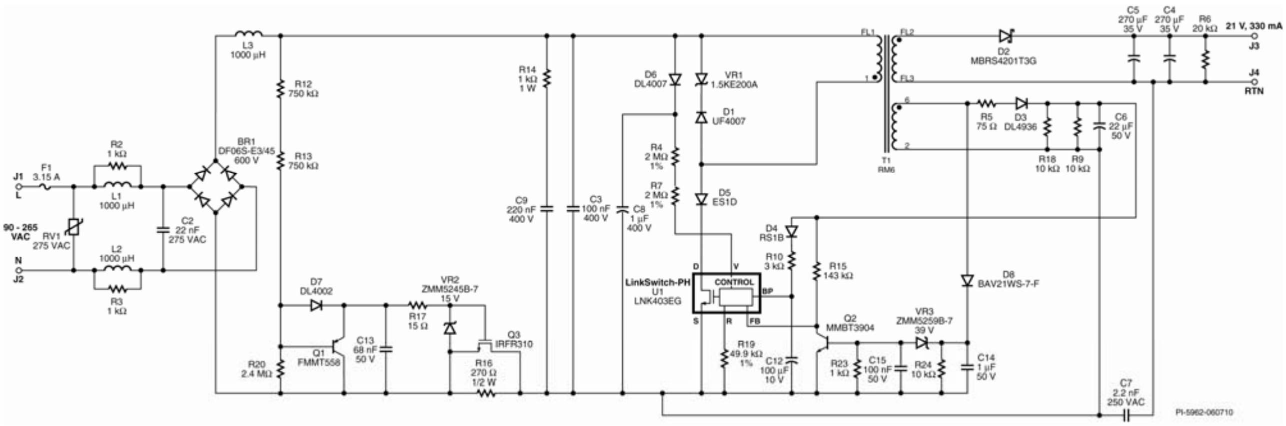

Figure 3 – Schematic.

4 Circuit Description

The LinkSwitch-PH device is a controller and integrated 725 V MOSFET intended for use in LED driver applications. The LinkSwitch-PH is configured for use in a single-stage continuous conduction mode Flyback topology and provides a primary side regulated constant current output while maintaining high power factor from the AC input.

4.1 Input Filtering

Fuse F1 fuses the input and BR1 rectifies the AC line voltage. Inductor L1-L3, C2, R2, and R3 form EMI filter with C7 Y capacitor. Small bulk capacitor C3 is required for a low impedance path for the primary switching current. A low value of capacitance is necessary to maintain a power factor of greater than 0.9.

4.2 LinkSwitch-PH Primary

Diode D6 and C8 detect the peak AC line voltage. This voltage is converted to a current into the V pin via R4 and R7. This current is also used by the device to set the input over/undervoltage protection thresholds. The V pin current and the FB pin current are used internally to control the average output LED current. TRIAC phase-angle dimming applications require 49.9 kΩ resistors on the R pin and 4 MΩ on the V pin to provide a linear relationship between input voltage and the output current. Resistor R4 also sets the internal references to select the brown-in and brown-out and input overvoltage protection thresholds.

Diode D1 and VR1 clamp the drain voltage to a safe level from the leakage inductance voltage spike. Diode D5 is necessary to prevent reverse current from flowing through the LinkSwitch-PH device.

4.3 Bias and Output Rectification

Diode D3, C6, R5, R9 and R18 create the primary bias supply. This voltage created from the transformer bias winding supplies bias current into the BYPASS pin through D4 and R10. Capacitor C12 is the main supply for the LinkSwitch-PH, which is charged to ~6 V at start-up from an internal high-voltage current source tied to the device DRAIN pin. A current proportional to the output voltage from the primary bias winding is fed into the FEEDBACK pin through R15. Diode D2 rectifies the secondary winding while capacitors C4 and C5 filter the output. Diode D8, R24, C14, VR3, C15, R23, and Q2 provide an open load overvoltage protection function. This protects output capacitors, C4 and C5 from excessive voltage should the load be disconnected.

4.4 TRIAC Phase Dimming Control

Components R12, R13, R20, R17, D7, Q1, C13, VR2, and Q3 in conjunction with R16 reduce the inrush current when the TRIAC dimmer turns on. This circuit allows the inrush current to flow through R16 for the first 2.4 ms at 115 VAC (1.2 ms at 230 VAC) of the TRIAC conduction. After approximately 2.4 ms, Q3 turns on and shorts R16. This keeps the power dissipation on R16 low. Resistor R12, R13, R20 and C13 provide a 2.4 ms

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delay after the TRIAC conducts. Transistor Q1 discharges C13 when the TRIAC is not conducting. Zener VR2 clamps the gate voltage of Q3 to 15 V.

Capacitor C9 and R14 keep the TRIAC current above the holding threshold to prevent multiple firings.

5 PCB Layout

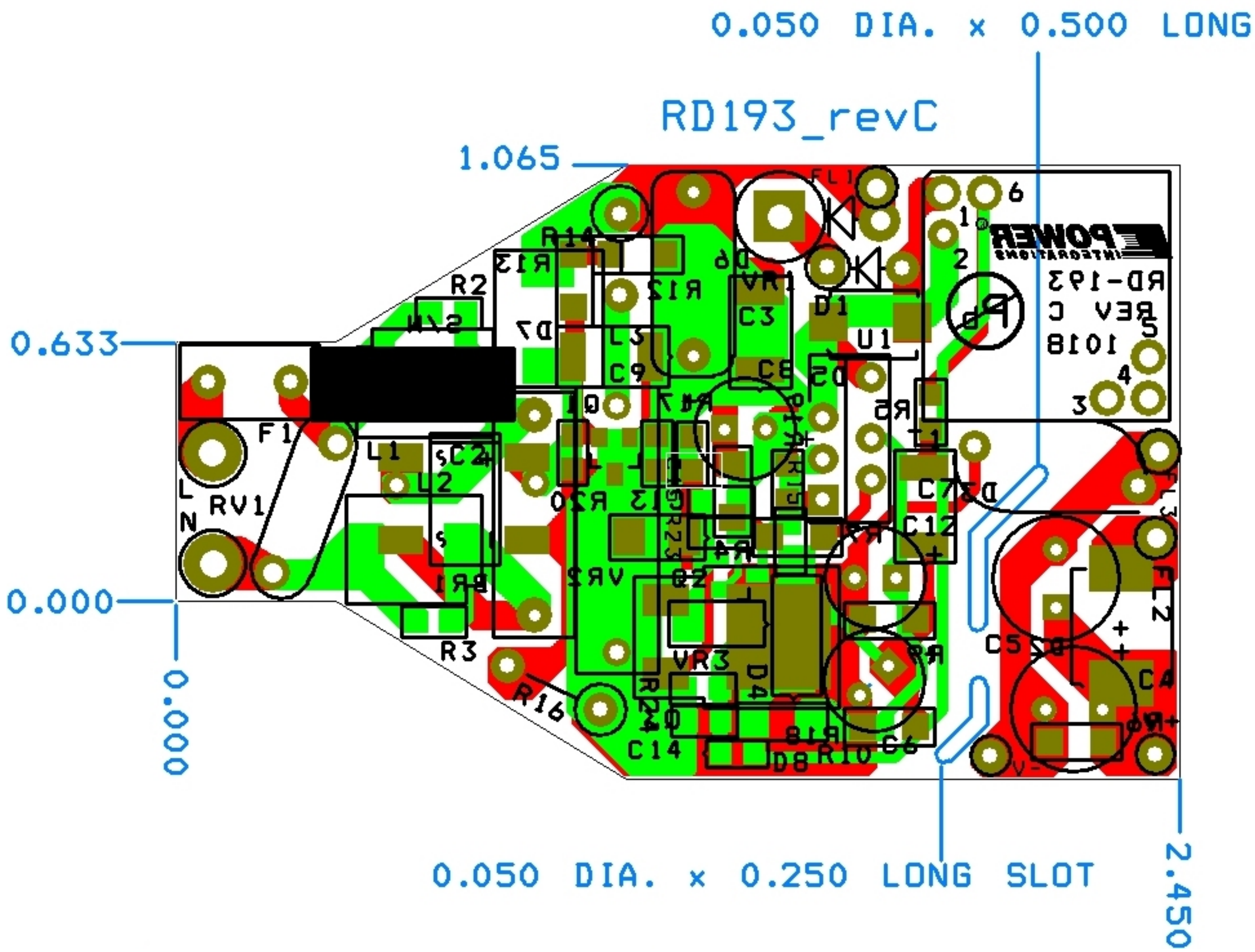

Figure 4 – Printed Circuit Layout (Designed to Fit Inside PAR20 Lamp Form Factor).

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 1 A, Bridge Rectifier, SMD, DFS	DF06S-E3/45	Vishay
2	1	C2	22 nF, 275VAC, Film, X2	ECQ-U2A223ML	Panasonic
3	1	C3	100 nF, 400 V, Film	ECQ-E4104KF	Panasonic
4	2	C4 C5	270 μF, 35 V, Electrolytic, Very Low ESR, 41 mΩ, (8 x 20)	EKZE350ELL271MH20D	Nippon Chemi-Con
5	1	C6	22 μF, 50 V, Electrolytic, Low ESR, 900 mΩ, (5 x 11.5)	ELXZ500ELL220MEB5D	Nippon Chemi-Con
6	1	C7	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
7	1	C8	1 μF, 400 V, Electrolytic, (6.3 x 11)	EKMG401ELL1R0MF11D	United Chemi-Con
8	1	C9	220 nF, 400 V, Film	ECQ-E4224KF	Panasonic
9	1	C12	100 μF, 10 V, Electrolytic, Very Low ESR, 300 mΩ, (5 x 11)	EKZE100ELL101ME11D	Nippon Chemi-Con
10	1	C13	68 nF, 50 V, Ceramic, X7R, 0805	ECJ-2YB1H683K	Panasonic
11	1	C14	1 μF, 50 V, Ceramic, X7R, 0805	08055D105KAT2A	AVX Corporation
12	1	C15	100 nF, 50 V, Ceramic, X7R, 0805	ECJ-2YB1H104K	Panasonic
13	1	D1	1000 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4007-E3	Vishay
14	1	D2	200 V, 4 A, Schottky, SMC, DO-214AB	MBRS4201T3G	ON Semiconductor
15	1	D3	400V, 1 A, Rectifier, Fast Recovery, MELF (DL-41)	DL4936-13-F	Diodes Inc
16	1	D4	100 V, 1 A, Fast Recovery, 150 ns, SMA	RS1B-13-F	Diodes, Inc
17	1	D5	200 V, 1 A, Ultrafast Recovery, 25 ns, DO-214AC	ES1D	Vishay
18	1	D6	1000 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4007-13-F	Diodes Inc
19	1	D7	100 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4002-13-F	Diodes Inc
20	1	D8	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diode Inc.
21	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
22	3	FL1 FL2 FL3	PCB Terminal Hole, 22 AWG	N/A	N/A
23	2	L N	Test Point, WHT,THRU-HOLE MOUNT	5012	Keystone
24	3	L1 L2 L3	1000 μH, 0.14 A	SLF7045T-102MR14-PF	TDK Corporation
25	1	Q1	PNP, 400V 150MA, SOT-23	FMMT558TA	Zetex Inc
26	1	Q2	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-23	MMBT3904LT1G	On Semiconductor
27	1	Q3	400 V, 1.7 A, 3.6 Ω, N-Channel, DPAK	IRFR310TRPBF	Vishay
28	3	R2 R3 R23	1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
29	2	R4 R7	2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
30	1	R5	75 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ750V	Panasonic
31	1	R6	20 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ203V	Panasonic
32	2	R9 R18	10 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ103V	Panasonic
33	1	R10	3 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ302V	Panasonic
34	2	R12 R13	750 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7503V	Panasonic
35	1	R14	1 kΩ, 5%, 1 W, Metal Oxide	RSF100JB-1K0	Yageo
36	1	R15	143 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1433V	Panasonic

37	1	R16	270 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-270R	Yageo
38	1	R17	15 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF15R0V	Panasonic
39	1	R19	49.9 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4992V	Panasonic
40	1	R20	2.4 MΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ245V	Panasonic
41	1	R24	10 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
42	1	RV1	275 V, 80J, 10 mm, RADIAL	ERZ-V10D431	Panasonic
43	1	T1	Custom Transfomer, RM6,6pins	SNX-R1537	Santronics USA
44	1	TP3	Test Point, RED,Miniature THRU-HOLE MOUNT	5000	Keystone
45	1	TP4	Test Point, BLK,Miniature THRU-HOLE MOUNT	5001	Keystone
46	1	U1	LinkSwitch, LNK406EG, eSIP	LNK406EG	Power Integrations
47	1	VR1	200 V, 1500W, TVS, GP-20	1.5KE200A-E3/54	Vishay
48	1	VR2	15 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5245B-7	Diodes Inc
49	1	VR3	39V, 5%, 500 mW, DO-213AA (MELF)	ZMM5259B-7	Diodes Inc

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7 Transformer Specification

7.1 Electrical Diagram

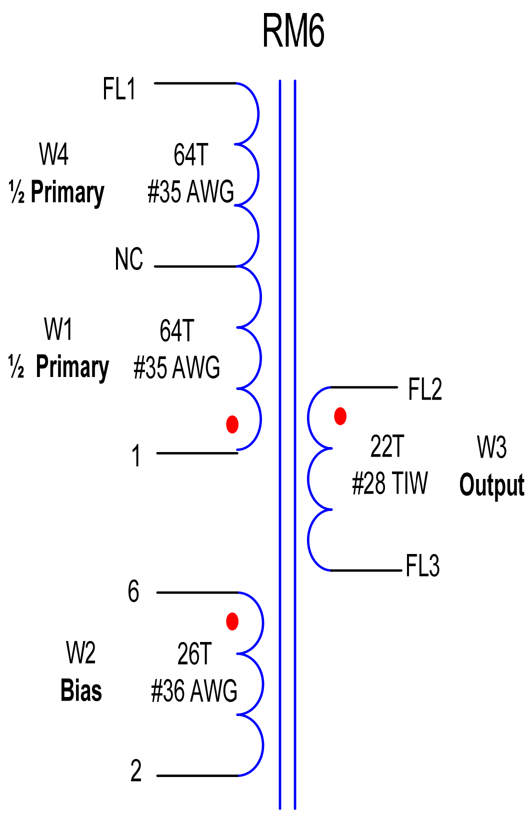

Figure 5 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1, 2, 6, FL1 to FL2, FL3	3000 VAC
Primary Inductance	Pins 1-FL1, all other windings open, measured at 100 kHz, 0.4 VRMS	2.45 mH ± 10%
Resonant Frequency	Pins 1-FL1, all other windings open	750 kHz (Min.)
Primary Leakage Inductance	Pins 1-FL1 with FL2-FL3 shorted, measured at 100 kHz, 0.4 VRMS	35 μH ± 10%

7.3 Materials

Item	Description
[1]	Core: PC95RM6 from TDK or equivalent, ALG = 149.5nH/n^2
[2]	Bobbin: 6 pin vertical, B-RM6-V-6P from Epcos, or equivalent
[3]	Magnet Wire: #35 AWG.
[4]	Magnet Wire: #36 AWG
[5]	Magnet Wire: #28 AWG T.I.W.
[6]	Tape: 3M 1298 Polyester Film, 7 mm wide.
[7]	Mounting clip, CLI/P-RM6, and varnish.

7.4 Transformer Build Diagram

Pins Side

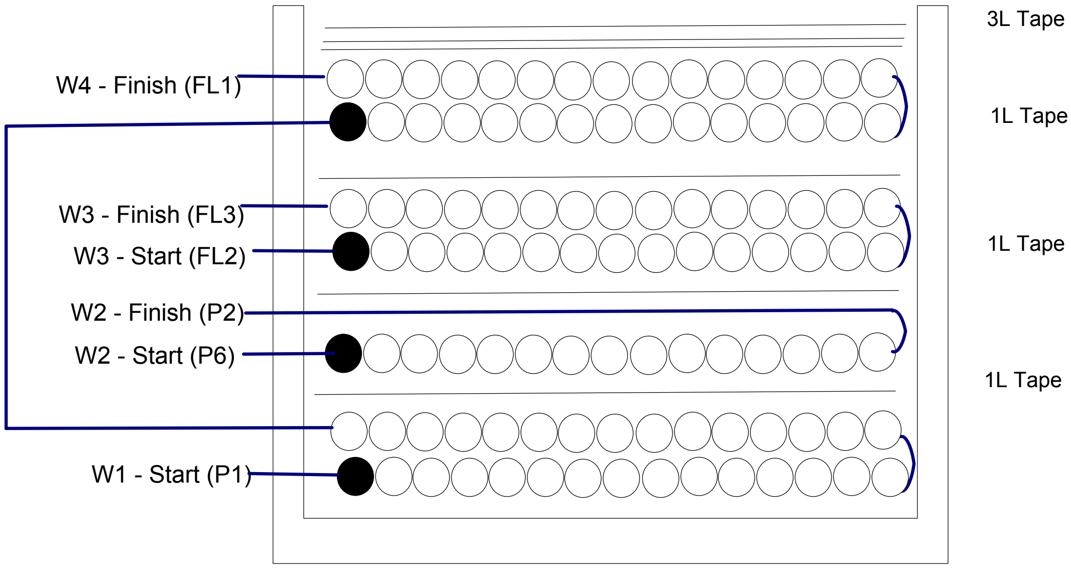

Figure 6 – Transformer Build Diagram.

7.5 Transformer Construction

Bobbin Preparation	Place the bobbin item [2] on the mandrel such that pin side on the left side. Winding direction is the clockwise direction.
WD 1	Start at pin 1, wind 64 turns of #35 AWG item [3] from left to right two layers. At the last turn exit the same slot, leave enough length wire floating to wind next 64 turns in WD4.
Insulation	Apply one layer of tape [6] for insulation.
WD 2	Start at pin 6, wind 26 turns of #36 AWG [4] wire from left to right. Finish at pin 2.
Insulation	Apple one layer of tape [6] for insulation.
WD 3	Leave about 1” of wire item [5], use small tape to mark as FL2, enter into slot of secondary side of bobbin, wind 22 turns in two layers. At the last turn exit the same slot, leave about 1”, and mark as FL3.
Insulation	Apple one layer of tape [6] for insulation.
WD 4	Continue to wind with floating wire, 64 turns of #35 AWG from left to right two layers. Leave 1” and mark as FL1
Insulation	Apply three layers of tape [6] for insulation.
Final Assembly	Cut FL1, FL2, FL3 wire length to 0.75”. Grind core. Assemble core and varnish using item [7].

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8 Transformer Design Spreadsheet

ACDC LinkSwitch-PH 042910; Rev.1.0; Copyright Power Integrations 2010	INPUT	INFO	OUTPUT	UNIT	LinkSwitch-PH_042910: Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
Dimming required	**YES**	*Info*	**YES**		!!! Info. When configured for dimming, best output current line regulation is achieved over a single input voltage range.
VACMIN			90	V	Minimum AC Input Voltage
VACMAX	265		265	V	Maximum AC input voltage
fL			50	Hz	AC Mains Frequency
VO	21.00			V	Typical output voltage of LED string at full load
VO_MAX			23.10	V	Maximum expected LED string Voltage.
VO_MIN			18.90	V	Minimum expected LED string Voltage.
V_OVP			25.41	V	Over-voltage protection setpoint
IO	0.33				Typical full load LED current
PO			6.9	W	Output Power
n			0.8		Estimated efficiency of operation
VB	25		25	V	Bias Voltage
ENTER LinkSwitch-PH VARIABLES					
LinkSwitch-PH	**LNK403**			Universal	115 Doubled/230V
Chosen Device		LNK403	Power Out	12.5W	12.5W
Current Limit Mode	**FULL**		FULL		Select "RED" for reduced Current Limit mode or "FULL" for Full current limit mode
ILIMITMIN			0.81	A	Minimum current limit
ILIMITMAX			0.92	A	Maximum current limit
fS			66000	Hz	Switching Frequency
fSmin			62000	Hz	Minimum Switching Frequency
fSmax			70000	Hz	Maximum Switching Frequency
IV			39.9	uA	V pin current
RV			4	M-ohms	Upper V pin resistor
RV2			1E+12	M-ohms	Lower V pin resistor
IFB	139.00		139.0	uA	FB pin current (85 uA < IFB < 210 uA)
RFB1			158.3	k-ohms	FB pin resistor
VDS			10	V	LinkSwitch-PH on-state Drain to Source Voltage
VD	0.50			V	Output Winding Diode Forward Voltage Drop (0.5 V for Schottky and 0.8 V for PN diode)
VDB	0.70			V	Bias Winding Diode Forward Voltage Drop
Key Design Parameters					
KP	1.06		1.06		Ripple to Peak Current Ratio (For PF > 0.9, 0.4 < KP < 0.9)
LP			2450	uH	Primary Inductance
VOR	125.00		125	V	Reflected Output Voltage.
Expected IO (average)			0.33	A	Expected Average Output Current
KP_VACMAX		*Info*	1.35		!!! Info. PF at high line may be less than 0.9. Decrease KP for higher PF
TON_MIN			1.91	us	Minimum on time at maximum AC input voltage
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**RM6**		**RM6**		
Bobbin		*#N/A*		*P/N:*	#N/A
AE	0.3600		0.36	cm^2	Core Effective Cross Sectional Area

LE	2.8600		2.86	cm	Core Effective Path Length
AL	2280.0		2280	nH/T^2	Ungapped Core Effective Inductance
BW	6.4		6.4	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	4.00		4		Number of Primary Layers
NS	22		22		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			127	V	Peak input voltage at VACMIN
VMAX			375	V	Peak input voltage at VACMAX
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.50		Minimum duty cycle at peak of VACMIN
IAVG			0.33	A	Average Primary Current
IP			0.42	A	Peak Primary Current (calculated at minimum input voltage VACMIN)
IRMS			0.14	A	Primary RMS Current (calculated at minimum input voltage VACMIN)
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			2450	uH	Primary Inductance
NP			128		Primary Winding Number of Turns
NB			26		Bias Winding Number of Turns
ALG			150	nH/T^2	Gapped Core Effective Inductance
BM			2244	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP			2715	Gauss	Peak Flux Density (BP<3700)
BAC			1122	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1441		Relative Permeability of Ungapped Core
LG			0.28	mm	Gap Length (Lg > 0.1 mm)
BWE			25.6	mm	Effective Bobbin Width
OD			0.20	mm	Maximum Primary Wire Diameter including insulation
INS			0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.16	mm	Bare conductor diameter
AWG			35	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			32	Cmils	Bare conductor effective area in circular mils
CMA			234	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 600)
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			2.45	A	Peak Secondary Current
ISRMS			0.72	A	Secondary RMS Current
IRIPPLE			0.65	A	Output Capacitor RMS Ripple Current
CMS			145	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			28	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.32	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.29	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
VOLTAGE STRESS PARAMETERS					
VDRAIN			628	V	Estimated Maximum Drain Voltage assuming maximum LED string voltage (Includes Effect of Leakage Inductance)

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PIVS			90	V	Output Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
PIVB			107	V	Bias Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
FINE TUNING (Enter measured values from prototype)					
V pin Resistor Fine Tuning					
RV1			4.00	M-ohms	Upper V Pin Resistor Value
RV2			1E+12	M-ohms	Lower V Pin Resistor Value
VAC1			115.0	V	Test Input Voltage Condition1
VAC2			230.0	V	Test Input Voltage Condition2
IO_VAC1			0.33	A	Measured Output Current at VAC1
IO_VAC2			0.33	A	Measured Output Current at VAC2
RV1 (new)			4.00	M-ohms	New RV1
RV2 (new)			20911.63	M-ohms	New RV2
V_OV			319.6	V	Typical AC input voltage at which OV shutdown will be triggered
V_UV			66.3	V	Typical AC input voltage beyond which power supply can startup
FB pin resistor Fine Tuning					
RFB1			158	k-ohms	Upper FB Pin Resistor Value
RFB2			1E+12	k-ohms	Lower FB Pin Resistor Value
VB1			22.5	V	Test Bias Voltage Condition1
VB2			27.5	V	Test Bias Voltage Condition2
IO1			0.33	A	Measured Output Current at Vb1
IO2			0.33	A	Measured Output Current at Vb2
RFB1 (new)			158.3	k-ohms	New RFB1
RFB2(new)			1.00E+12	k-ohms	New RFB2

Note: Actual R_{FB} = 142 kΩ due to lower bias voltage. Measured PF at 230 VAC was 0.9.

9 Performance Data

All measurements performed at room temperature.

9.1 Efficiency vs. Line and Output (LED String) Voltage

9.1.1 21 V

Hz	V_{IN} (VAC)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)	PF
60	90	7.63	21	295	6.20	81	
60	100	8.1	21.09	314	6.62	82	
60	115	8.78	21.24	340	7.22	82	0.97
60	130	9.37	21.36	362	7.73	83	
Hz	**V_{IN} (VAC)**	**P_{IN} (W)**	**V_{OUT} (V)**	**I_{OUT} (mA)**	**P_{OUT} (W)**	**Efficiency (%)**	**PF**
50	185	10.82	21.63	415	8.98	83	
50	200	11.15	21.68	426	9.24	83	
50	215	11.48	21.74	437	9.50	83	
50	230	11.8	21.79	448	9.76	83	0.9
50	245	12.11	21.83	458	10.00	83	
50	265	12.53	21.88	471	10.31	82	

9.1.2 18 V

Hz	V_{IN} (VAC)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)	PF
60	90	6.57	17.82	301	5.36	**82**	
60	100	6.95	17.91	318	5.70	**82**	
60	115	7.48	18.04	343	6.19	**83**	**0.96**
60	130	7.98	18.14	365	6.62	**83**	
Hz	**V_{IN} (VAC)**	**P_{IN} (W)**	**V_{OUT} (V)**	**I_{OUT} (mA)**	**P_{OUT} (W)**	**Efficiency (%)**	**PF**
50	185	9.27	18.42	418	7.70	**83**	
50	200	9.56	18.43	429	7.91	**83**	
50	215	9.84	18.5	440	8.14	**83**	
50	230	10.12	18.54	451	8.36	**83**	**0.88**
50	245	10.4	18.59	461	8.57	**82**	
50	265	10.76	18.64	474	8.84	**82**	

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9.1.3 24 V

Hz	V_{IN} (VAC)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)	PF
60	90	8.76	24.07	290	6.98	**80**	
60	100	9.26	24.17	309	7.47	**81**	
60	115	10.07	24.35	337	8.21	**81**	**0.97**
60	130	10.76	24.49	359	8.79	**82**	
Hz	**V_{IN} (VAC)**	**P_{IN} (W)**	**V_{OUT} (V)**	**I_{OUT} (mA)**	**P_{OUT} (W)**	**Efficiency (%)**	**PF**
50	185	12.39	24.8	412	10.22	**82**	
50	200	12.77	24.86	424	10.54	**83**	
50	215	13.14	24.92	435	10.84	**82**	
50	230	13.51	24.98	446	11.14	**82**	**0.91**
50	245	13.86	25.04	456	11.42	**82**	
50	265	14.32	25.1	468	11.75	**82**	

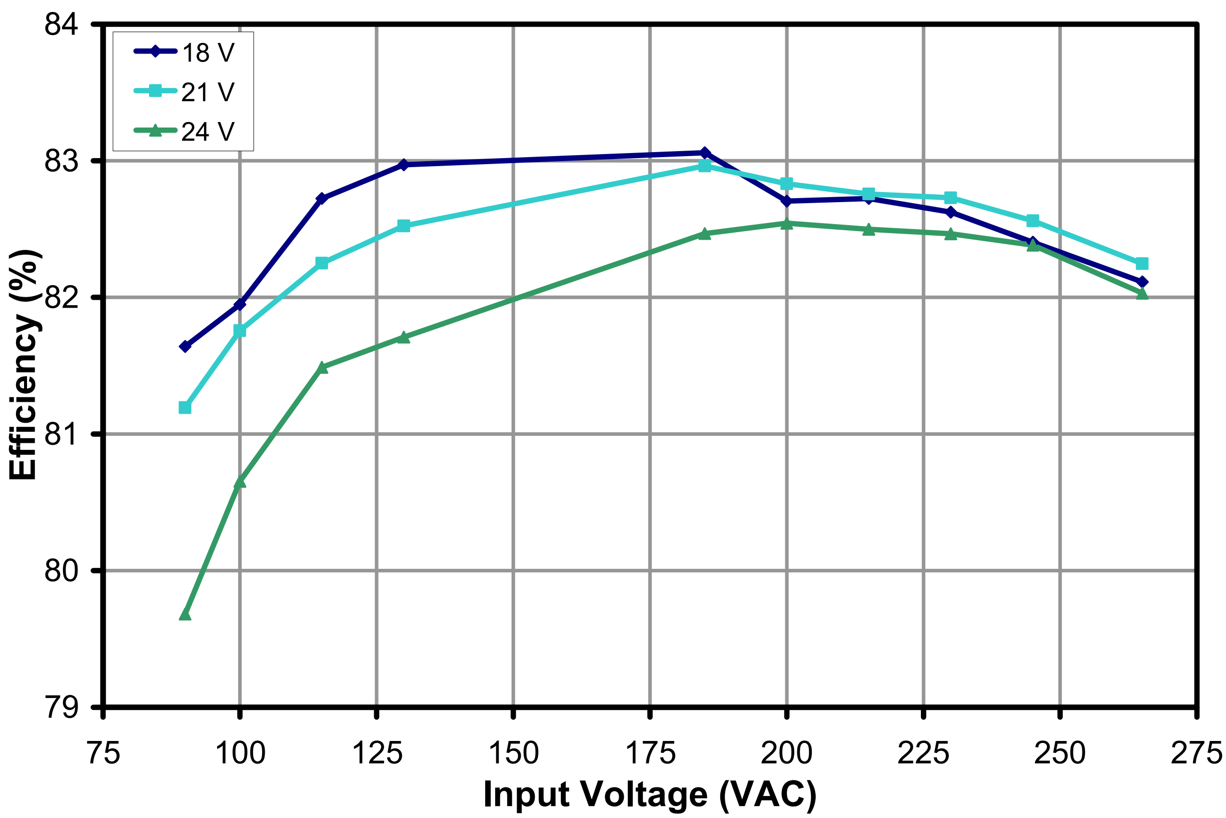

Figure 7 – Efficiency vs. Input Voltage, Room Temperature.

9.2 Regulation

9.2.1 Output Voltage and Line

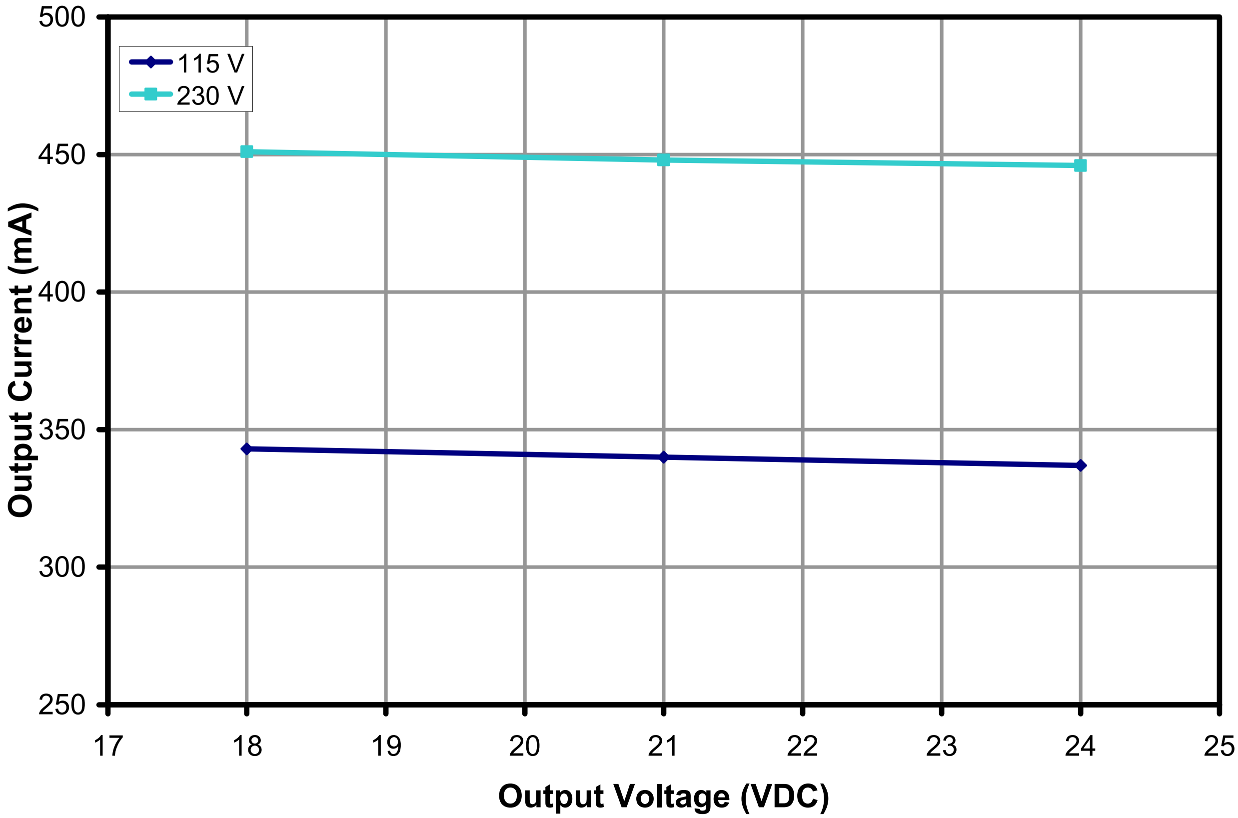

Figure 8 – Voltage and Line Regulation, Room Temperature.

The line regulation result shown above is typical for a design where the phase angle dimming mode of U1 is selected (to provide a very wide dimming range). For a given line voltage the output current can be centered by changing the value of the FEEDBACK resistor (R15). The table below shows the resistor values to adjust the mean output current at specific input voltages,

Line Voltage (VAC)	Value of R15 (kΩ)
100	133
115	143
230	182

Table 1 – Feedback Resistor Value to Center Output Current at Different Nominal Line Voltages.

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9.2.2 Line Regulation

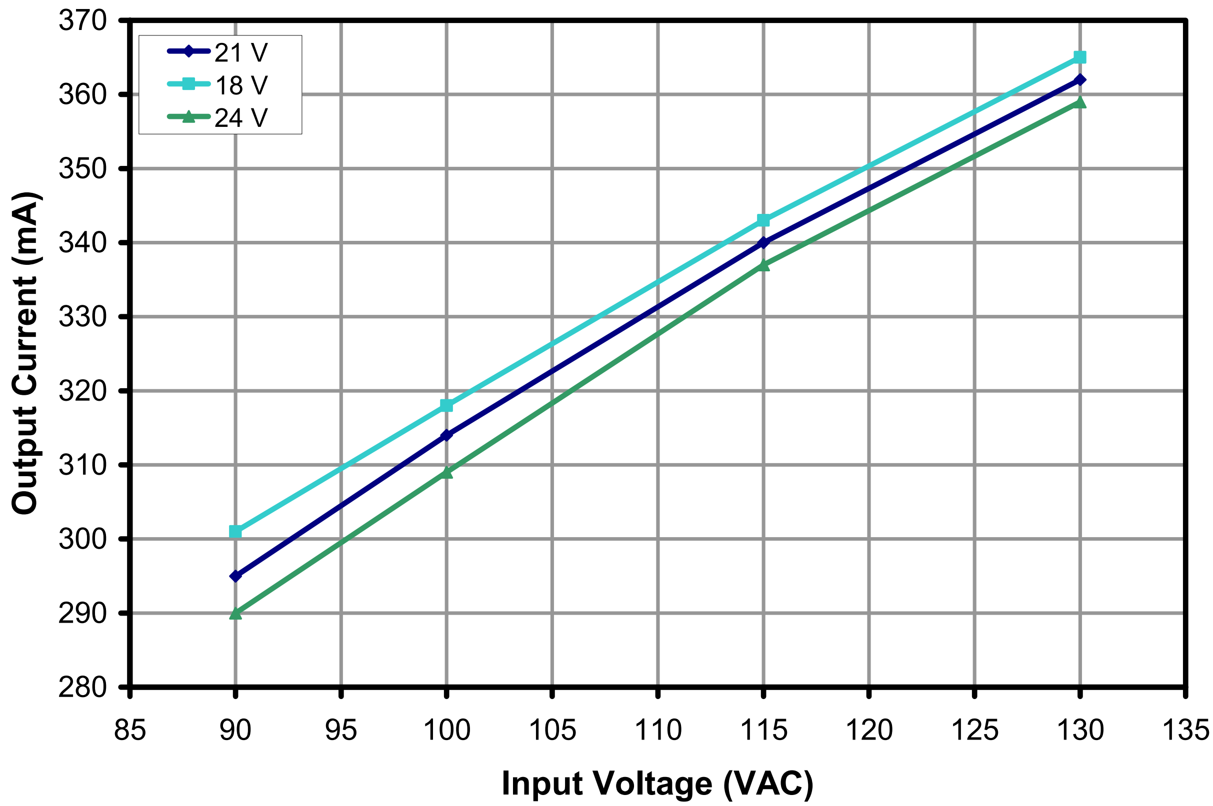

Figure 9 – Low Line Regulation, Room Temperature, Full Load.

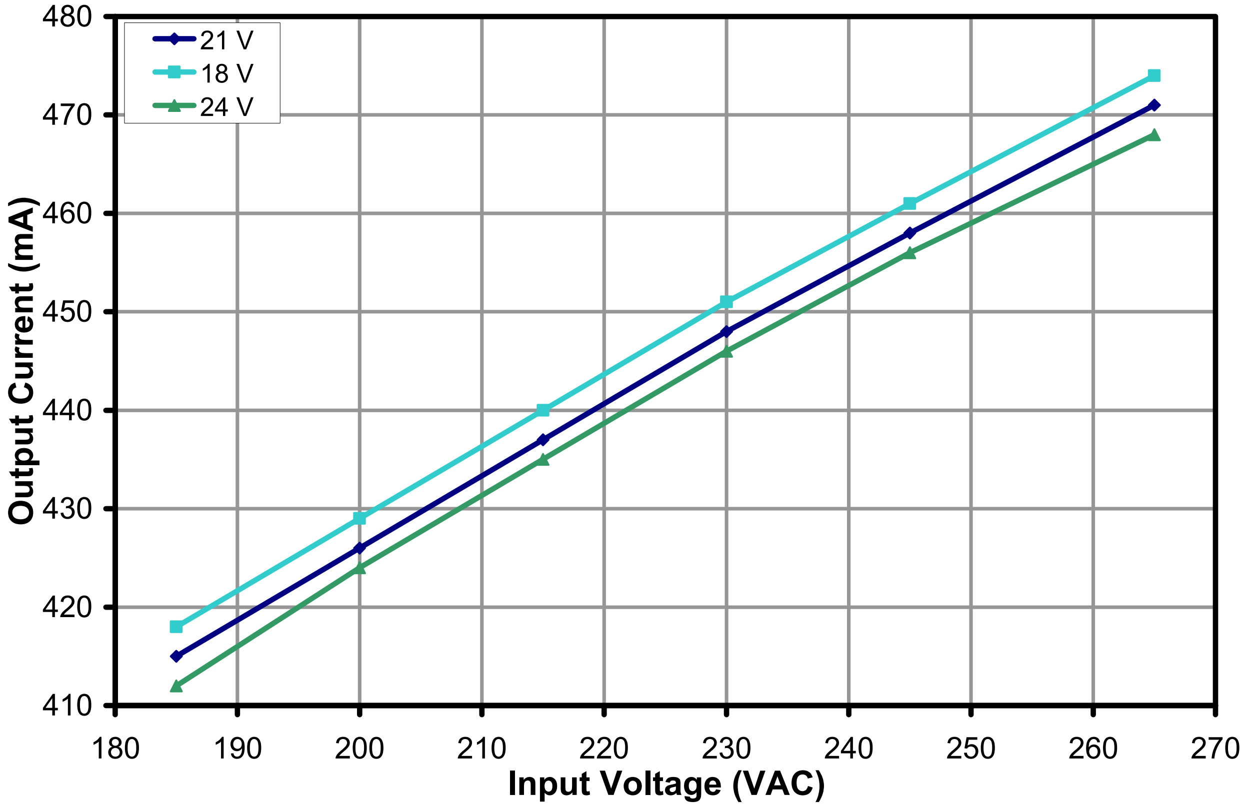

Figure 10 – High Line Regulation, Room Temperature, Full Load.

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10 Thermal Performance

Images captured after running for 30 minutes at room temperature (25 °C), full load. This indicates an operating temperature of 100°C at 50°C for the LinkSwitch-PH. The addition of a small heatsink (width of board) to the device reduces the operating temperature by ~25°C.

10.1 V_{IN} = 115 VAC

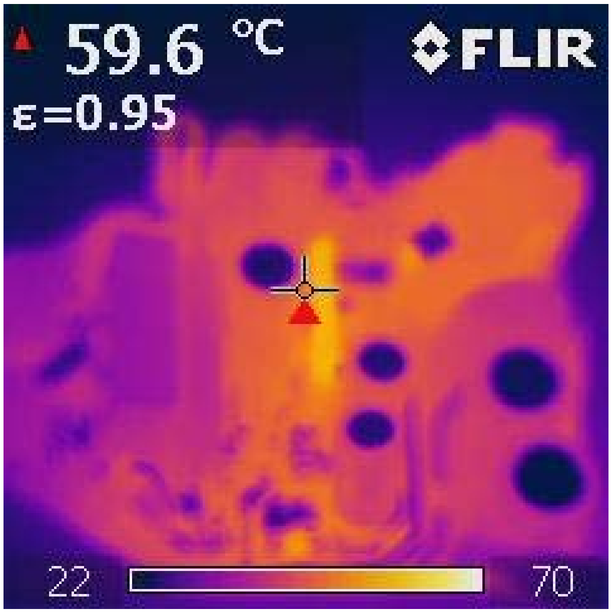

Figure 11 – Top Side.

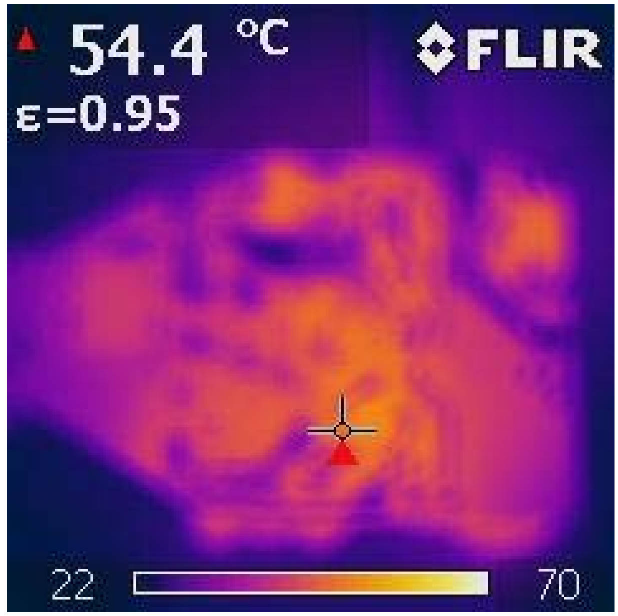

Figure 12 – Bottom Side.

10.2 V_{IN} = 230 VAC

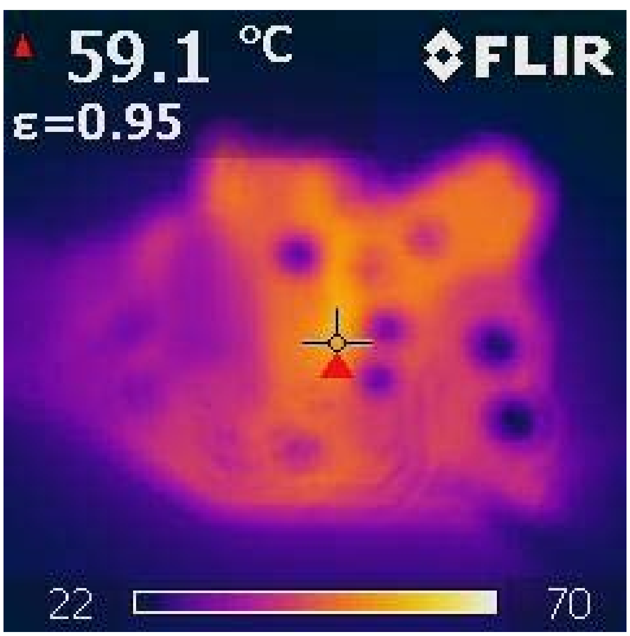

Figure 13 – Top Side.

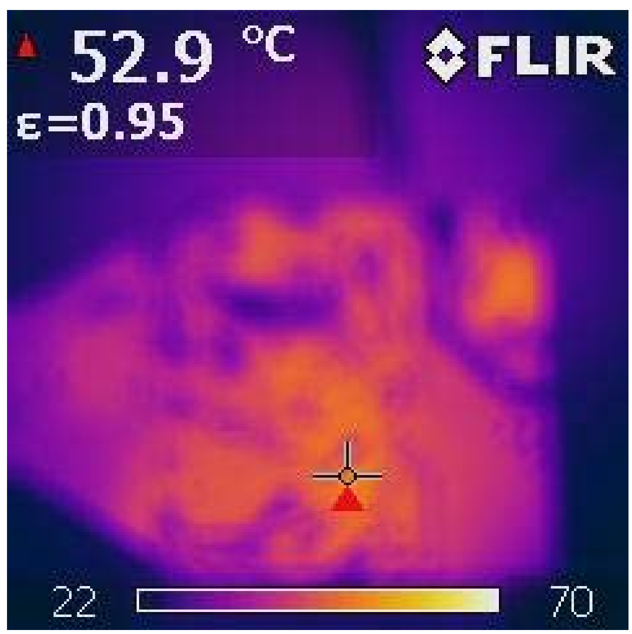

Figure 14 – Bottom Side.

11 Harmonic Data

The design passes Class C requirement.

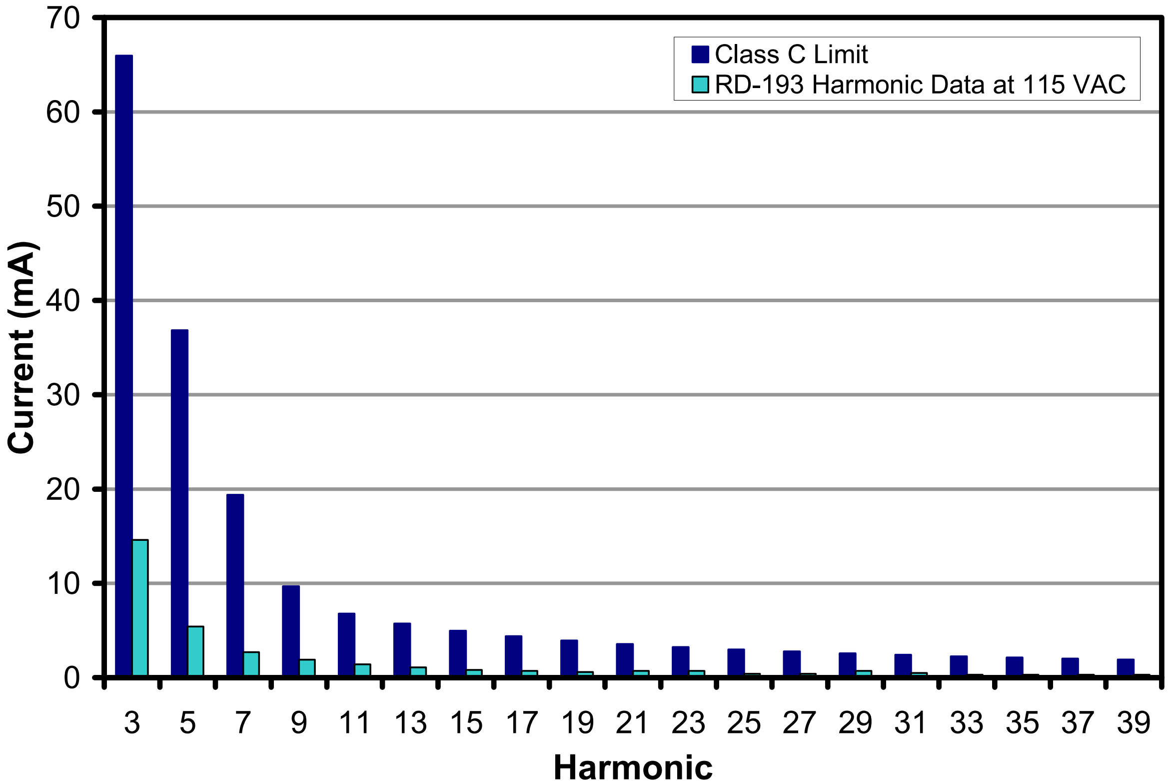

Figure 15 – 115 VAC Harmonic, Room Temperature, Full Load.

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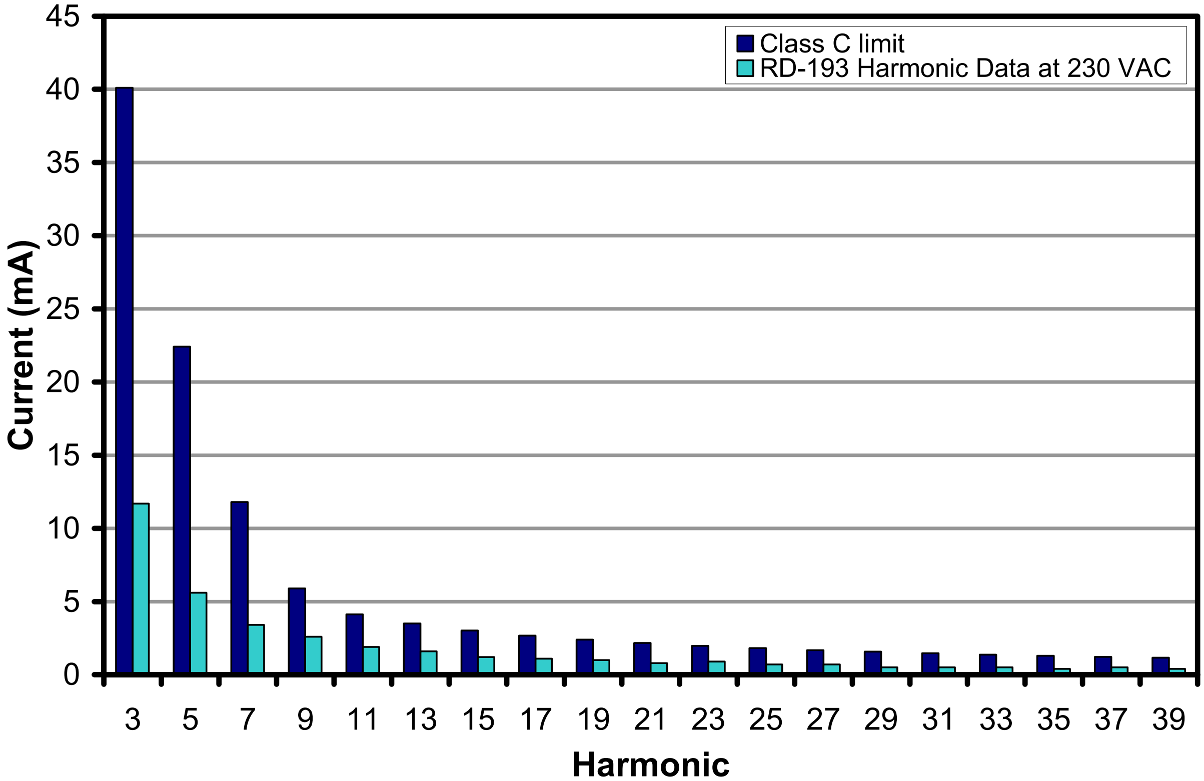

Figure 16 – 230 VAC Harmonic, Room Temperature, Full Load.

V_{IN} =115 VAC		
THD (%)	**Limit (%)**	**Margin (%)**
21.00	**33**	**12.0**
V_{IN} = 230 VAC		
THD (%)	**Limit (%)**	**Margin (%)**
27.80	**33**	**5.2**

12 Waveforms

12.1 Input Line Voltage and Current

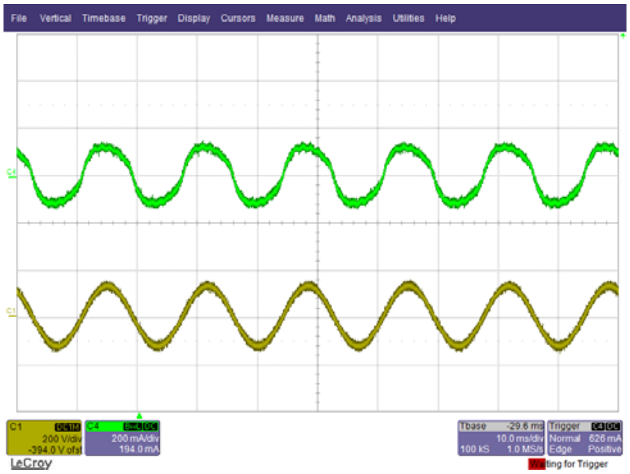

Figure 17 – 90 VAC, Full Load.
Upper: I_{IN}, 0.2 A / div.
Lower: V_{IN}, 200 V, 10 ms / div.

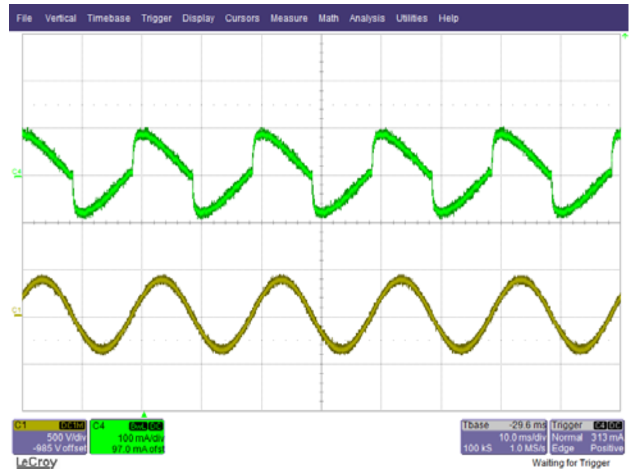

Figure 18 – 265 VAC, Full Load.
Upper: I_{IN}, 0.1 A / div.
Lower: V_{IN}, 500 V / div., 10 ms / div.

12.2 Drain Voltage and Current

Figure 19 – 90 VAC, Full Load.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 200 V, 5 μs / div.

Figure 20 – 265 VAC, Full Load.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 200 V / div., 5 μs / div.

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12.3 Output Voltage and Ripple Current

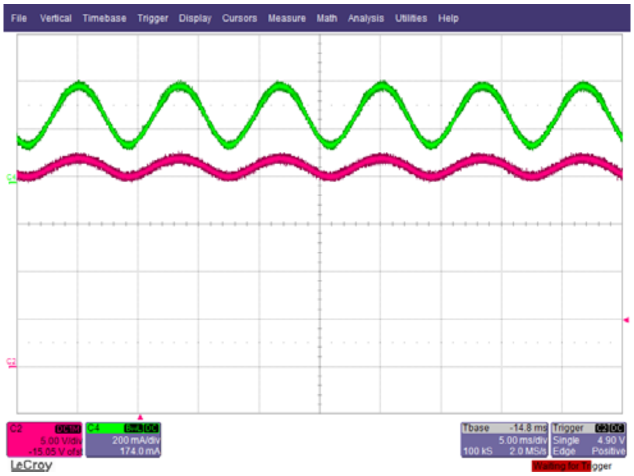

Figure 21 – 90 VAC, Full Load.
Upper: I_{RIPPLE}, 0.2 A / div.
Lower: V_{OUTPUT} 5 V, 5 ms / div.

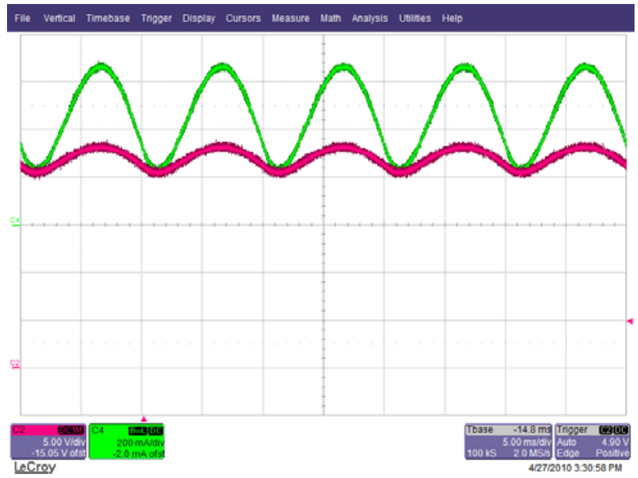

Figure 22 – 265 VAC, Full Load.
Upper: I_{RIPPLE}, 0.2 A / div.
Lower: V_{OUTPUT} 5 V, 5 ms / div.

12.4 Drain Voltage and Current Start-up Profile

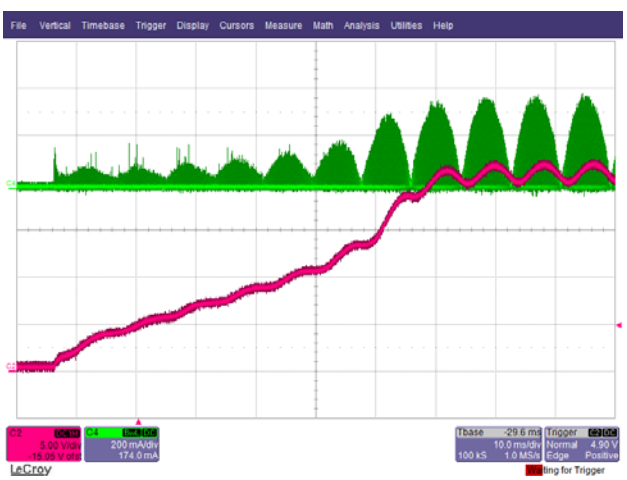

Figure 23 – 90 VAC, Full Load.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: $V_{OUTPUT,}$ 5 V, 10 ms / div.

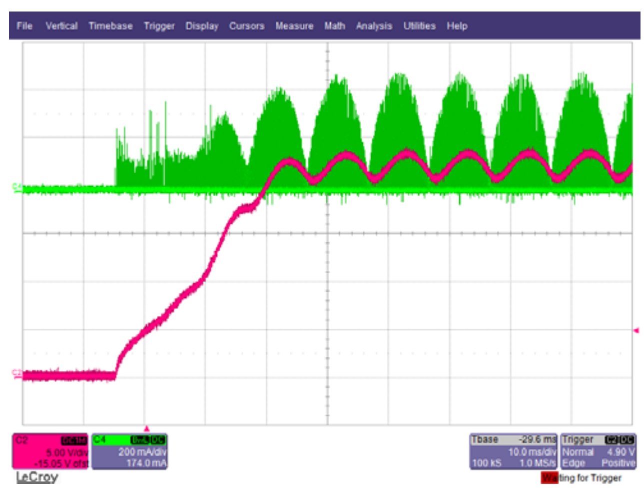

Figure 24 – 265 VAC, Full Load.
Upper: I_{RIPPLE}, 0.2 A / div.
Lower: $V_{OUTPUT,}$ 5 V, 10 ms / div.

12.5 Output Current and Drain Voltage at Shorted Output

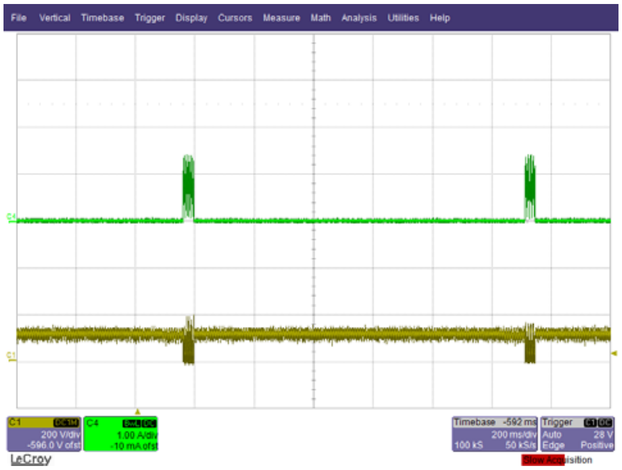

Figure 25 – 90 VAC, Full Load.
Upper: I_{OUTPUT}, 1 A / div.
Lower: $V_{DRAIN,}$ 200 V, 200 ms / div.

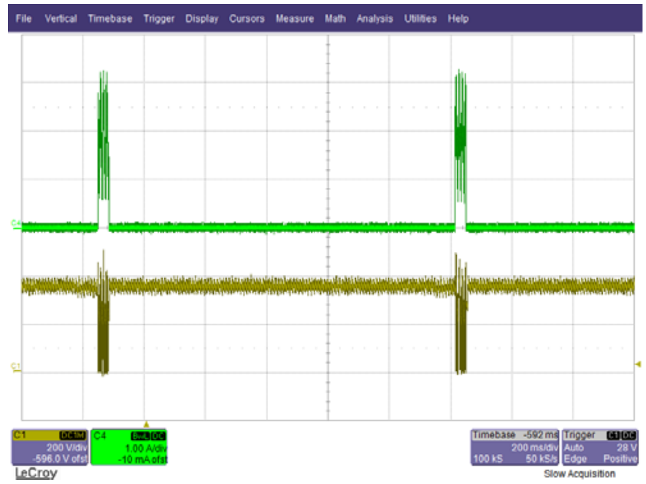

Figure 26 – 265 VAC, Full Load.
Upper: I_{OUTPUT}, 1 A / div.
Lower: $V_{DRAIN,}$ 200 V, 200 ms / div.

12.6 Open Load Output Voltage

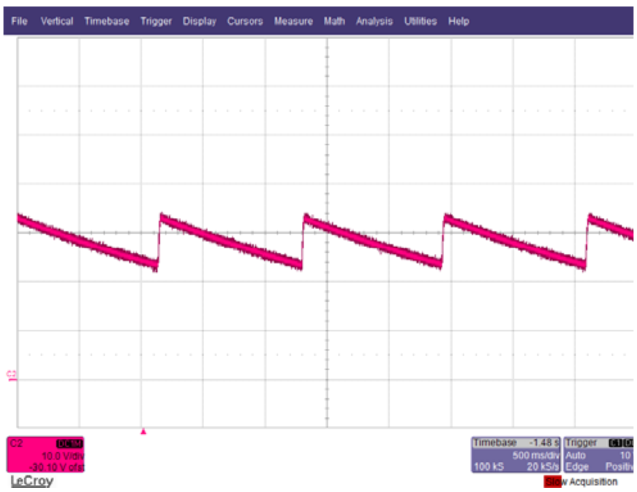

Figure 27 – Output Voltage: 115 VAC.
V_{OUT}, 10 V / div., 500 ms / div.

Figure 28 – Output Voltage: 230 VAC.
V_{OUT}, 10 V / div., 500 ms / div.

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13 Dimming

13.1 Input Phase vs. Output Current

115 VAC		230 VAC	
Phase Angle	**I_{OUT} (mA)**	**Phase Angle**	**I_{OUT} (mA)**
163	310	160	430
91	150	88	210
61	70	61	110
35	24	49	74
9	2	34	28
0	0	11	8
		0	0

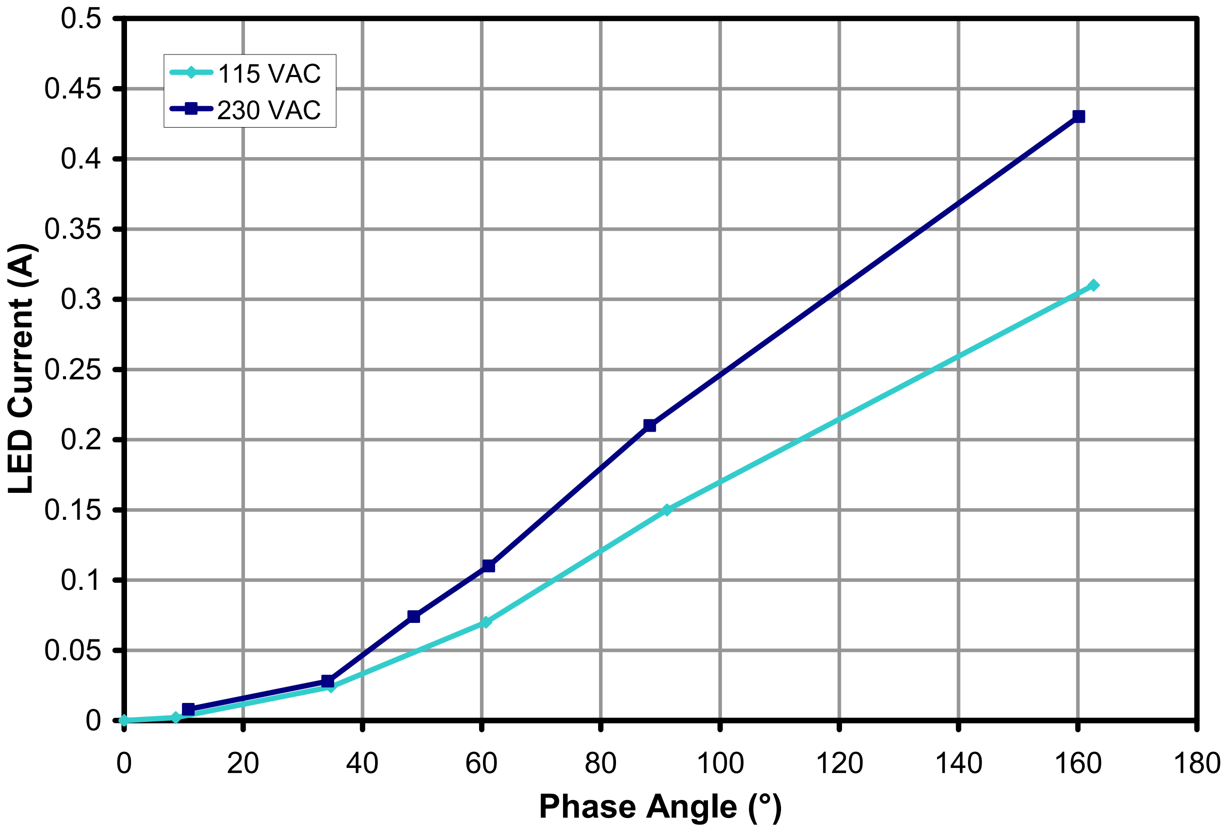

Figure 29 – Input Phase vs. Output Current.

13.2 Output Voltage and Input Current Waveforms During Dimming

13.2.1 V_{IN} = 115 VAC / 60 Hz

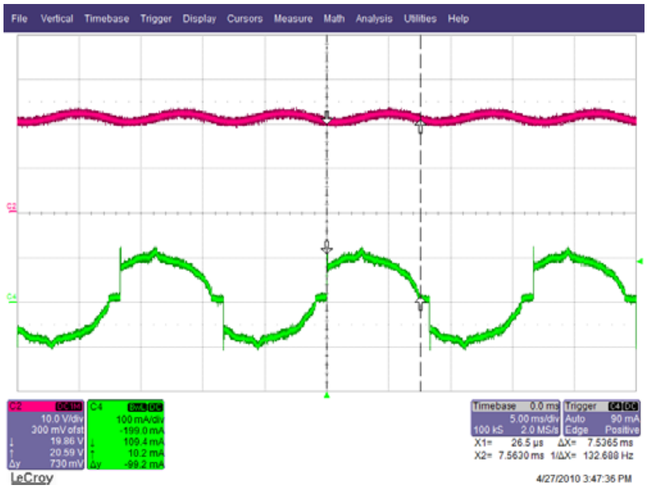

Figure 30 – 115 VAC, Full Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

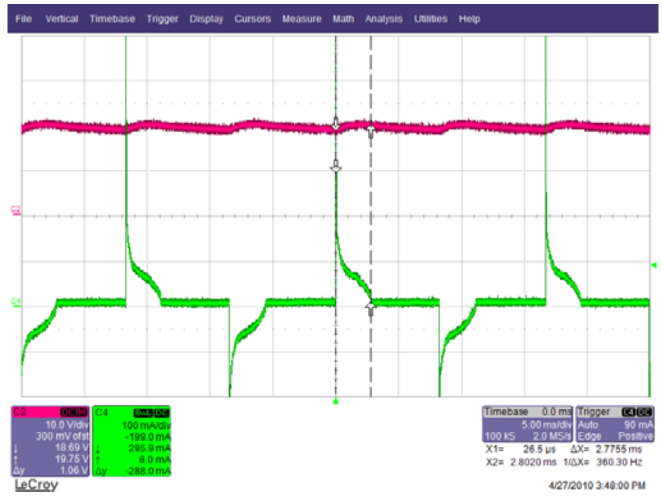

Figure 31 – 115 VAC, 60° Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

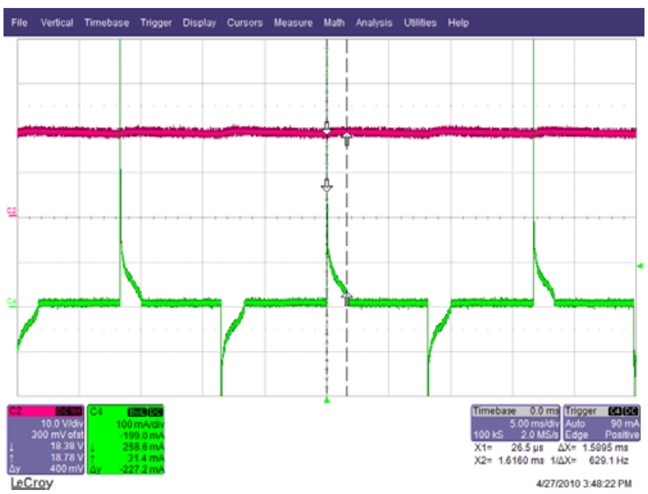

Figure 32 – 115 VAC, 35° Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

Figure 33 – 115 VAC, 8° Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

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13.2.2 V_{IN} = 230 VAC / 50 Hz

Figure 34 – 230 VAC, Full Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

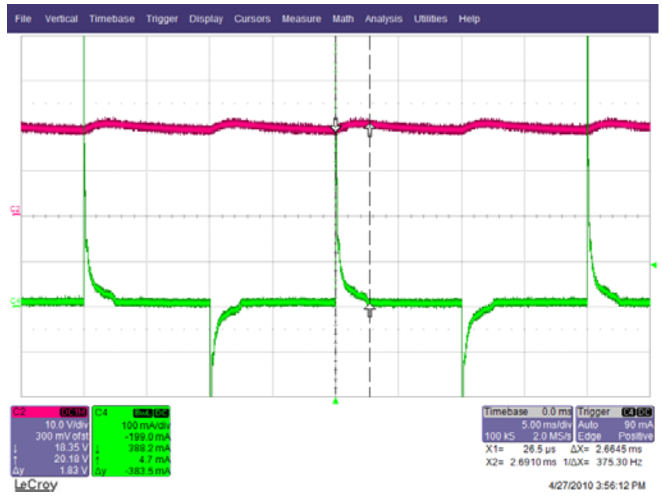

Figure 35 – 230 VAC, 49° Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

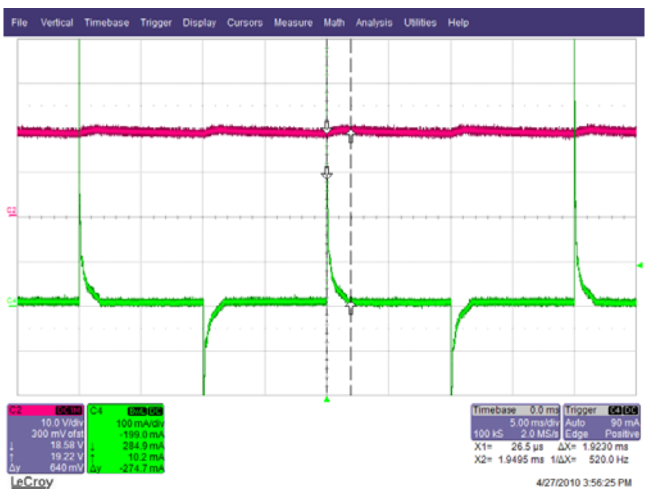

Figure 36 – 230 VAC, 34° Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

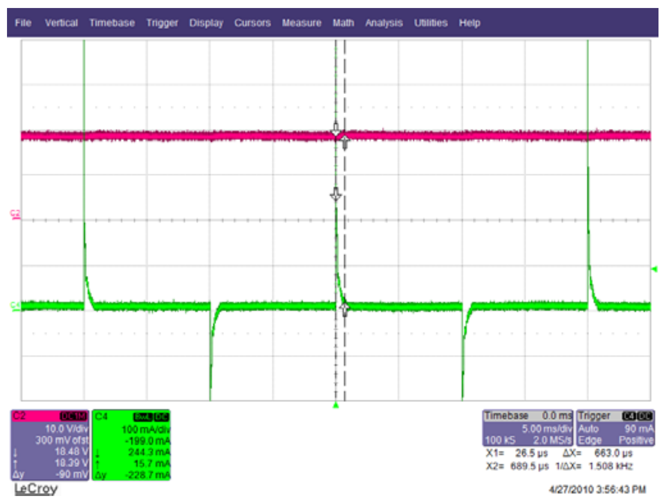

Figure 37 – 230 VAC, 12° Phase.
Upper: V_{OUT}, 10 V / div.
Lower: I_{IN}, 0.1 A / div., 5 ms / div.

14 Line Surge

Differential and common input line 200A ring wave testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
2500	230	L to N	90	Pass
2500	230	L to N	90	Pass
2500	230	L to PE	90	Pass
2500	230	L to PE	90	Pass
2500	230	N to PE	90	Pass
2500	230	N to PE	90	Pass

Unit passes under all test conditions.

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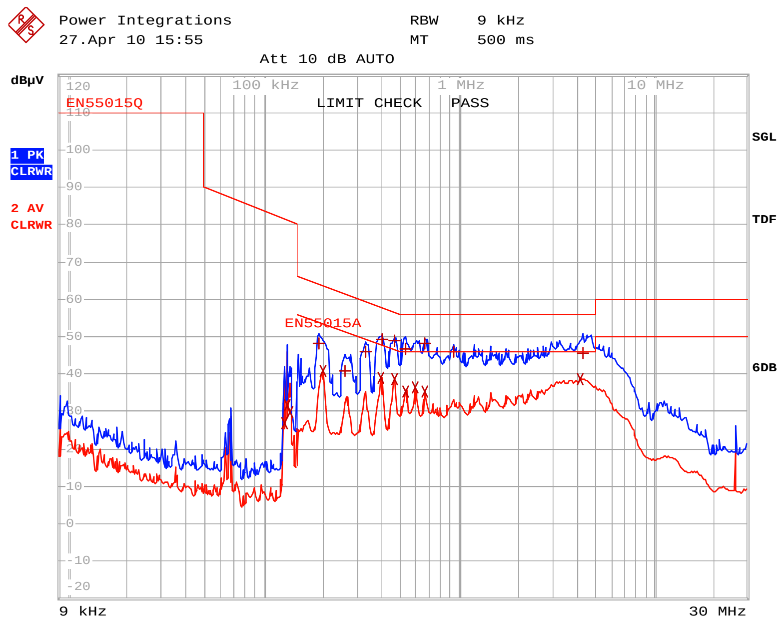
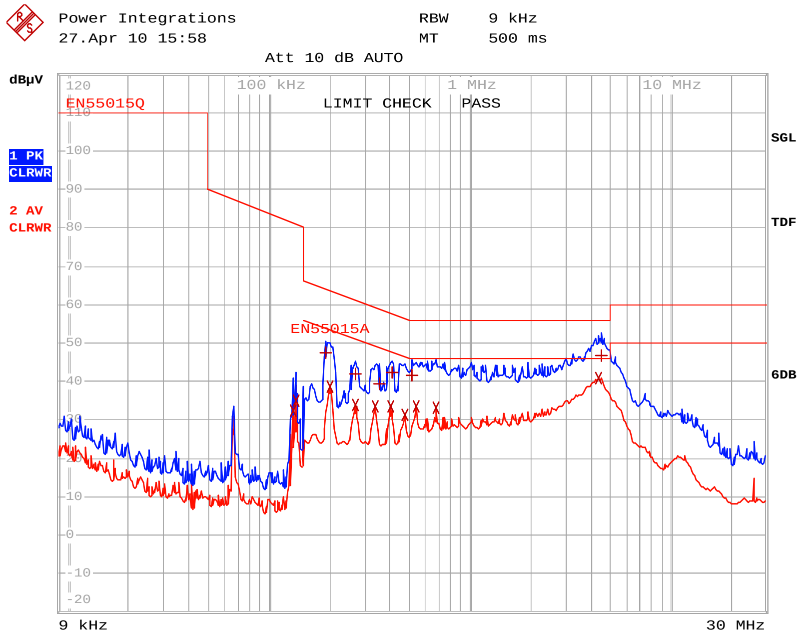
15 Conducted EMI

Note: Refer to table for margin to standard – blue line is peak measurement but limit line is quasi peak.



EDIT PEAK LIST (Final Measurement Results)				
Trace1:	EN55015Q			
Trace2:	EN55015A			
Trace3:	---			
TRACE	FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2 Average	128.247618558 kHz	26.98	N gnd	
2 Average	132.133649648 kHz	31.57	N gnd	
2 Average	136.137431366 kHz	29.83	N gnd	
1 Quasi Peak	190.46019728 kHz	48.16	L1 gnd	-15.85
2 Average	200.175581485 kHz	40.71	N gnd	-12.89
1 Quasi Peak	261.871472881 kHz	40.66	N gnd	-20.70
1 Quasi Peak	332.507282579 kHz	45.95	L1 gnd	-13.43
2 Average	397.727746704 kHz	38.88	L1 gnd	-9.01
1 Quasi Peak	401.705024172 kHz	49.29	L1 gnd	-8.52
1 Quasi Peak	466.367062279 kHz	48.81	N gnd	-7.76
2 Average	466.367062279 kHz	38.69	N gnd	-7.88
1 Quasi Peak	530.769219795 kHz	46.57	L1 gnd	-9.42
2 Average	530.769219795 kHz	35.42	L1 gnd	-10.57
2 Average	598.084042089 kHz	36.37	L1 gnd	-9.62
1 Quasi Peak	667.263434405 kHz	48.01	N gnd	-7.98
2 Average	667.263434405 kHz	35.42	N gnd	-10.57
1 Quasi Peak	935.888336808 kHz	45.80	L1 gnd	-10.19
2 Average	4.16322710559 MHz	38.65	N gnd	-7.34
1 Quasi Peak	4.33227082061 MHz	45.55	N gnd	-10.44

Figure 38 – Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55015 B Limits.



EDIT PEAK LIST (Final Measurement Results)			
Trace1:	EN55015Q		
Trace2:	EN55015A		
Trace3:	---		
TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2 Average	130.825395691 kHz	32.43 N gnd	
2 Average	136.137431366 kHz	34.96 L1 gnd	
1 Quasi Peak	192.364799253 kHz	47.32 L1 gnd	-16.60
2 Average	202.1773373 kHz	38.56 N gnd	-14.95
1 Quasi Peak	267.135089486 kHz	41.78 N gnd	-19.42
2 Average	269.806440381 kHz	34.00 N gnd	-17.11
2 Average	335.832355405 kHz	33.36 L1 gnd	-15.94
1 Quasi Peak	352.963180679 kHz	39.19 L1 gnd	-19.69
2 Average	405.722074413 kHz	33.60 N gnd	-14.13
1 Quasi Peak	409.779295157 kHz	42.10 N gnd	-15.54
2 Average	471.030732902 kHz	31.24 L1 gnd	-15.25
1 Quasi Peak	515.159375557 kHz	41.49 N gnd	-14.50
2 Average	541.437681113 kHz	33.55 N gnd	-12.44
2 Average	673.936068749 kHz	32.91 L1 gnd	-13.08
2 Average	4.37559352882 MHz	40.83 N gnd	-5.16
1 Quasi Peak	4.55326017222 MHz	46.83 N gnd	-9.16

Figure 39 – Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55015 B Limits.

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16 Production Distribution Data

Each RD-193 board is ATE tested and the data recorded prior to shipping. The distribution data for output current is presented below for a fixed line condition of 115 VAC and a device junction temperature of 50°C. This shows very low unit to unit variation (sigma of 3.3 mA) which includes both the device and external component influences.

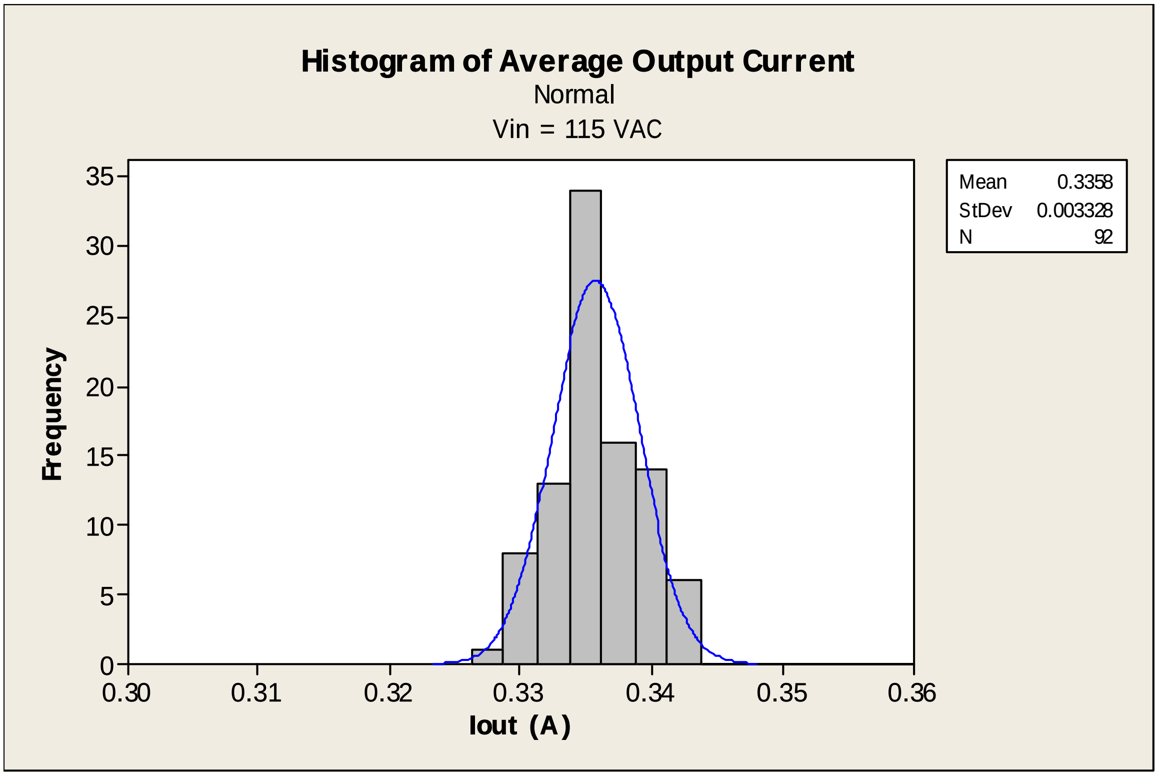

Figure 40 – Production Variation of I_{OUT} at 115 VAC.

17 Revision History

Date	Author	Revision	Description & changes	Reviewed
09-Jun-10	DK	1.0	Initial Release	Apps and Mktg

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18 Appendix

18.1 Dimming Test with TRIAC Dimmer Switches

18.1.1 115 VAC Input, 60 Hz

Style	Country	Manufacturer	Model number	Dimming Test Data		
				Max Current (mA)	Controlled Min. Current (mA)	Min. Current without Off Switch (mA)
Rotary						
1	Taiwan		WS-5005	325	3	0
2	USA	Leviton	OB4911	324	16	0
Slider						
1	USA	Lutron	GLR11-F38875	288	14	0
2	Taiwan	SG Electric	XH004186	310	2	0

18.1.2 230 VAC Input, 50 Hz

Style	Country	Manufacturer	Model Number	Dimming Test Data		
				Max. Current (mA)	Controlled Min. Current (mA)	Min. Current without Off Switch (mA)
Rotary						
1	Taiwan		Y-25088A	440	2	0
2	Taiwan		Y-25082A	439	2	0
3	Taiwan		D-2160B	442		30
4	China	CLIPMEI		440	5	0
5	China	MBR		440		92
6	China	KBE		438	7	0
7	China	MANK	NK/TG100001	441		120
8	China	SB Electric	BM2	426	2	0
9	China	EBAHuang		440	1	0
10	China	Myongbo		444		100
11	China	TCL	L2.0	438		48
12	Italy	RTS34DLI		444		53

18.2 Audible Noise Test Data

Unit measured open frame with calibrated laboratory microphone placed 25 mm above the transformer.

Results show very acceptable audible noise levels created by supply when using leading edge phase angle dimming. Levels measured were only slightly above noise floor.

18.2.1 V_{IN} = 115 VAC, Full Phase

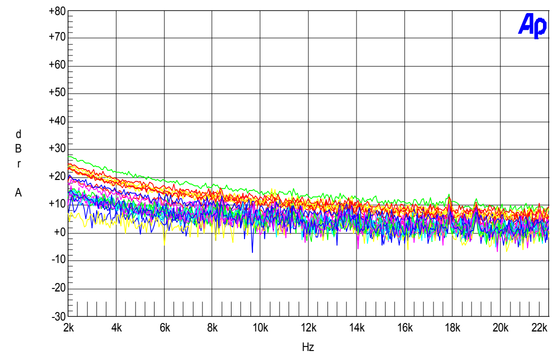

Figure 41 – 2 kHz – 22 kHz.

18.2.2 V_{IN} = 115 VAC, Half Phase

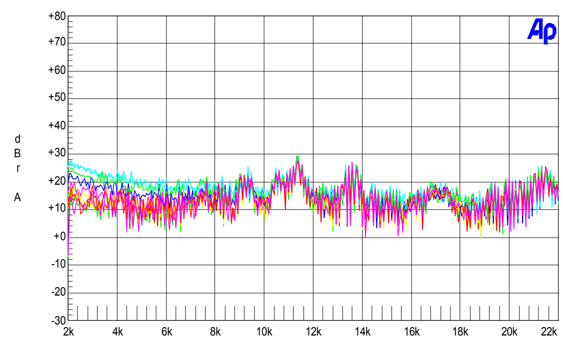

Figure 42 – 2 kHz – 22 kHz.

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18.2.3 V_{IN} = 230 VAC, Full Phase

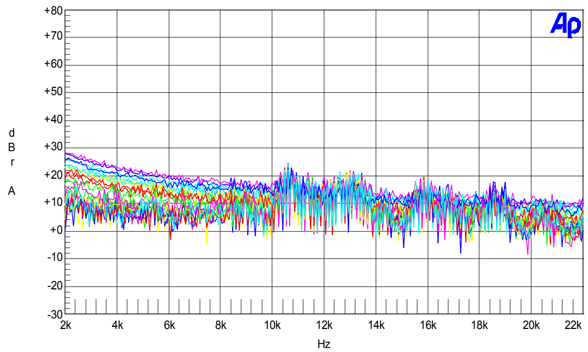

Figure 43 – 2 kHz – 22 kHz.

18.2.4 V_{IN} = 230 VAC, Half Phase

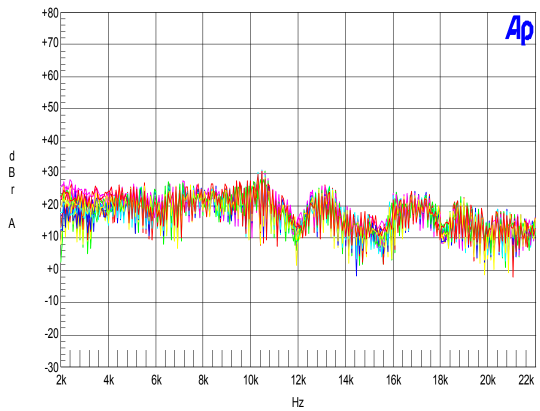

Figure 44 – 2 kHz – 22 kHz.

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The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.powerint.com/ip.htm.

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