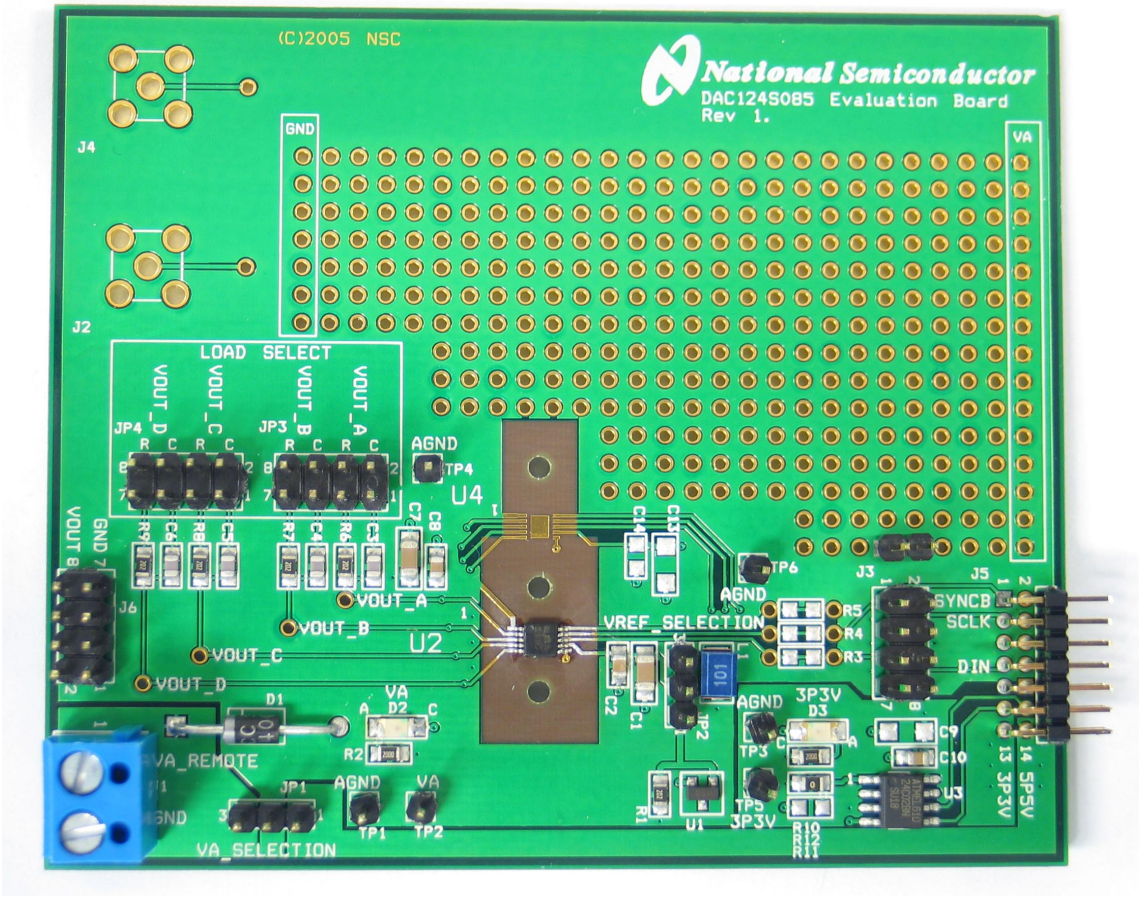
National Semiconductor

September 19, 2006
Rev -1.1
PEL

Evaluation Board User's Guide

DAC124S085 12-Bit Quad, DAC104S085 10-Bit Quad, DAC084S085 8-Bit Quad, DAC122S085 12-Bit Dual, DAC102S085 10-Bit Dual, DAC082S085 8-Bit Dual

Micro Power Digital-to-Analog Converter with Rail-to-Rail Output



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1.0 Introduction

The DAC124S085EB Design Kit (consisting of the DAC124S085 Evaluation Board and this User's Guide) is designed to ease evaluation and design-in of the National Semiconductor DAC124S085 12-Bit Quad, DAC104S085 10-Bit Quad, DAC084S085 8-Bit Quad, DAC122S085 12-Bit Dual, DAC102S085 10-Bit Dual, DAC082S085 8-Bit Dual Micro-Power Digital-to-Analog Converter with Rail-to-Rail Output. This family of pin-compatible DACs, will be referenced throughout this document as the DAC124S085.

The evaluation board can be used with suitable test equipment, such as a pattern generator and signal analyzer, to evaluate the DAC124S085 performance.

Data transmitted to the DAC124S085 via a serial interface is converted to an analog waveform by U2/U4, the DAC124S085.

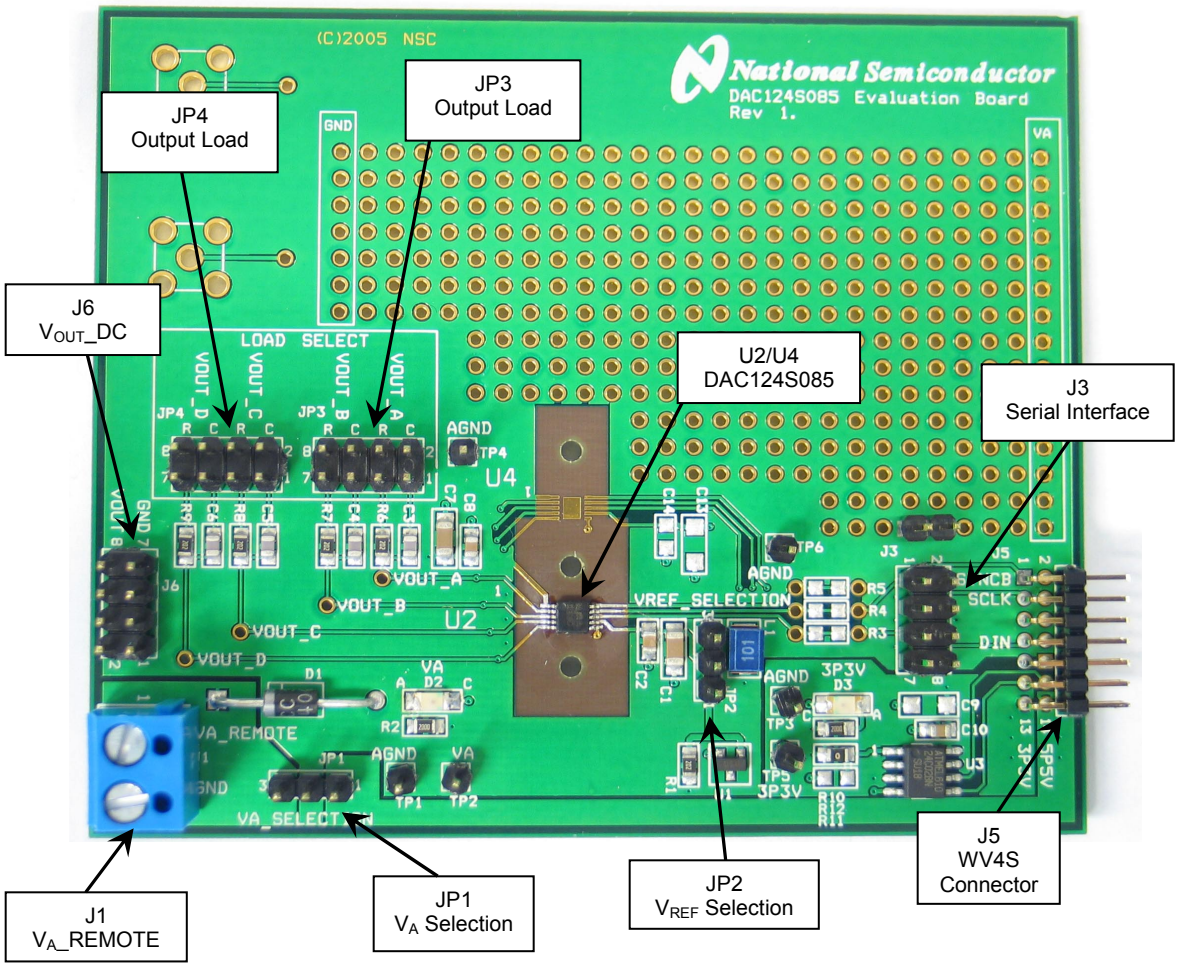


Figure 1: Component and Test Point Location

2.0 Board Assembly

The DAC124S085 evaluation board comes fully assembled and ready for use. Refer to the Bill of Materials for a description of components, to *Figure 1* for major component placement, and to *Figure 6* for the Evaluation Board schematic.

3.0 Quick Start

The DAC124S085 evaluation board may be used in the Stand-Alone mode while a Pattern Generator is used to drive the DAC124S085, and a Signal Analyzer is used to evaluate the analog output signal

3.1 Stand-Alone Mode

Refer to *Figure 1* for locations of test points and major components.

1. Connect a clean analog (not switching) +5V power source to Power Connector J1 on the DAC124S085 board and turn on the power. Place a jumper across pins 2 and 3 of JP1 to select VA_REMOTE.
2. Place a jumper across the appropriate pins of JP2 to select the desired reference voltage. For the default selection of V_{REF} = VA, place a jumper across pins 2 & 3. Please see *Table 1* for details.
3. Create the digital waveforms seen in *Figure 2* with your Pattern Generator. Ensure that SCLK doesn't exceed 40MHz. Refer to "Section 1.4: Serial Interface" and the DAC124S085 Datasheet for further details.

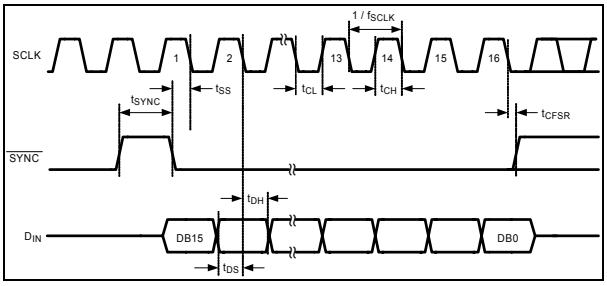


Figure 2: Digital Input Timing Diagram
(*Refer to Appendix 2.0 for an enlarged version*)

4. Connect your Pattern Generator to Serial Interface header J3. Refer to *Figure 3* below for connection details.

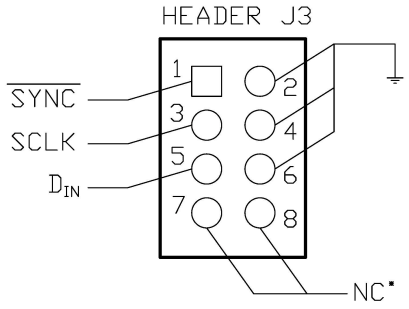


Figure 3: J3 Serial Interface Header
(*Pins 7&8 are used for SCL and SDA, respectively, when modified for WV4.0)

5. The Analog Output signals of each channel can be seen DC coupled at header J6. See the header schematic of *Figure 4* for details.

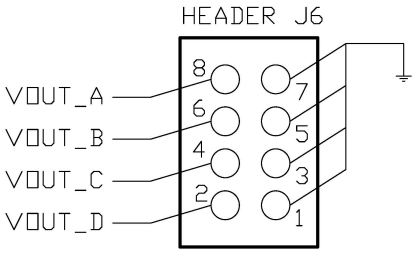


Figure 4: J6 Output Header

6. Select the desired output load by adding jumpers to headers JP3 & JP4. See *Figure 5* and *Table 1* in Section 4.0 for jumper configurations.

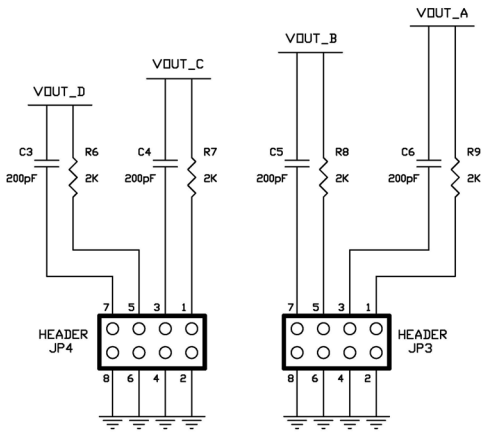


Figure 5: JP3 & JP4 Load Select Headers

4.0 Functional Description

Table 1 describes the function of the various jumpers on the DAC124S085 evaluation board. The Evaluation Board schematic is shown in *Figure 6*.

Jumper	Pins 1 & 2	Pins 2 & 3
JP1	Select VA=5.5V from WV4.1 Board	Select VA_REMOTE from J1
JP2	Select 2.5V as V_{REF}	Select VA as V_{REF}

Pin	JP3	JP4
1 & 2	Select 200pF Output Load Capacitance VOUT_A	Select 200pF Output Load Capacitance VOUT_C
3 & 4	Select 2kΩ Output Load Resistance VOUT_A	Select 2kΩ Output Load Resistance VOUT_C
5 & 6	Select 200pF Output Load Capacitance VOUT_B	Select 200pF Output Load Capacitance VOUT_D
7 & 8	Select 2kΩ Output Load Resistance VOUT_B	Select 2kΩ Output Load Resistance VOUT_D

Table 1: Jumper Configurations

4.1 Serial Interface

In Stand-Alone Mode, the serial interface must be driven by an external device. The three-wire interface (SCLK, SYNC, D_{IN}) is compatible with SPI, QSPI and MICROWIRE, as well as most DSPs. See the Timing Diagram (*Figure 2*) for information on a write sequence.

The maximum digital input level of the three-wire interface is independent of the analog supply voltage (V_A). The range of all digital inputs is 0V to 5.25V regardless of V_A.

A write sequence begins by bringing the SYNC line low. Once SYNC is low, the *Binary* data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. On the 16th falling clock edge, the last data bit is clocked in and the programmed function (a change in the mode of operation and/or a change in the DAC register contents) is executed. At this point the SYNC line may be kept low or brought high. In either case, it must be brought high for the minimum specified time before the next write sequence as a falling edge of SYNC will initiate the next write cycle.

Since the SYNC and D_{IN} buffers draw more current when they are high, they should be idled low between write sequences to minimize power consumption.

Please refer to the DAC124S085 datasheet for more information.

4.2 DAC Reference Circuitry

The reference voltage for the DAC124S085 is selected by JP2. (See Table 1 for details.) The reference can either be selected as a fixed 2.5 volts, or as the supply voltage. In the latter case, the analog output range of the DAC124S085 can be scaled by adjusting the supply voltage (V_A). This voltage can be set anywhere from +2.7V to +5.5V.

4.3 Analog Output

The analog output of this Eval board is available DC coupled at the header J6. An AC coupled output is not provided, however SMA footprints are available at J2 and J4. These footprints can be used along with the prototype field to design another output circuit, should it be desired.

4.4 Power Supply Connections

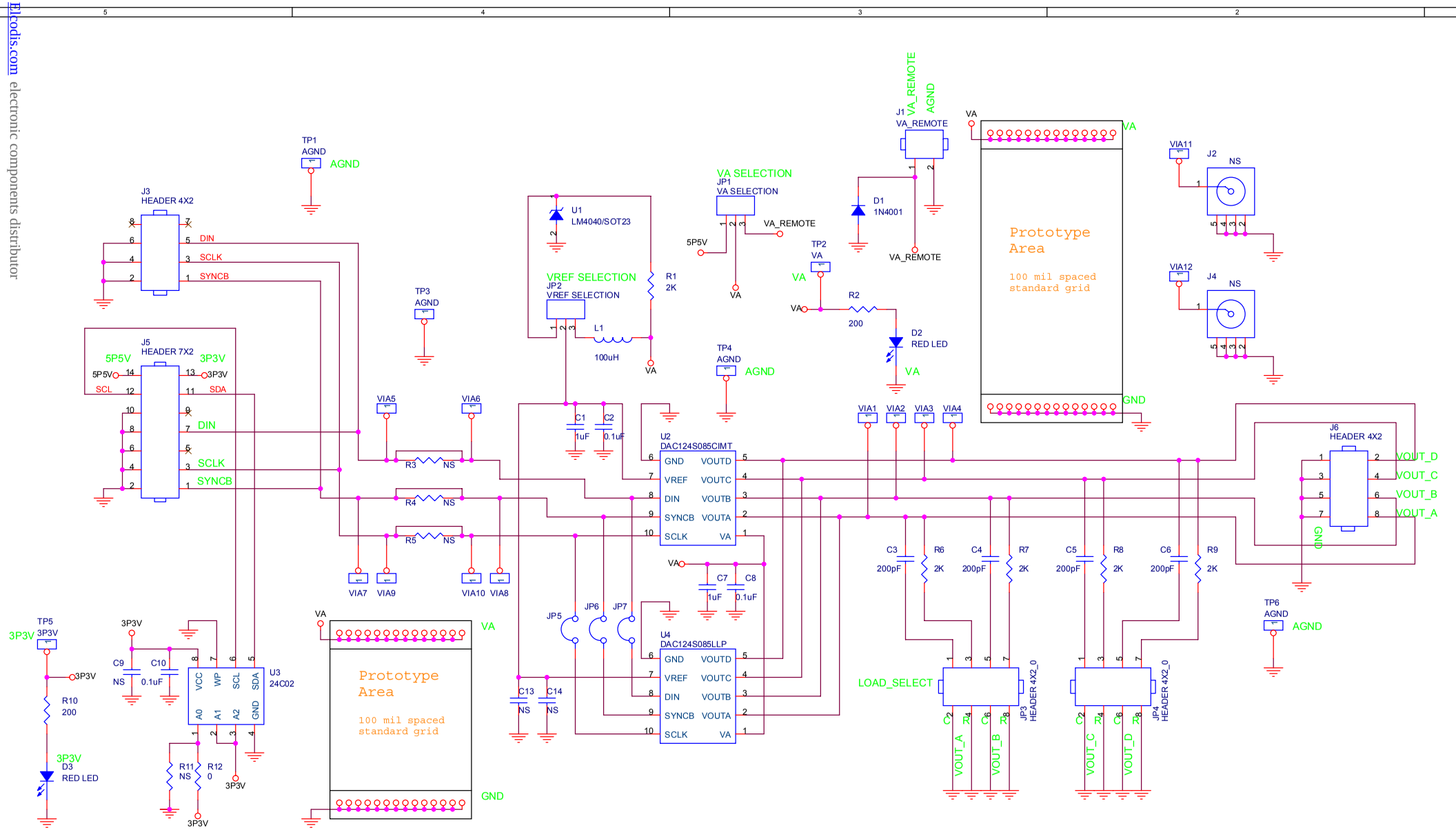
In Stand-alone mode, the DAC124S085 board must be powered by an external supply.

Connect a DC voltage supply to connector J1 and place a jumper across pins 2 and 3 of JP1 to select V_A_REMOTE. This voltage (V_A) can be set anywhere from +2.7V to +5.5V.

If the supply voltage (V_A) serves as the reference for the DAC124S085, ensure a clean power supply is used.

6.0 Evaluation Board Specifications

Board Size:	3.70" x 3.15" (9.4 cm x 8 cm)	
Power Requirements	Min: +2.7V , 3mA	Max: +5.5V, 5 mA
Max Clock Frequency:	40 MHz	
Analog Output		
Impedance:	User Selectable: 2KΩ, 200pF, or ∞.	



t Notes:

text in green should appear on the board as Top Silkscreen.

DAC124S085_BOM

7/31/06

870012729-100A Revision: 1.1 CS

Bill Of Materials August 1, 2006

Item	Quantity	Reference	Description	Value	Rating	Package	Manufacturer	Manufacturer P/N	Source	Source P/N
1	2	C7,C1	CAP	1uF	50V	1206	TDK	C3216X7R1H105K	Digikey	445-1423-2-ND
2	1	C14		NS	10V	0805	NS	NS		NS
3	3	C2,C8,C10	CAP	0.1uF	50V	0805	Panasonic	ECJ-2YB1H104K	Digikey	PCC1840TR-ND
4	4	C3,C4,C5,C6	CAP	200pF	100V	0805	Murata	GRM2165C2A201JA01D	Digikey	490-1606-1-ND
5	2	C13,C9		NS		sm/c_1206	NS	NS		NS
6	1	D1	Dio	1N4001	50V	DAX2/DO41	Micro Comm	1N4001-TP	Digikey	1N4001-TPMSTR-ND
7	2	D3,D2	LED	RED LED	2.1V	1206	Avago Tech	HSMS-C150	Digikey	516-1440-1-ND
8	1	JP1	Hdr	Hdr 1x3		.100 Singl Str 36 Pos.	Sullins Elect	PBC36SAAN	Digikey	S1011E-36-ND
9	1	JP2	Hdr	Hdr 1x3		.100 Singl Str 36 Pos.	Sullins Elect	PBC36SAAN	Digikey	S1011E-36-ND
10	2	JP3, JP4	Hdr	Hdr 2x4		.100 dual str 60 Pos	Sullins Elect	PBC30DADN	Digikey	S2041E-30-ND
11	1	J1	Term	term block 2 Pos		term block 2 Pos	On Shore Tech	ED120/2DS	Digikey	ED1609-ND
12	2	J2,J4	NS	SMA-5		rf/sma/v_clr	NS	NS		NS
13	2	J3, J6	HDR	Hdr 2x4		.100 dual str 60 Pos	Sullins Elect	PBC30DADN	Digikey	S2041E-30-ND
14	1	J5	HDR	Hdr 2X7		rt angle hdr	Sullins Elect	PRPN212PARN-RC	Digikey	S5803-21-ND
15	1	L1	IND	100uH	100mA	1210	TDK Corp	NLCV32T-101K-PF	Digikey	445-1543-1-ND
16	5	R1,R6,R7,R8,R9	RES	2K	5%	0805	Panasonic	ERJ-6GEYJ202V	Digikey	P2.0KATR-ND
17	2	R10,R2	RES	200	1%	0805	Panasonic	ERJ-6ENF2000V		P200CTR-ND
18	4	R3,R4,R5,R11		NS		sm/r_0805	NS	NS		NS
19	1	R12	RES	0.0	5%	0805	ROHM	MCR1-0EZHJ000	Digikey	RHM0.0ATR-ND
20	4	TP1,TP3,TP4,TP6	HDR	Hdr 1X1		.100 Singl Str 36 Pos.	Sullins Elect	PBC36SAAN	Digikey	S1011E-36-ND
21	1	TP2	HDR	Hdr 1X1		.100 Singl Str 36 Pos.	Sullins Elect	PBC36SAAN	Digikey	S1011E-36-ND
22	1	TP5	HDR	Hdr 1X1		.100 Singl Str 36 Pos.	Sullins Elect	PBC36SAAN	Digikey	S1011E-36-ND
23	1	U1	REF	LM4040/SOT23		SOT23	National Semi	LM4040DIM3-2.5	Digikey	LM4040DIM3-2.5TR
24	1	U2	IC	DAC124S085CIMT		socket	National Semi	DAC124S085CIMT		National Semi
25	1	U3	IC	24C02	1.8 - 5.5V	8- SOIC	ATMEL	AT24C02BN-10SU-1.8	Digikey	AT24C02BN-10SU-1.8-ND
26	1	U4	IC	DAC124S085LLP		LLP	National Semi	DAC124S085LLP		National Semi
27	10	-	SHUNT	Hdr Jumper		Hdr Jumper	Sullins Elect	SPC02SYAN	Digikey	S9001-ND
28	1	-		Blank PC Board-						
				Immersion Gold						

APPENDIX

A1.0 Summary Tables of Test Points, Jumpers, and Connectors

Test Points on the DAC124S085 Evaluation Board

TP1: AGND	Ground. Located at the lower left of the board.
TP2: VA	V_A Test Point. Located in the lower left of the board.
TP3: AGND	Ground. Located at the lower right of the board.
TP4: AGND	Ground. Located in the center of the board
TP5: 3P3V	3.3V test point. Located at the lower right edge of the board.
TP6: AGND	Ground. Located in the center of the board.

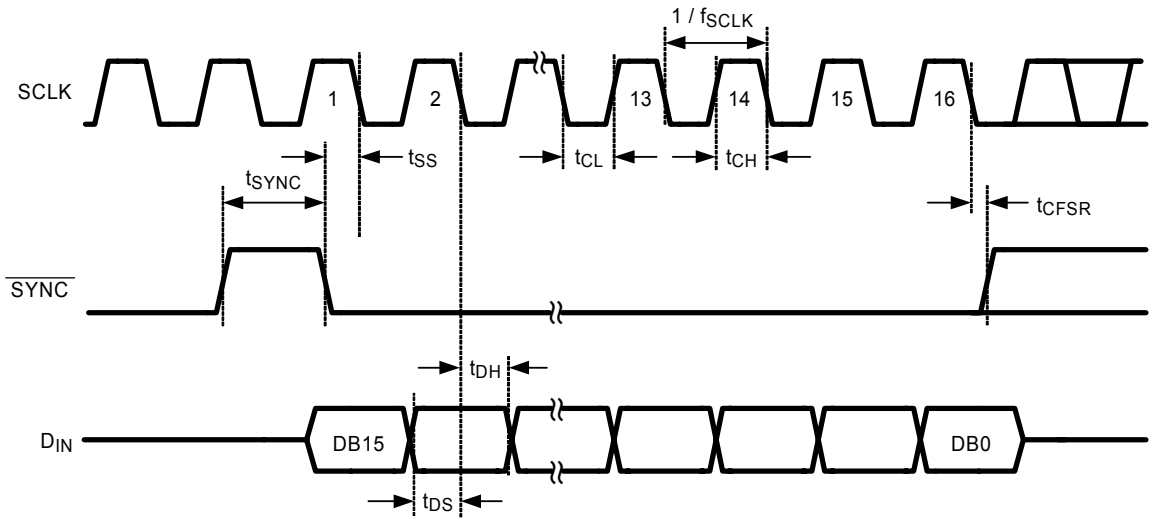
Connectors on the DAC124S085 Evaluation Board

J1: Terminal Block	VA_REMOTE. External power supply connector.
J2: SMA Footprint	Not Used
J3: Serial Interface Header	Serial Interface connector. Logic Input. (Refer to *Figure 3* for a pin-out diagram.)
J4: SMA Footprint	Not Used
J5: WV4.1 Connector	WaveVision 4.1 connector (for future use)
J6: Output Header	DC Coupled output for channels A-D

Selection Jumpers on the DAC124S085 Evaluation Board (Refer to *Table 1* in Section 4.0 for configuration details)

JP1: VA_SELECTION	Selects source of V_A.
JP2: VREF_SELECT	Selects V_{REF} Level
JP3: LOAD SELECT	Configures the output load for channels A & B
JP4: LOAD SELECT	Configures the output load for channels C & D

A2.0 Enlarged Timing Diagram



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