Evaluation Board for 32-/40-Channel, 12-/14-Bit, Parallel and Serial Input, Voltage-Output DACs

EVAL-AD5380/81/82/83EB

FEATURES

Full-featured evaluation board
On-board reference
On-board ADC for MON_OUT voltage readback
Link options
Direct hook-up to printer port of PC
PC software for control of DACs

INTRODUCTION

This evaluation board is for the AD5380, AD5381, AD5382, and AD5383, 32-/40-channel, 12-/14-bit DACs. The AD538x parts contain 32/40, 12-/14-bit DACs in one package. They have a maximum output voltage span of 5 V derived from a reference voltage of 2.5 V.

The AD538x parts have a parallel interface in which 12/14 data bits are loaded into one of the input registers under the control of the $\overline{WR}$, $\overline{CS}$, and DAC channel address pins, A0 to A5. They also have a 2-wire I^2C interface and a 3-wire serial interface, which are compatible with SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

The DAC outputs are updated when the DAC registers receive new data. All the outputs can be updated simultaneously by taking the $\overline{LDAC}$ input low.

Each channel has a programmable gain and offset adjust register. Each DAC output is gained and buffered on-chip.

See the AD5380, AD5381, AD5382, and AD5383 data sheets for product details.

AD538x EVALUATION BOARD POWER SUPPLIES

The following external supplies must be provided:

- 5 V between the DV_{CC} and DGND inputs for the digital supply of the AD538x.
- 5 V between the AV_{CC} and AGND inputs for the analog supply of the AD538x.

Both AGND and DGND inputs are provided on the board. The AGND and DGND planes are connected at one location close to the AD538x. Avoid connecting AGND and DGND elsewhere in the system to avoid ground loop problems.

Each supply is decoupled to the relevant ground plane with 47 µF and 0.1 µF capacitors. Each device supply pin is again decoupled with a 10 µF and 0.1 µF capacitor pair to the relevant ground plane.

FUNCTIONAL BLOCK DIAGRAM

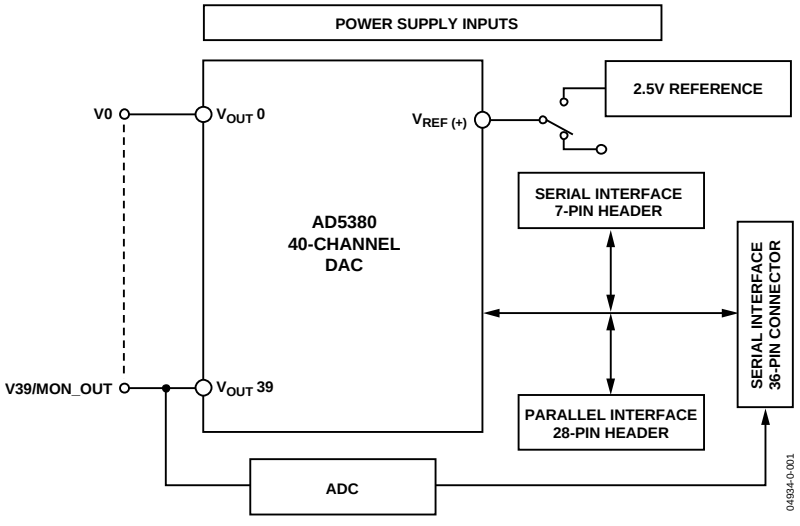

Figure 1.

Rev. 0

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REVISION HISTORY

7/04 —Revision 0: Initial Version

LINK AND SWITCH OPTIONS

The link and switch options on the evaluation board should be set for the required operating setup before using the board. The functions of the link and switch options are described in Table 1.

Table 1. Link Options

Link/Switch No.	Function
LK1	For normal operation, this link should be in the off position.
	When this link is in the on position, it connects the RESET pin to DGND, resetting the AD538x.
LK2	For normal operation, this link should be in the off position.
	When this link is in the on position, it connects the CLR pin to DGND, clearing the outputs of the AD538x to the user-programmed value.
LK3	This link selects the state of the $\overline{\text{LDAC}}$ pin.
	In the on position, $\overline{\text{LDAC}}$ is connected to DGND and, therefore, the DACs update automatically.
	In the off position, $\overline{\text{LDAC}}$ is connected to DV_{CC} and must be brought low by the digital interface to update the DACs.
LK4	This link selects the reference.
	Position A selects the externally applied reference at J8.
	Position B selects the on-board 2.5 V reference.
S1	Dual function input.
	In parallel mode, this switch should be placed in its center position.
	In serial mode, this switch selects the interface.
	Position H selects the I^2C interface.
	Position L selects the SPI interface.
S2	In both parallel and SPI modes, this switch should be set to its center position.
	In I^2C mode, this switch selects the state of the Address Bit AD0.
	Position H sets AD0 = 1.
	Position L sets AD0 = 0.
S3	In parallel mode, this switch should be set to its center position.
	In I^2C mode, this switch selects the state of the Address Bit AD1.
	Position H sets AD1 = 1.
	Position L sets AD1 = 0.
	In SPI mode, this switch selects the state of daisy-chain mode.
	Position H enables daisy-chain mode.
	Position L disables daisy-chain mode.
S4	This switch selects the state of the input FIFO.
	Position H enables the input FIFO.
	Position L disables the input FIFO.
S5	This switch selects the mode.
	Position H selects serial mode.
	Position L selects parallel mode.
S6	This switch selects the power-down state.
	Position H powers down the AD538x.
	Position L removes the AD538x from power-down.

LINK AND SWITCH OPTION SETUP FOR PC CONTROL

The PC controls the AD538x over the SPI interface, which must be enabled for PC control. The link and switch options for PC control are listed in Table 2.

Table 2. Link and Switch Options for PC Control

Link/Switch No.	Option
LK1	Off
LK2	Off
LK3	Off
LK4	B
S1	L
S2	Center Position
S3	H: Daisy-Chain Mode Disabled L: Daisy-Chain Mode Enabled
S4	H: FIFO Enabled L: FIFO Disabled
S5	H
S6	L

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

The EVAL-AD5380/81/82/83EB evaluation kit includes self-installing software on CD-ROM. If the setup file does not run automatically, you can run setup.exe from the CD-ROM.

The evaluation board software is compatible with Windows® 95 to Windows XP. Ensure that the Centronics cable connects the PC to the EVAL-AD5380/81/82/83EB evaluation board.

1. On the Analog Devices menu, select **AD538x Evaluation Software**.
2. At the prompt, select the relevant device.

The **AD5380/81/82/83 Evaluation Software** dialog box is displayed. Figure 2 shows the drop-down menus (**File**, **Printer Port**, **Dac**, **Register**, and **Help**).

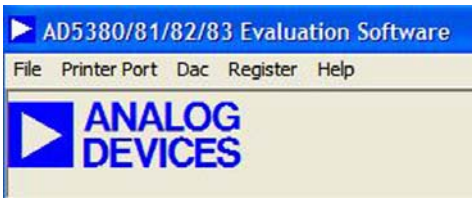

Figure 2.

LOAD DAC CHANNELS

The **Dac** menu allows user control of the 32/40 DAC channels, as well as other functions such as hardware reset of the DAC channels and clearing the outputs.

To load DAC channels:

1. On the **Dac** menu, select **Load/Calibrate Dac Channel**. The **Load/Calibrate Dac Outputs** dialog box is displayed.

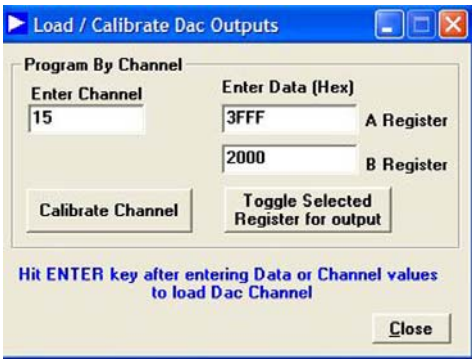

Figure 3.

2. In the Enter Channel box, enter the channel selection.
3. In the Enter Data (Hex) box, type a DAC code to load to the selected channel.
4. Press **Enter** on your keyboard after entering data.
5. Each DAC has two associated data registers, the A Register and the B Register. Click the **Toggle Selected Register for output** button to toggle between the two registers.

CHANNEL CALIBRATION

1. Click **Calibrate Channel** to display the **Channel Calibration** dialog box.

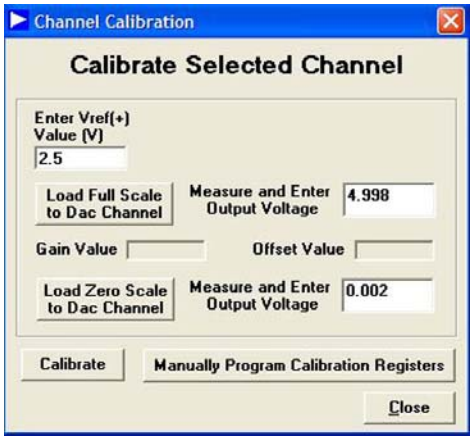

Figure 4.

2. Type the reference value in the **Enter Vref(+) Value (V)** box.
3. Load full scale and measure the output voltage on the relevant channel.
4. Input this value in the appropriate field in the dialog box.
5. Load zero scale and again enter the measured value in the appropriate field.
6. Click **Calibrate** to calibrate the device to the required output voltage.

You can also manually program the gain and offset registers.

1. Click **Manually Program Calibration Registers**. The **Program m and c Registers** dialog box is displayed.

Figure 5.

2. Type values for the gain and offset registers and click the accompanying buttons to program the registers.

PROGRAM OUTPUT RANGE

You can reduce the output range of each DAC channel using the offset and gain registers. To access the **Output Range** dialog box, select **Program Output Range** from the **Dac** menu.

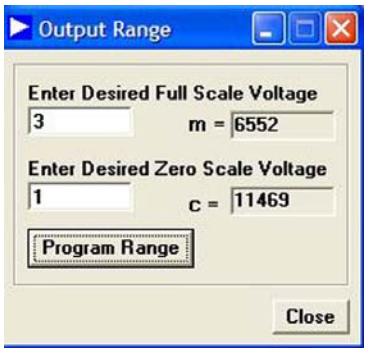

Figure 6.

1. Type the desired full-scale and zero-scale values in the appropriate boxes.
2. Click **Program Range**. The m and c registers are programmed with the displayed values, and the output range is set to the user-selected values.

SPECIAL FUNCTION REGISTER

The **Special Function Register** dialog box allows access to all the register functions. To access this dialog box, select **Special Function Register** from the **Register** menu.

Software Clear

The **Software Clear** area allows you to clear the DAC channels to a user-specified value :

1. If you want to clear the DAC channels to the user-specified value (default value is 0 V), click **Soft Clear**.
2. If you want to program the user-specified value, type the value in the **Enter Code** box and click **Write Code**.

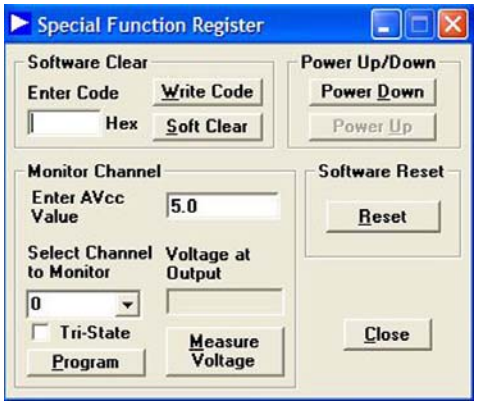

Figure 7.

Monitor Channel

The **Monitor Channel** area allows you to monitor the DAC channels via the MON_OUT pin. Before the monitor function can operate, you must enable it in the control register:

1. Type the AV_{CC} value in the **Enter AV_{CC} Value** box. This value is used as the reference for the on-board ADC.
2. Select the channel that you want to monitor in the **Select Channel to Monitor** box.
3. Optional: To three-state the MON_OUT pin, select the **Tri-State** check box.
4. Click **Program.**
5. To measure and display the voltage at the MON_OUT pin, click **Measure Voltage**.

Power Up/Down and Software Reset Functions

Click **Power Down**, **Power Up**, or **Reset**, as needed, to activate or deactivate these functions.

CONTROL REGISTER

To access the **Control Register** dialog box, select **Register** from the **AD5380/81/82/83 Evaluation Software** dialog box. The **Control Register** dialog box allows user access to all the control register functions. The current bit values of the control register are displayed in the **Contents of Control Register** area. Eight functions are available, as shown in Figure 8.

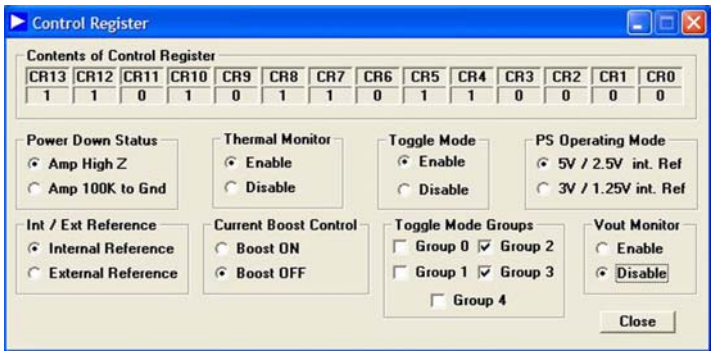

Figure 8.

COMPONENT LISTING

Table 3.

Qty	Reference Designator	Description	Supplier/Number
1	U1	AD538x	Analog Devices
1		14 mm LQFP Device Clamp	IM Tech
1	U2	AD780	Analog Devices
1	U3	AD7476ART	Analog Devices
3	R1–R3	10k Resolution (0805 Package)	FEC 911-975
12	C8–C14, C16, C18, C25, C30, C32	0.1 µF Multilayer Ceramic Capacitor (0603 Package)	FEC 499-675
10	C2–C7, C15, C17, C24, C26	10 µF Tantalum Capacitor (TAJ-A Package)	FEC 197-130
5	C19–C23	47 0pF X7R Ceramic Capacitor (0603 Package)	FEC 498-580
1	C27	10 nF X7R Ceramic Capacitor (0603 Package)	FEC 499-146
1	C28	1 µF Y5V Ceramic Capacitor (0603 Package)	FEC 317-640
2	C29, C31	47 µF Tantalum Capacitor (TAJ-C Package)	FEC 197-324
1	J1	36-Lead Centronics Connector (IEEE 488 Style)	FEC 147-753
1	J2	Header 2	FEC 148-195
7	J3–J6, J8, J9, J11	Gold 50 Ω SMB Jack	FEC 310-682
1	J7	Header 40	FEC 148-535
1	J10	Header 07	FEC 512-084
2	J12, J14	Black Banana Socket	FEC 150-040
2	J13, J15	Red Banana Socket	FEC 150-039
3	LK1–LK3	Slide Header (2 × 1 pin)	FEC 986-501
1	LK4	Slide Header (3 × 1 pin)	ERG Components JSC-16-GO
6	S1–S6	Slide Header (3 × 1 pin)	ERG Components JSC-16-GO

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

EVALUATION BOARD SCHEMATICS

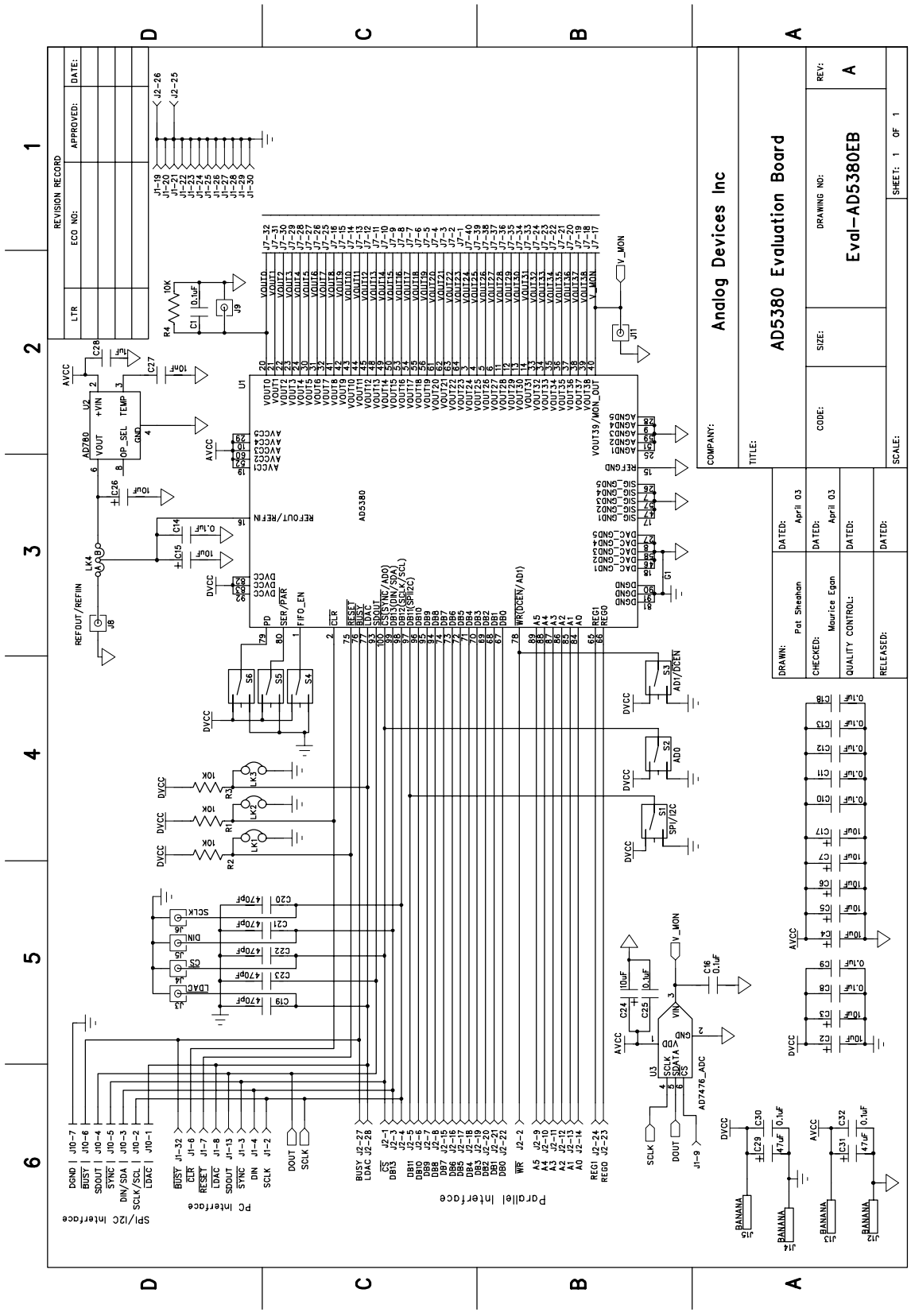

Figure 9.

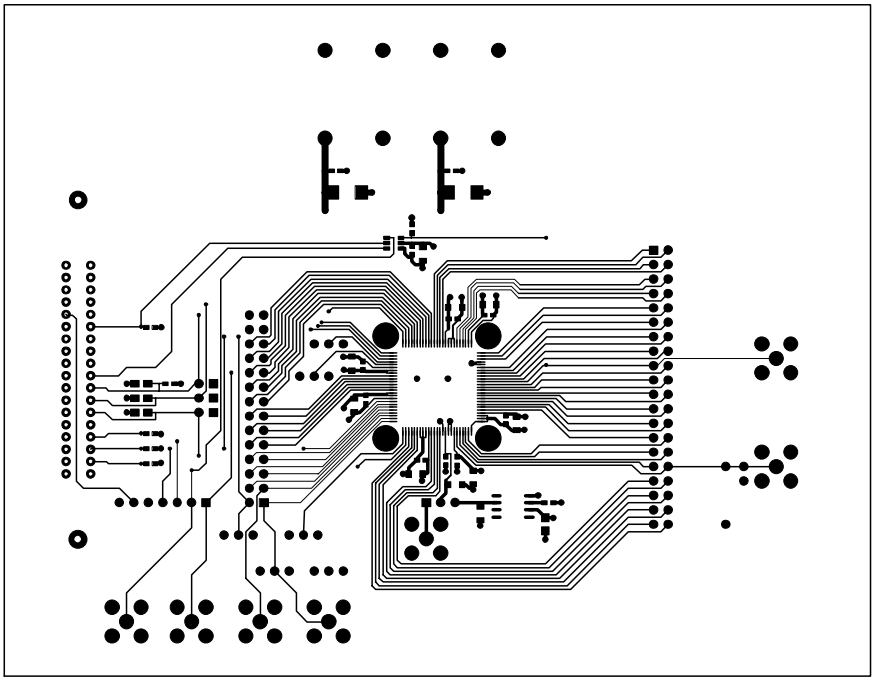

Figure 10.

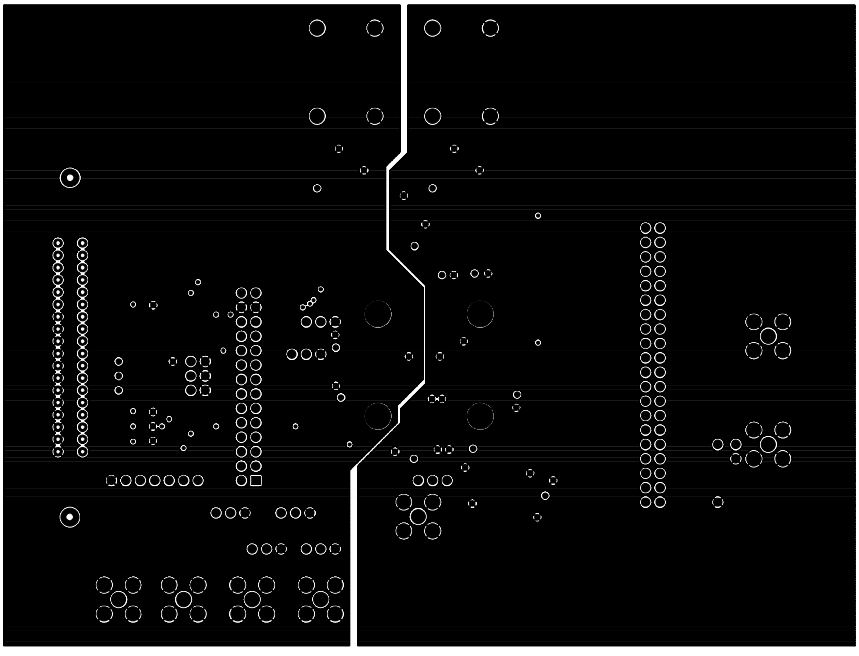

Figure 11.

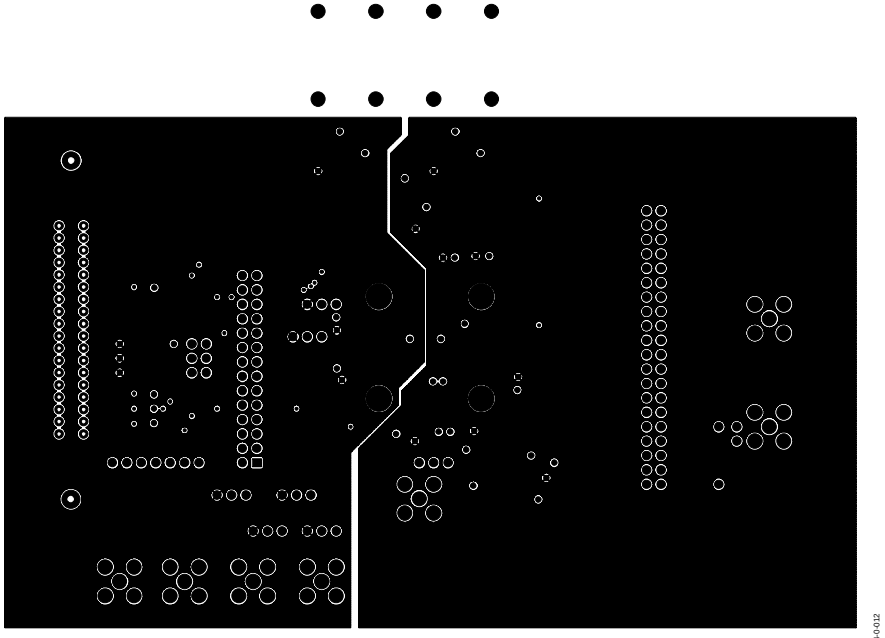

Figure 12.

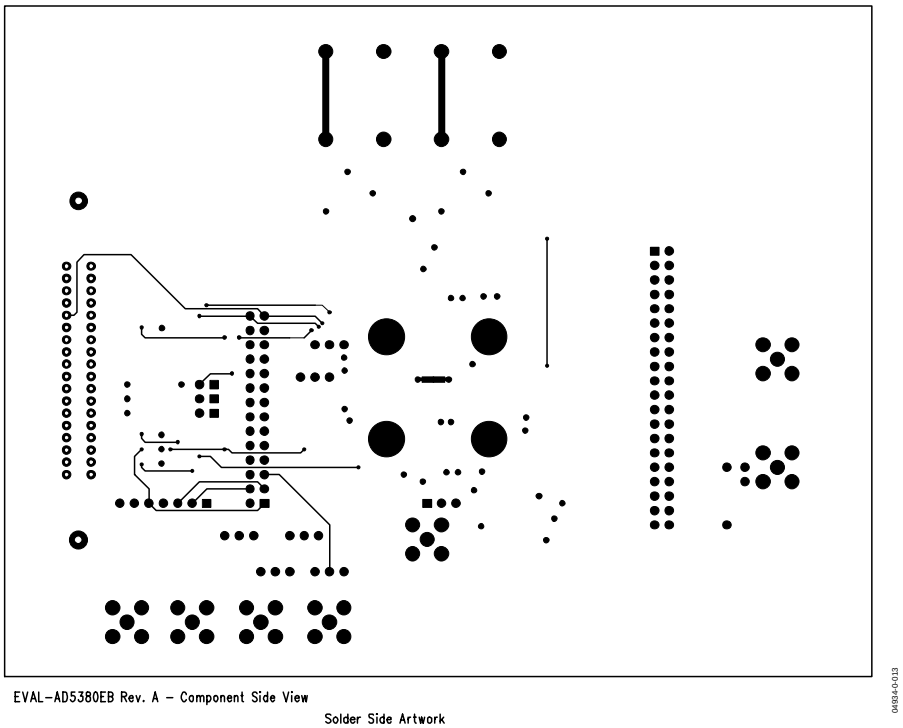

Figure 13.

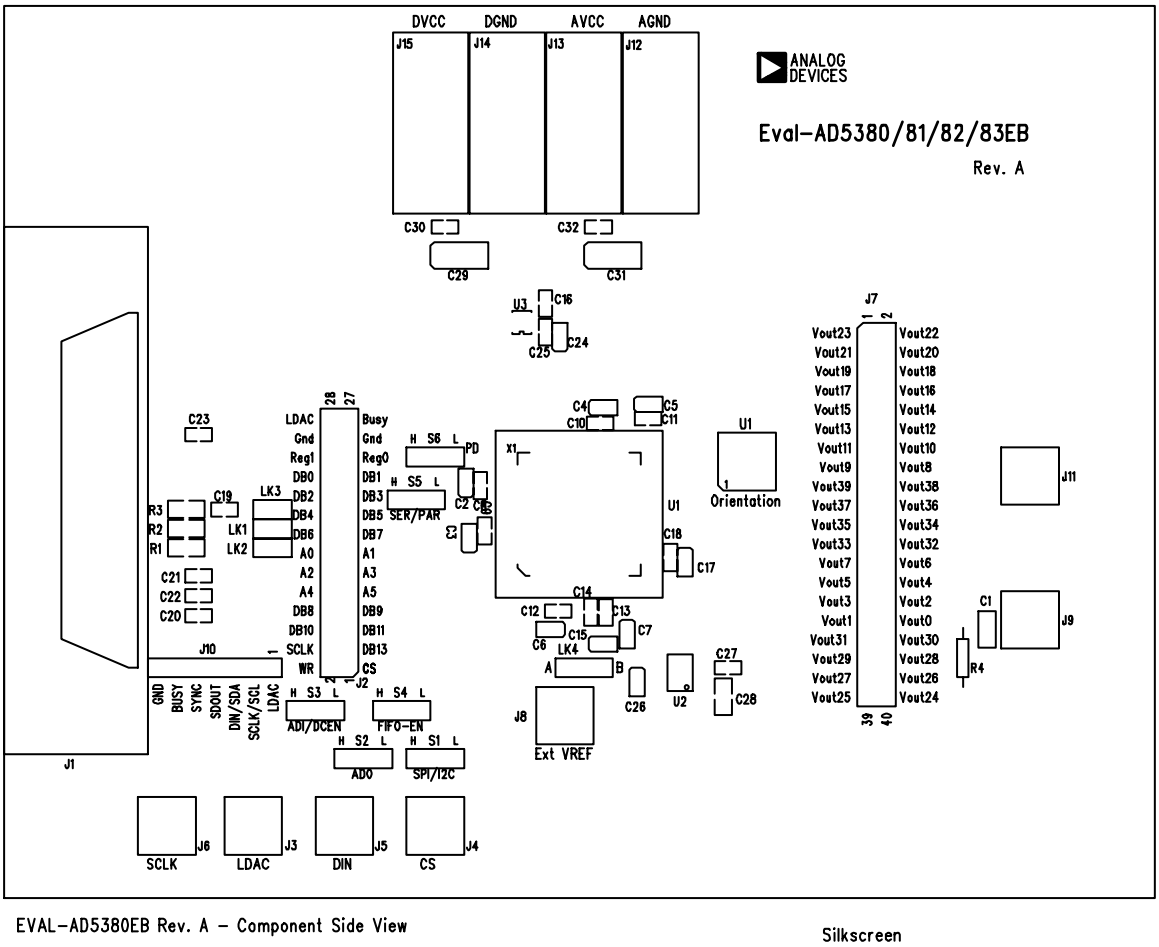

Figure 14.

ORDERING GUIDE

Model	Package Description
EVAL-AD5380EB	AD5380 Evaluation Board Kit
EVAL-AD5381EB	AD5381 Evaluation Board Kit
EVAL-AD5382EB	AD5382 Evaluation Board Kit
EVAL-AD5383EB	AD5383 Evaluation Board Kit