

### FEATURES

- Operates from dual  $\pm 12\text{ V}$  and  $+5\text{ V}$  supplies
- On-board reference and output amplifiers
- Direct hookup to printer port of PC
- PC software for control of DAC

### INTRODUCTION

This data sheet describes the evaluation board for the AD5415 DAC. The AD5415 is a CMOS 12-bit, current output digital-to-analog converter (DAC). It operates from a 2.5 V to 5.5 V power supply, making it suited to battery-powered and other applications.

On power-up, the internal register and latches are filled with 0s and the DAC outputs are at zero scale.

As a result of manufacture on a CMOS submicron process, the AD5415 offers excellent 4-quadrant multiplication characteristics, with large-signal multiplying bandwidths of up to 10 MHz.

The applied voltage reference determines the full-scale output current. An integrated feedback resistor (RFB) provides temperature tracking and full-scale voltage output when combined with an external I-to-V precision amplifier.

The evaluation board consists of the AD5415, three AD8065 op amps, and a 10 V reference, ADR01. An external reference can also be applied via an SMB input connector. DAC A is set to work in unipolar mode; DAC B is set to work in bipolar mode. Note that, while excellent for dc performance, the bandwidth performance of the combined DAC and amplifier is limited to approximately 8 MHz.

The evaluation kit includes a CD-ROM with self-installing software to control the DAC. The software allows you to exercise all functions of the AD5415.

Full data on the DAC is available in the AD5415 data sheet, which should be consulted in conjunction with this data sheet when using the evaluation board.

### EVALUATION BOARD FUNCTIONAL BLOCK DIAGRAM

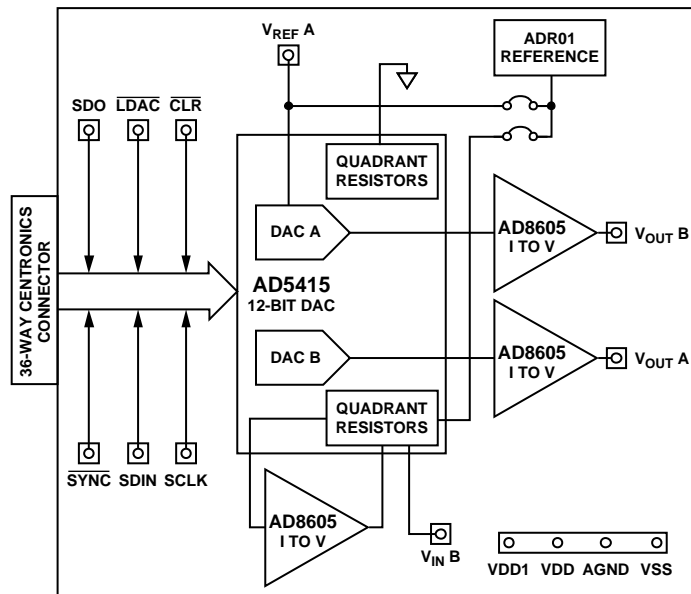


Figure 1.

### Rev. 0

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## TABLE OF CONTENTS

Operating the Evaluation Board.....	3	Ordering Information.....	7
Software Installation .....	3	Bill of Materials.....	7
Operating the Evaluation Software.....	3	Ordering Guide .....	8
Evaluating AD5415 Functions and Registers.....	3	ESD Caution.....	8
Evaluation Board Schematic .....	5		
Evaluation Board PCB Layers.....	6		

## REVISION HISTORY

10/04—Revision 0: Initial Version

## OPERATING THE EVALUATION BOARD

The evaluation board requires  $\pm 12\text{ V}$  and  $+5\text{ V}$  supplies. The  $+12\text{ V } V_{DD}$  and  $-12\text{ V } V_{SS}$  are used to power the output amplifier. The  $+5\text{ V } V_{DD1}$  is used to power the DAC. All supplies are decoupled to ground with  $10\text{ }\mu\text{F}$  tantalum and  $0.1\text{ }\mu\text{F}$  ceramic capacitors.

### SOFTWARE INSTALLATION

The evaluation kit includes self-installing software on CD-ROM. This software is compatible with Windows® 95/97/2000/NT/XP.

If the setup file does not run automatically, run the **setup.exe** file from the CD-ROM.

### OPERATING THE EVALUATION SOFTWARE

To operate the evaluation software:

1. Ensure that the centronics cable connects the PC to the evaluation board.
2. Run the program file from the **Analog Devices** menu. The **AD5415 Device Setup** dialog box is displayed, as shown in Figure 2. This dialog box lets you choose whether daisy chaining is enabled or disabled and on which edge of the clock data is clocked into the input shift register.



Figure 2. AD5415 Device Setup Dialog Box

The default settings are daisy chaining enabled and data clocked on the falling edge. Click the checkbox next to one or both of these functions, if you do not want the default setting.

3. Click OK to open the **AD5415 Evaluation Software** dialog box, as shown in Figure 3.

### EVALUATING AD5415 FUNCTIONS AND REGISTERS

From the **AD5415 Evaluation Software** dialog box, shown in Figure 3, you can evaluate all the functions of the AD5415. Table 1 and Table 2 describe the control functions and the control registers, respectively.

The dropdown **Printer Port** menu allows you to select the printer port address from a list of available addresses.

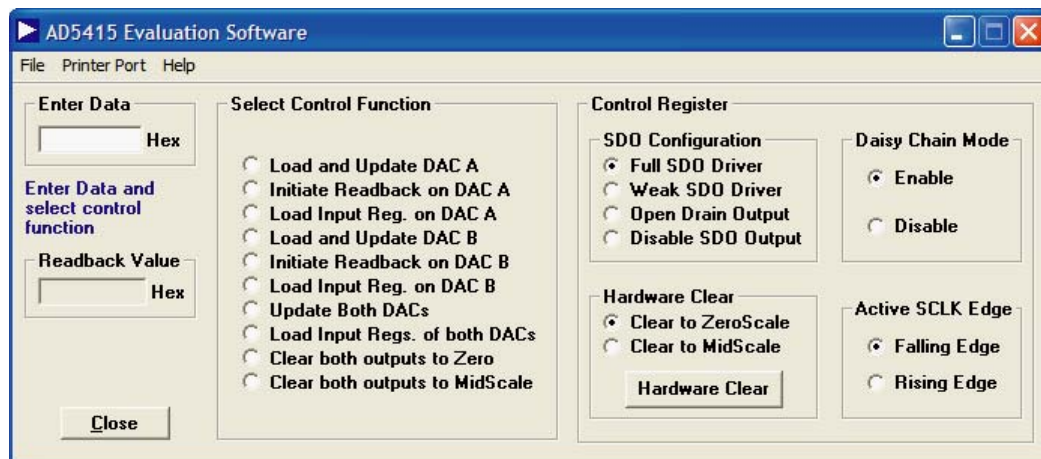


Figure 3. AD5415 Evaluation Software Dialog Box

# EVAL-AD5415EB

**Table 1. Control Functions**

<b>Control Function</b>	<b>Description</b>
Load and Update DAC A	Loads the DAC A register with the entered data-word and updates the DAC A output, irrespective of the state of $\overline{\text{LDAC}}$ .
Initiate Readback on DAC A	Reads the contents of the DAC A input register and displays the value on-screen.
Load Input Register of DAC A	Loads the DAC A register with the entered data-word. The DAC A output is updated only if $\overline{\text{LDAC}}$ is low.
Load and Update DAC B	Loads the DAC B register with entered data-word and updates the DAC B output, irrespective of the state of $\overline{\text{LDAC}}$ .
Initiate Readback on DAC B	Reads the contents of the DAC B input register and displays the value on-screen.
Load Input Register of DAC B	Loads DAC B register with entered data-word. The DAC B output is updated only if $\overline{\text{LDAC}}$ is low.
Update Both DACs	Updates both DAC outputs with the entered data-word, irrespective of the state of $\overline{\text{LDAC}}$ .
Load Input Registers of Both DACs	Loads the input registers of both DACs with the entered data-word. Both outputs are updated only if $\overline{\text{LDAC}}$ is low.
Clear Both Outputs to Zero Scale	Loads both DACs and updates their outputs with zero-scale code, irrespective of the state of $\overline{\text{LDAC}}$ .
Clear Both Outputs to Midscale	Loads both DACs and updates their outputs with midscale code, irrespective of the state of $\overline{\text{LDAC}}$ .

**Table 2. Control Register**

<b>Control Register</b>	<b>Description</b>
SDO Configuration	The SDO bits enable you to control the SDO output driver strength, disable the SDO output, or configure it as an open-drain driver. The strength of the SDO driver affects timing. A stronger SDO output driver allows a faster clock cycle to be used.
Daisy-Chain Mode	Enables or disables daisy-chain functionality.
Hardware Clear	Sets the value to which the outputs are cleared on the falling edge of the $\overline{\text{CLR}}$ signal. The value can be either zero scale or midscale.
Active SCLK Edge	Selects the edge of SCLK on which data is clocked into the input register. Data is clocked out from SDO on the opposite edge.

EVALUATION BOARD SCHEMATIC

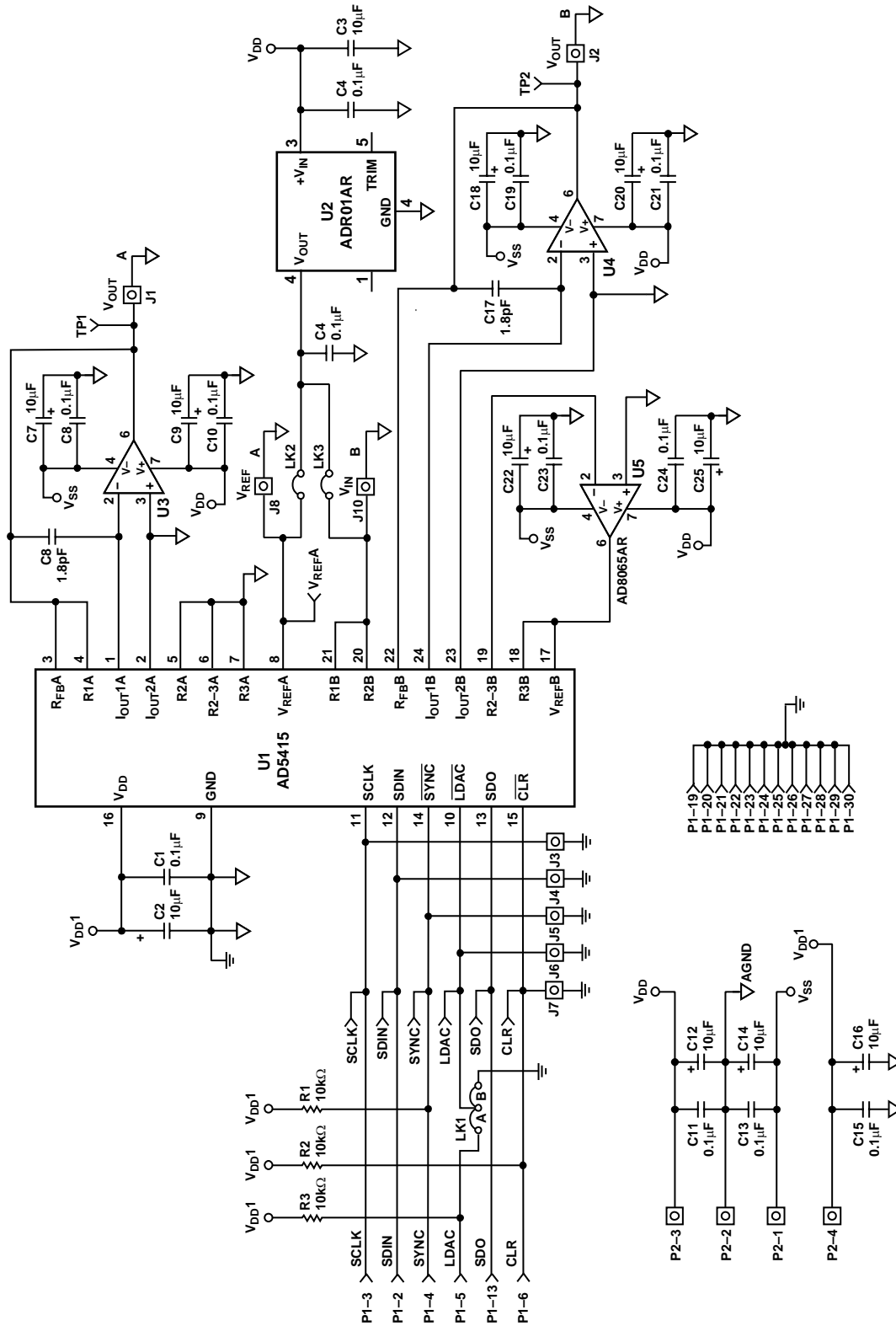


Figure 4. Evaluation Board Schematic

06216-004

# EVAL-AD5415EB

## EVALUATION BOARD PCB LAYERS

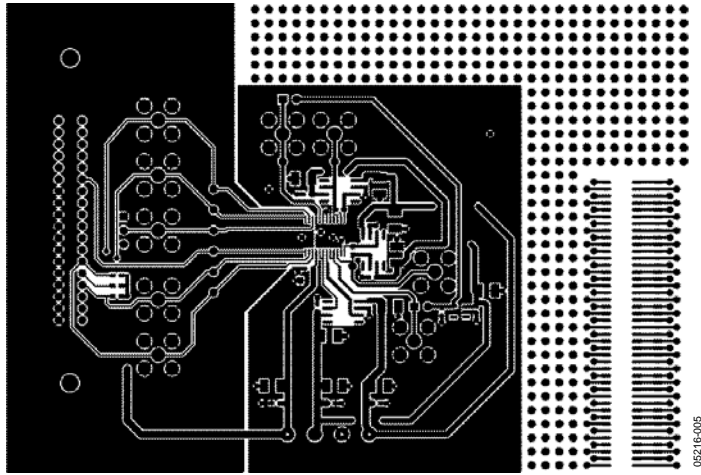


Figure 5. Component-Side Artwork

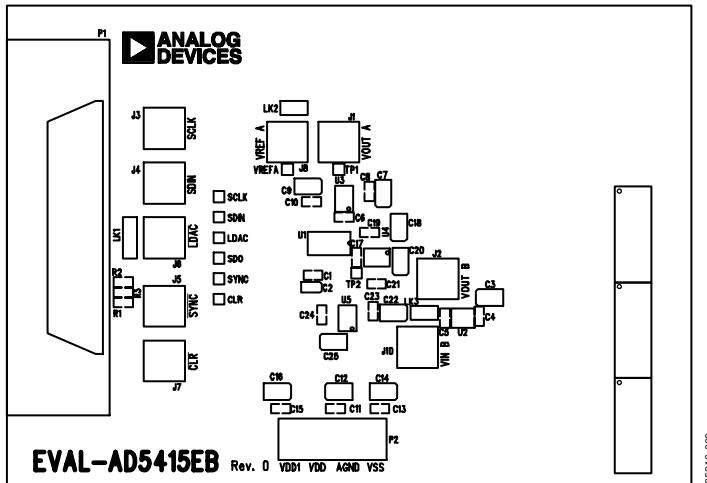


Figure 6. Silkscreen—Component-Side View (Top)

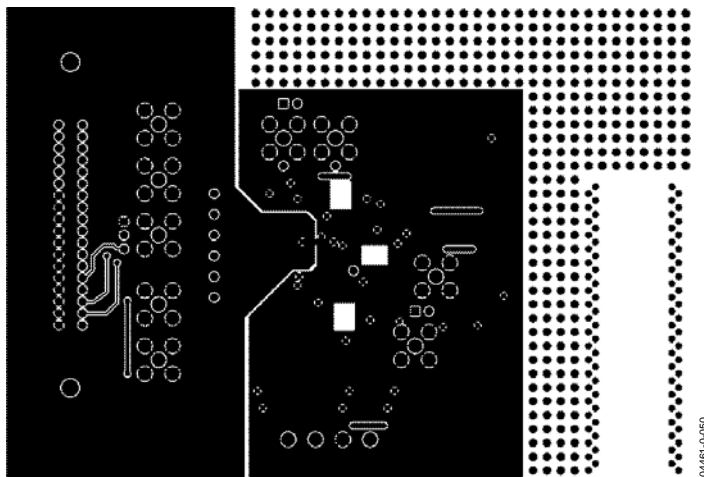


Figure 7. Solder-Side Artwork

## ORDERING INFORMATION

### BILL OF MATERIALS

Table 3.

Name	Part Type	Value	PCB Decal	SMD	Part Description	Stock Code
C1	CAP	0.1 $\mu$ F	0603	Yes	Multilayer Ceramic Capacitor—X7R	FEC 499-675
C2	CAP+	10 $\mu$ F	CAP\TAJ_A	Yes	Tantalum Capacitor—Taj Series—10 V	FEC 197-130
C3	CAP+	10 $\mu$ F	CAP\TAJ_B	Yes	Tantalum Capacitor—Taj Series—20 V	FEC 197-427
C4	CAP	0.1 $\mu$ F	0603	Yes	Multilayer Ceramic Capacitor—X7R	FEC 499-675
C5	CAP	0.1 $\mu$ F	0603	Yes	Multilayer Ceramic Capacitor—X7R	FEC 499-675
C6	CAP	1.8 pF	0603	Yes	Multilayer Ceramic Capacitor—NPO	FEC 721-876
C7	CAP+	10 $\mu$ F	CAP\TAJ_B	Yes	Tantalum Capacitor—Taj Series—20 V	FEC 197-427
C8	CAP	0.1 $\mu$ F	0603	Yes	Multilayer Ceramic Capacitor—X7R	FEC 499-675
C9	CAP+	10 $\mu$ F	CAP\TAJ_B	Yes	Tantalum Capacitor—Taj Series—20 V	FEC 197-427
C10	CAP	0.1 $\mu$ F	0603	Yes	Multilayer Ceramic Capacitor—X7R	FEC 499-675
C11	CAP	0.1 $\mu$ F	0603	Yes	Multilayer Ceramic Capacitor—X7R	FEC 499-675
C12	CAP+	10 $\mu$ F	CAP\TAJ_B	Yes	Tantalum Capacitor—Taj Series—20 V	FEC 197-427
C13	CAP	0.1 $\mu$ F	0603	Yes	Multilayer Ceramic Capacitor—X7R	FEC 499-675
C14	CAP+	10 $\mu$ F	CAP\TAJ_B	Yes	Tantalum Capacitor—Taj Series—20V	FEC 197-427
C15	CAP	0.1 $\mu$ F	0603	Yes	Multilayer Ceramic Capacitor—X7R	FEC 499-675
C16	CAP+	10 $\mu$ F	CAP\TAJ_B	Yes	Tantalum Capacitor—Taj Series—20V	FEC 197-427
C17	CAP	1.8 pF	0603	Yes	Multilayer Ceramic Capacitor—NPO	FEC 721-876
C18	CAP+	10 $\mu$ F	CAP\TAJ_B	Yes	Tantalum Capacitor—Taj Series—20 V	FEC 197-427
C19	CAP	0.1 $\mu$ F	0603	Yes	Multilayer Ceramic Capacitor—X7R	FEC 499-675
C20	CAP+	10 $\mu$ F	CAP\TAJ_B	Yes	Tantalum Capacitor—Taj Series—20 V	FEC 197-427
C21	CAP	0.1 $\mu$ F	0603	Yes	Multilayer Ceramic Capacitor—X7R	FEC 499-675
C22	CAP+	10 $\mu$ F	CAP\TAJ_B	Yes	Tantalum Capacitor—Taj Series—20 V	FEC 197-427
C23	CAP	0.1 $\mu$ F	0603	Yes	Multilayer Ceramic Capacitor—X7R	FEC 499-675
C24	CAP	0.1 $\mu$ F	0603	Yes	Multilayer Ceramic Capacitor—X7R	FEC 499-675
C25	CAP+	10 $\mu$ F	CAP\TAJ_B	Yes	Tantalum Capacitor—Taj Series—20 V	FEC 197-427
CLR	TESTPOINT		TESTPOINT	No	Red Testpoint	FEC 240-345 (Pack)
J1	SMB		SMB	No	SMB Socket	FEC 310-682
J2	SMB		SMB	No	SMB Socket	FEC 310-682
J3	SMB		SMB	No	SMB Socket	FEC 310-682
J4	SMB		SMB	No	SMB Socket	FEC 310-682
J5	SMB		SMB	No	SMB Socket	FEC 310-682
J6	SMB		SMB	No	SMB Socket	FEC 310-682
J7	SMB		SMB	No	SMB Socket	FEC 310-682
J8	SMB		SMB	No	SMB Socket	FEC 310-682
J10	SMB		SMB	No	SMB Socket	FEC 310-682
LDAC	TESTPOINT		TESTPOINT	No	Red Testpoint	FEC 240-345 (Pack)
LK1	JUMPER-2\SIP3		LINK-3P_TEXT_INV	No	3-Pin Header (3 $\times$ 1)	FEC 511-717 and 150-411
LK2	JUMPER		SIP-2P	No	2-Pin Header (2 $\times$ 1)	FEC 511-705 and 150-411
LK3	JUMPER		SIP-2P	No	2-Pin Header (2 $\times$ 1)	FEC 511-705 and 150-411
P1	CENTRONICS		36WAY	No	36-Pin 90° Centronics Connector	FEC 147-753
P2	CON\POWER4		CON\POWER4	No	4-Pin Terminal Block	FEC 151-791
R1	RES	10 k $\Omega$	0603	Yes	Resistor	FEC 911-355
R2	RES	10 k $\Omega$	0603	Yes	Resistor	FEC 911-355
R3	RES	10 k $\Omega$	0603	Yes	Resistor	FEC 911-355
SCLK	TESTPOINT		TESTPOINT	No	Red Testpoint	FEC 240-345 (Pack)
SDIN	TESTPOINT		TESTPOINT	No	Red Testpoint	FEC 240-345 (Pack)
SDO	TESTPOINT		TESTPOINT	No	Red Testpoint	FEC 240-345 (Pack)
SYNC	TESTPOINT		TESTPOINT	No	Red Testpoint	FEC 240-345 (Pack)
TP1	TESTPOINT		TESTPOINT	No	Red Testpoint	FEC 240-345 (Pack)

# EVAL-AD5415EB

Name	Part Type	Value	PCB Decal	SMD	Part Description	Stock Code
TP2	TESTPOINT		TESTPOINT	No	Red Testpoint	FEC 240-345 (Pack)
U1	AD5415		TSSOP24	Yes	D/A Converter	AD5415YRU
U2	ADR01_TSOT		TSOT-5	Yes	10 V Reference	ADR01AUJ
U3	OP07		SO8NB	Yes	Single Op Amp, 8-Pin	AD8065AR
U4	OP07		SO8NB	Yes	Single Op Amp, 8-Pin	AD8065AR
U5	OP07		SO8NB	Yes	Single Op Amp, 8-Pin	AD8065AR
VREFA	TESTPOINT		TESTPOINT	No	Red Testpoint	FEC 240-345 (Pack)
					Rubber Stick-On Feet (x4)	FEC 148-922
					Evaluation Kit CD-ROM and Sleeve	ADI Issue
					Barcode Label	ADI Issue
					Evaluation Board Box	
					Antistatic Bag	
					Bubble Wrap	

## ORDERING GUIDE

Model	Description
EVAL-AD5415EB	Evaluation Board

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

