Power Management Controller For Mixed-Voltage FPGA Based Systems

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Introduction

Field Programmable Gate Arrays (FPGAs) are providing a path for rapid prototyping and implementation of digital systems. The classes of programmable logic devices vary based on memory utilization and configuration. Power management systems designed to support them must stand-up to potential programming enhancements which boost their power requirements. Responding to the changing needs of the industry, Intersil introduces the ISL6521 controller to power mixed-voltage FPGAs.

The versatility of the ISL6521 lends well to powering most any embedded processor or logic device which require a regulated high current, low voltage supply and up to three independent, lower current supplies.

Intersil ISL6521

The ISL6521 regulates four output voltages and provides simple protection functions. The PWM controller drives two external N-Channel MOSFETs in a synchronous buck converter topology. This output is intended to power the internal core logic (V_{CCINT}). The integrated linear controllers can drive up to 120mA directly, or up to 3A with an external NPN pass transistor. The linear controllers typically power the I/O bank (V_{CCO}), input buffer reference voltage (V_{REF}), and the auxiliary logic (V_{CCAUX}). The power management block diagram for an FPGA is shown in Figure 1. Integrated high-bandwidth error amplifiers and an accurate internal voltage reference insure a ±2% static voltage regulation tolerance over line, load and temperature ranges.

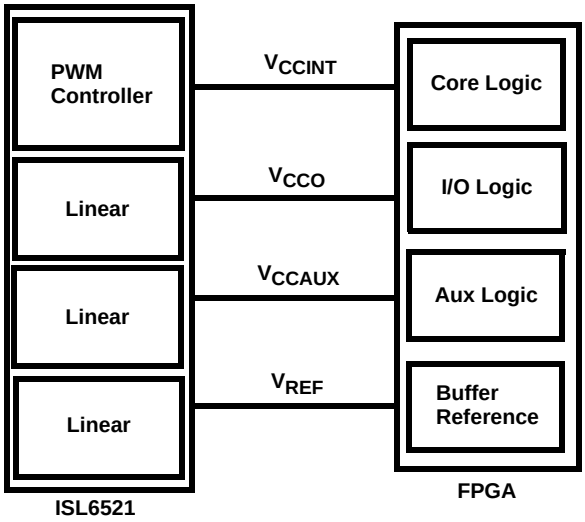


FIGURE 1. FPGA POWER MANAGEMENT BLOCK DIAGRAM

The ISL6521 features overcurrent protection of the switching converter and simple undervoltage protection of the linear controllers. For a more detailed description of the ISL6521 functionality, refer to the ISL6521 Data Sheet [1].

The ISL6521EVAL1 Reference Design

The ISL6521EVAL1 evaluation board is intended to provide a versatile platform for evaluation of surface mount and thru hole components. The evaluation board is designed to meet the output voltage and current specifications shown in Table 1. The synchronous buck converter can sustain 5A of continuous load current and handle 5A step, 2.5A/µs load current transients. Two linear regulators are designed to supply 1A of continuous load current with the third linear regulator providing 100mA with no external pass device. The board is implemented on a 1-ounce, 2-layer, printed circuit board. See pages 5-8 for schematic, bill of materials, and layout plots.

TABLE 1. ISL6521EVAL1 DESIGN PARAMETERS

PARAMETER	MAX	MIN
Buck Regulator:		
Static Regulation **VOUT1**	1.530V	1.470V
Continuous Load Current	5A	
Load-Current Transient	2.5A/µs	
Linear Regulators:		
Static Regulation **VOUT2**	3.366V	3.234V
Continuous Load Current	1A	
Static Regulation **VOUT3**	2.550V	2.450V
Continuous Load Current	1A	
Static Regulation **VOUT4**	1.836V	1.764V
Continuous Load Current	120mA	100mA

Quick Start Evaluation

Circuit Setup

Connect a +5V bench top power supply to the +5V and GND turrets located next to the Intersil logo, see Figure 2. Each output has a similar pair of turrets labeled VOUTx and GND. Each output can be exercised using either resistive or electronic loads connected across these points. Once the external supply and loads are connected to the board, the +5V supply can be energized. A light emitting diode, D2, should burn red to indicate power has been applied to the board. If D2 is not red, power-down the supply and check all external connections.

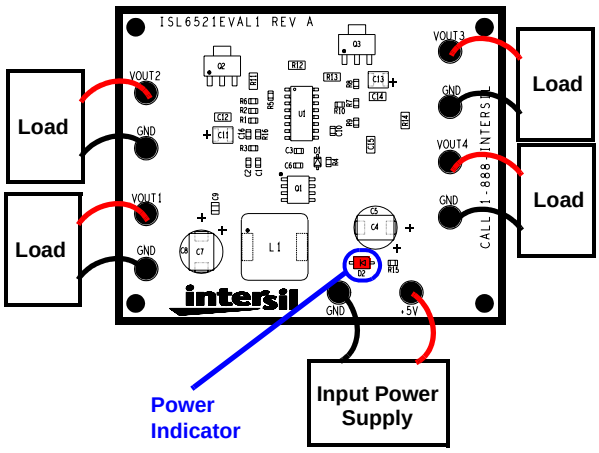


FIGURE 2. EXTERNAL POWER SUPPLY AND LOAD CONNECTIONS

ISL6521EVAL1 Performance

Enabling the Controller

Once the bias voltage applied to the PWM controller reaches the rising Power-On Reset (POR) threshold, the ISL6521 initiates a soft-start interval. The point at which the ISL6521 reaches the rising POR threshold is indicated as **Soft-start Begins** in Figure 3. After a short delay, the four outputs begin ramping to the output levels set by external resistor dividers to the FB pins. The controlled voltage ramp of all four outputs charges the output capacitors of each output slowly and softens the initial current drawn from the bias supply. Reducing the soft-start interval lasts about 3ms and ends just after all four output reach their programmed output levels. The point soft-start ends is indicated as **Soft-start Ends** in Figure 3.

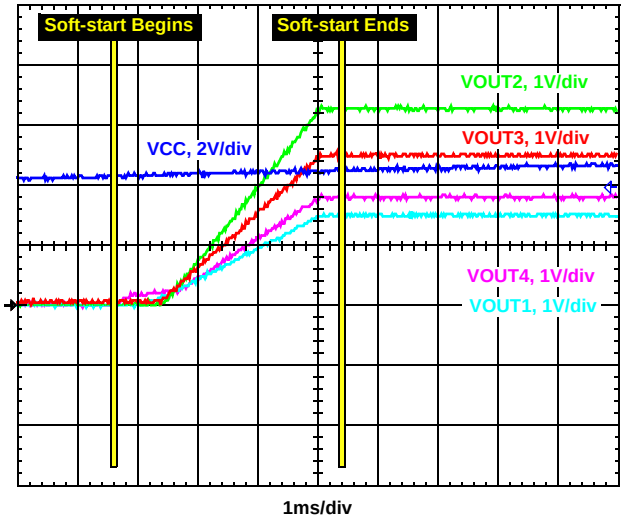


FIGURE 3. SOFT-START INTERVAL

Output Voltage Ripple

The evaluation platform is designed to meet a core voltage ripple specification of 20mV. Board performance is shown in Figure 4, under room temperature conditions and light loading. The output voltage ripple measures less than 18mV. Adjustment of output voltage ripple is addressed in the *Adapting Circuit Performance* section.

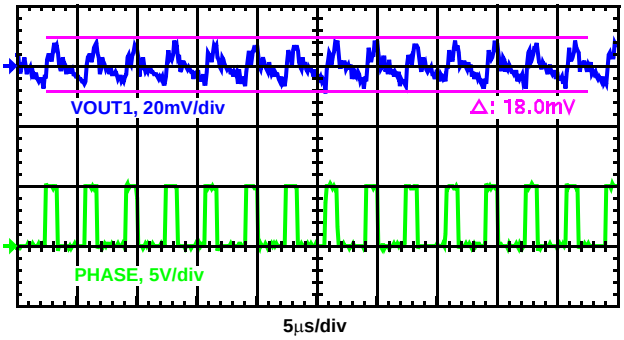


FIGURE 4. CORE VOLTAGE RIPPLE (VOUT1)

Protection Features

The ISL6521 features overcurrent protection on the PWM controller. The linear controllers feature undervoltage protection which doubles as overcurrent protection.

The PWM controller uses the upper MOSFET's on-resistance, $r_{DS(on)}$, to monitor the current flow through the device. This current level is then compared internally to the overcurrent trip point set externally. The overcurrent protection monitors these conditions on a cycle by cycle basis. When the overcurrent trip level is exceeded, the PWM controller removes gate drive to the MOSFETs. The ISL6521 then enters a wait period equivalent to three soft-start intervals. A soft-start interval follows and if the overcurrent condition remains, the controller will trip off again. This results in the hiccup mode response to a sustained short shown in Figure 5. The PWM controller exits this mode once the output voltage soft-starts successfully or bias is removed from the controller.

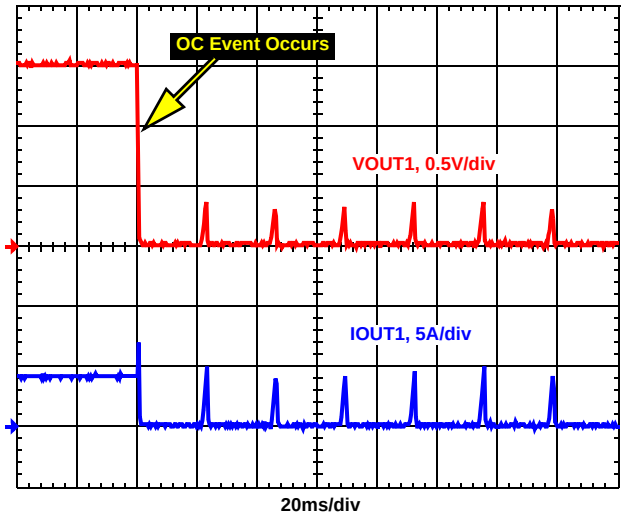


FIGURE 5. HICCUP MODE OVERCURRENT PROTECTION

The ISL6521EVAL1 is designed with a room temperature overcurrent trip point of 7A. The trip point is set by the OCSET resistor and is established relative to the $r_{DS(on)}$ of the upper MOSFET. See the product datasheet for additional information on setting this trip point.

The linear controllers feature undervoltage protection which also provide overcurrent protection. A low impedance short on a linear output will cause the output voltage to sag. When the output voltage drops below 70% of the output voltage set point, the linear controller shuts down. The linear controller then enters a wait period equivalent to three soft-start intervals. A soft-start interval follows and if the undervoltage condition remains, the linear controller will shutdown during soft-start. Until successful, the linear controller will attempt to restart the output in the same hiccup mode style outlined above.

Shutdown on any one output does not shutdown all outputs.

Transient Response

FPGA transient specifications vary depending on overall gate usage. The ISL6521EVAL1 is designed to meet a load step of 5A with a slew rate of 2.5A/µs. During a transient, the FPGA core voltage (VOUT1) must not exceed ±50mV of +1.5V. The leading edge transient response of the ISL6521EVAL1 to the aforementioned load is shown in Figure 6. The core voltage waveform is offset to +1.5V.

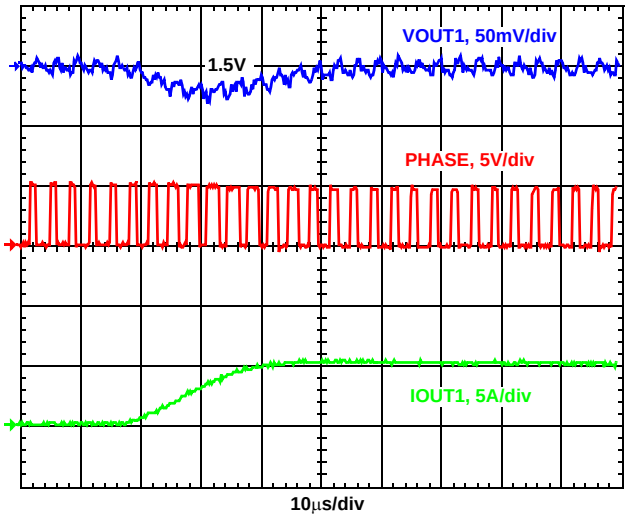


FIGURE 6. LEADING EDGE TRANSIENT RESPONSE

The core voltage sags as the inductor current begins to slew in response to the changing load current. The controller detects the new load level by the drop in output voltage and responds by increasing the pulse width to the upper MOSFET. The bulk output capacitors support the load as the inductor slews. The increase in duty cycle can be seen looking at the PHASE waveform just before, during, and after the transient edge reaches 5A. The inductor current rapidly increases to meet the new demand, supplying an increasing portion of the load. The output voltage returns to the +1.5V set point as the inductor picks up the load again.

In Figure 7, the output voltage rises in response to the removal of load and the inductor begins to slew down to the original load level. The controller detects the output voltage rise and immediately decreases the upper gate pulse width. The PHASE waveform shows that upper gate is not turned on for three to four cycles as the inductor sheds load. The upper gate pulse width is then narrow for the next few cycles as the inductor slowly picks up load current. The output voltage quickly settles back to the +1.5V set point.

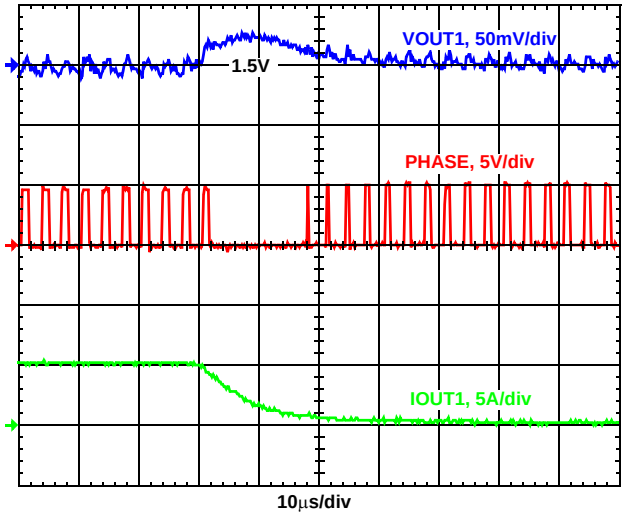


FIGURE 7. TRAILING EDGE TRANSIENT RESPONSE

The leading edge transient response is less than 30µs and the trailing edge transient response is less than 20µs. Achieving a faster transient response time means reducing the output inductance. The lower inductance would allow the inductor current to transition faster as load current changes. The main trade-off in speeding up transient response is a drop in efficiency due to the reduced inductance.

Efficiency

The performance of the ISL6521EVAL1 board, loaded from 1A to 6A, is plotted in Figure 8. Measurements were taken at

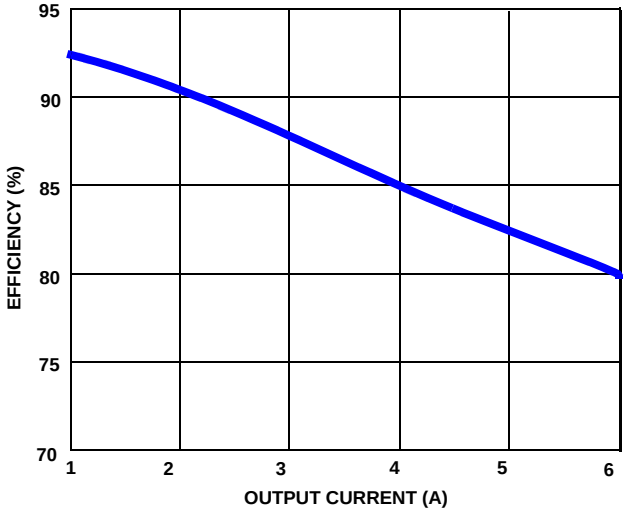


FIGURE 8. EFFICIENCY vs LOAD CURRENT

room temperature at thermal equilibrium with no air flow. The PWM converter design targets applications which specify a minimum full load efficiency of 80%. Design modifications to the output inductor and/or dual N-channel MOSFETs allow for achieving higher efficiency.

Adapting Circuit Performance

The board outlined in this application note supports the use of both surface mount and thru hole devices. This feature adds flexibility to the evaluation process by allowing easy replacement of components with counterparts for cost versus performance curve balancing.

In surface mount only applications or designs with height restrictions, the aluminum electrolytic bulk output capacitors could be replaced with surface mount capacitors with similar ESR characteristics and achieve similar performance. The Sanyo SVPC series or Panasonic SP series capacitors provide surface mount options over a range of price points.

Depending on the PWM output voltage ripple requirements, inductor and output capacitor selection are critical in achieving desired circuit performance. Care must be taken to adjust the compensation components when changing output capacitance and/or inductance.

Linear Combinations

The ISL6521 linear controllers can be used individually to provide 120mA each or drive an external pass device to achieve up to 3A. Two linear controllers can be ganged together to create one 240mA regulator or all three linears can be tied together to source 360mA. The ISL6521EVAL1 evaluation platform supports evaluation of this option. First, the external pass devices, Q2 and Q3, must be removed. The external pass devices, outlined in yellow, are highlighted in Figure 9. Next, resistors options, outlined in green, must be populated to short the output planes of each linear together. The feedback resistor pairs, accented in red, for each linear must be matching to provide proper voltage feedback. The minimum current output, over temperature and process variations, from the combined linears is 300mA.

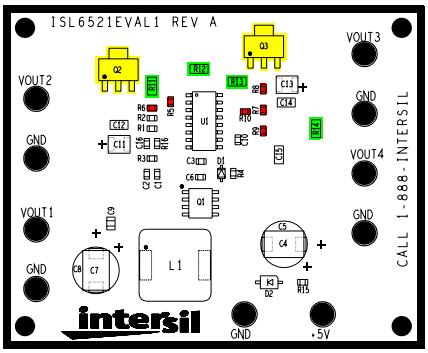


FIGURE 9. COMPONENT CHANGES FOR COMBINING LINEARS

Layout Considerations

Component placement and trace layout is important in high frequency switching converter design. With power devices switching efficiently at 300kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device over-voltage stress. Careful component layout and printed circuit board design minimizes these voltage spikes.

Component Placement

The switching components should be placed close to the ISL6521 first. Minimize the length of the connections between the input capacitors, C4 and C5, and the power switch, Q1, by placing them nearby. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible. Position the output inductor and output capacitors between the upper and lower MOSFETs and the load.

The critical small signal components include any bypass capacitors, feedback components, and compensation components. Place the PWM converter compensation components close to the FB and COMP pins. The feedback resistors should be located as close as possible to the FB pin with vias tied straight to the ground plane as required.

Trace Routing and Interconnects

Keep the trace from the PHASE terminal to the output inductor short and wide. A power plane layer, if available, should support the input power and output power nodes. Use copper filled polygons on the phase node layers. Keep the traces from the UGATE and LGATE pins to the MOSFET gates short and wide to easily handle the 1A of drive current.

In order to dissipate heat generated by the internal linears and PWM drivers, the ground pads (pins 5 and 9) should be connected to the ground plane through at least four vias. This allows the heat to move away from the IC and also ties the pad to the ground plane through a low impedance path.

Summary

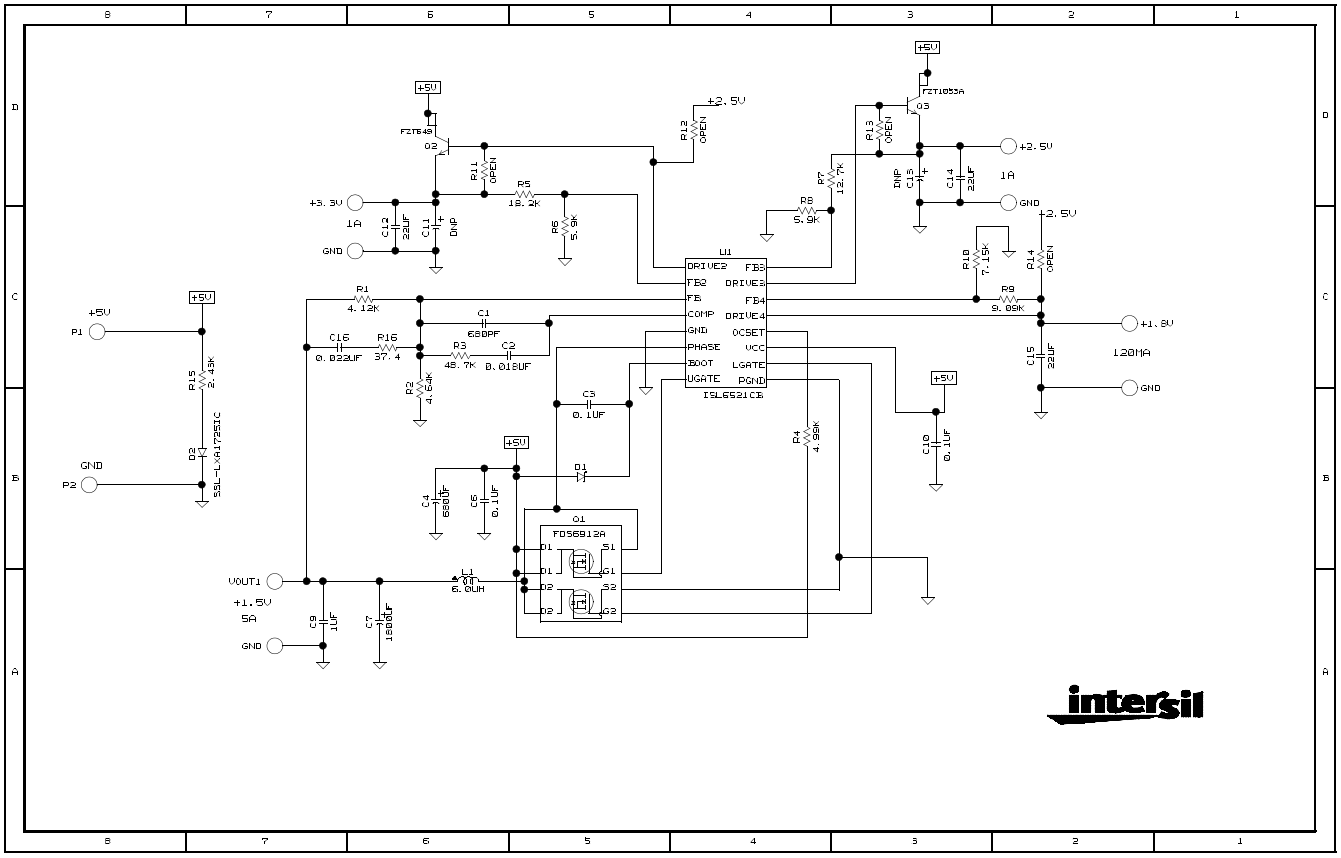
The ISL6521EVAL1 is an adaptable evaluation tool which showcases the performance of the ISL6521CB. Designed to meet the performance requirements of current FPGA applications, it allows the user the flexibility to configure it for future designs as well. The following pages provide a schematic of the board, bill of materials, and layout drawings to support implementation of this solution.

References

Intersil documents are available on the web at http://www.intersil.com/

[1] ISL6521 Data Sheet, Intersil Corporation, File No. FN9148

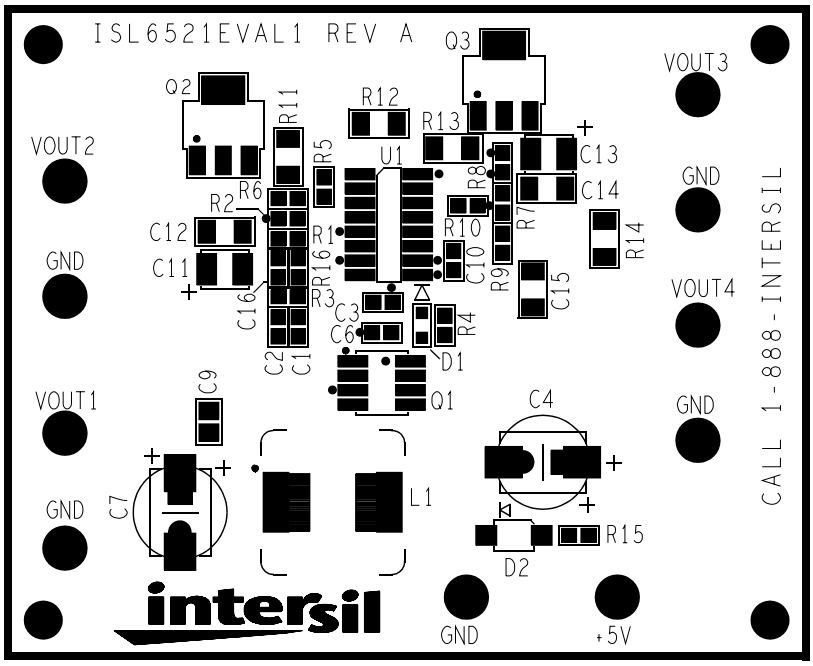
Schematic



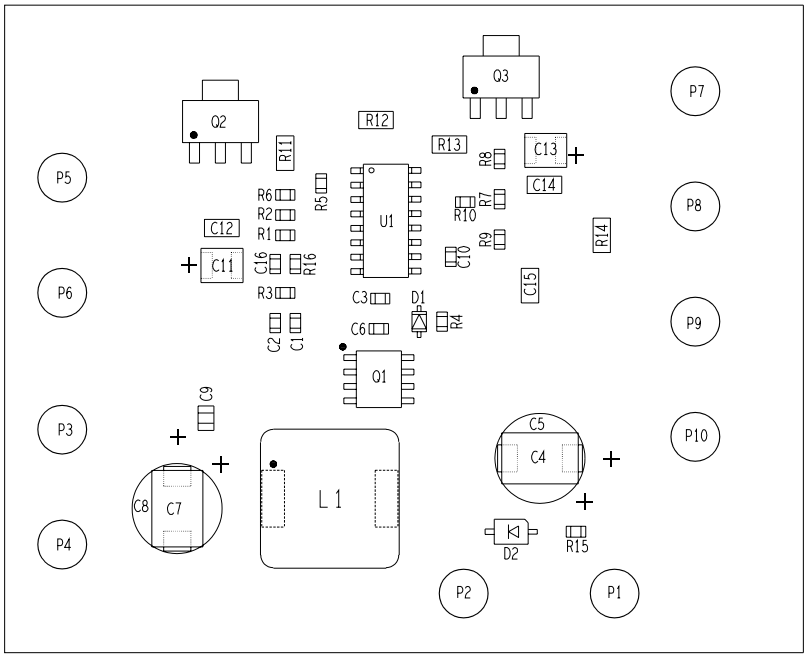
Bill of Materials

REFERENCE	PART NUMBER	DESCRIPTION	PACKAGE	VENDOR	QTY
U1	ISL6521CB	PWM Controller with Triple Linears	SO-8	Intersil	1
C1	ECU-V1H681KBV	680pF, 50V, X7R, 10%, Ceramic Capacitor	0603	Panasonic	1
C2	ECJ-1VB1H183K	0.018µF, 50V, X7R, 10%, Ceramic Capacitor	0603	Panasonic	1
C16	ECJ-1VB1H223K	0.022µF, 50V, X7R, 10%, Ceramic Capacitor	0603	Panasonic	1
C3	ECJ-1VBC104K	0.1µF, 16V, X7R, 10%, Ceramic Capacitor	0603	Panasonic	1
C4	EEUFC1A681L	680µF, 10V, Aluminum Electrolytic Capacitor	SMD	Panasonic	1
C6, C10	ECJ-1VB1C104K	0.1µF, X7R, 16V, 10%, Ceramic Capacitor	0603	Panasonic	2
C7	UHM0J182MPT6	1800µF, 5.3V, Special Polymer Aluminum Capacitor, 16mΩ ESR	SMD	Nichicon	1
C9	ECJ-1VB0J105K	1µF, X5R, 6.3V, 10%, Ceramic Capacitor	0805	Panasonic	1
C12, C14, C15	GRM31CR60J226KE19L	22µF, X5R, 6.3V, 10%, Ceramic Capacitor	1206	Murata	3
C5, C8, C11, C13		DNP, Ceramic Capacitor			
D1	MA732CT	Schottky Diode, 30V, 150mA	S-Mini	Panasonic	1
D2	SSL-LXA1725IC	LED 2X2.5MM Red Clear	SMD	Lumex	
L1	P1173.602T	6.0µH, 6.9A, Shielded Power Inductor	SMD	Pulse	1
Q1	FDS6912A	Dual N-Channel Power MOSFET, 24mΩ	SO-8	Fairchild	1
Q2, Q3	FZT649	NPN Transistor, 25V, 3A	SOT-223	Zetex	2
R1		Resistor, 4.12kΩ, 1%, 1/10W	0603	Various	1
R2		Resistor, 4.64kΩ, 1%, 1/10W	0603	Various	1
R3		Resistor, 48.7kΩ, 1%, 1/10W	0603	Various	1
R4		Resistor,4.99kΩ, 1%, 1/10W	0603	Various	1
R5		Resistor, 18.2kΩ, 1%, 1/10W	0603	Various	1
R6		Resistor, 5.9kΩ, 1%, 1/10W	0603	Various	1
R7		Resistor, 12.7kΩ, 1%, 1/10W	0603	Various	1
R8		Resistor, 5.9kΩ, 1%, 1/10W	0603	Various	1
R9		Resistor, 9.09kΩ, 1%, 1/10W	0603	Various	1
R10		Resistor, 7.15kΩ, 1%, 1/10W	0603	Various	1
R15		Resistor, 2.43kΩ, 1%, 1/10W	0603	Various	1
R16		Resistor, 37.4Ω, 1%, 1/10W	0603	Various	1
R11, R12, R13, R14		DNP Resistors, combine linears into one supply	1206	Various	
P1-P10	1514-2	Large Test Point	Thru Hole	Keystone	

ISL6521EVAL1 Layout

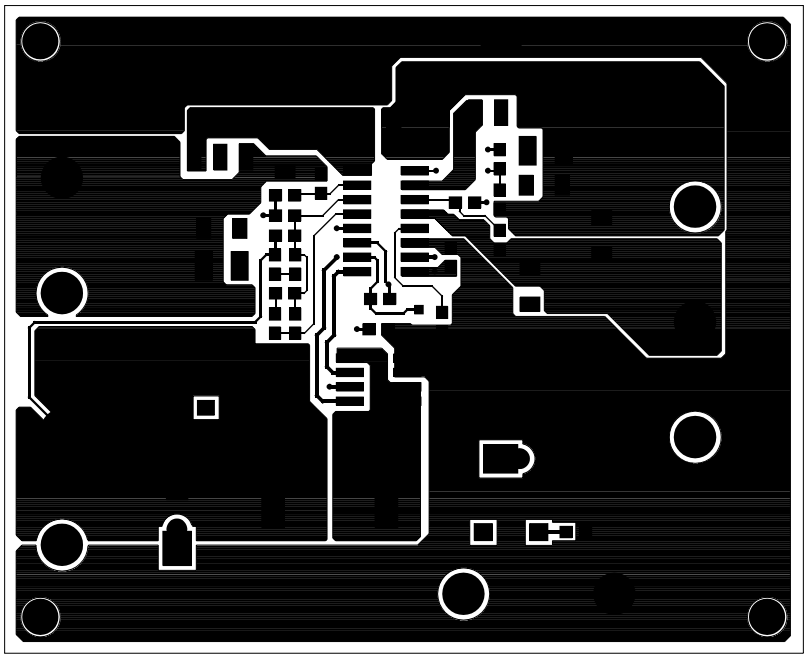


TOP SILK SCREEN

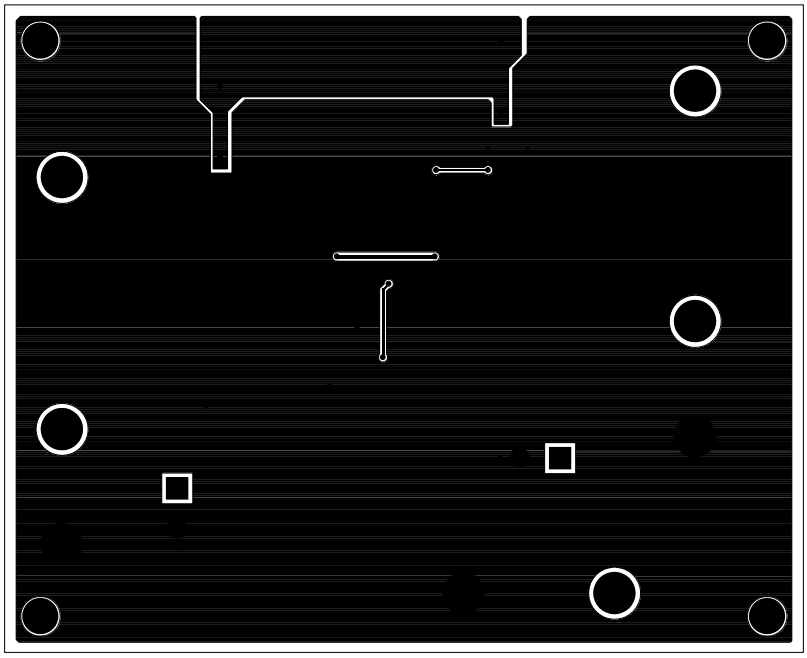


TOP ASSEMBLY

ISL6521EVAL1 Layout (Continued)



TOP LAYER



BOTTOM LAYER