

LM26484 Power Management Unit Evaluation Board Application Note

Application Manual

INTRODUCTION

The LM26484 evaluation board is a working demonstration of two step-down DC-DC converters and an LDO controller. This application note helps the user of the evaluation board make the best use of the LM26484 with their application. For more specific information about how the LM26484 device works as it relates to its electrical characteristics, please refer to the LM26484 datasheet.

The evaluation board comes with the regulators pre-configured to have VOUT Buck1 set to 1.8V, VOUT Buck2 set to 1.0V, and VOUT LDO set to 1.0V.

Because the LM26484 is externally configurable and has many voltage options, it is possible to change the feedback network to get a different regulator output voltage. Details are included in this document.

National Semiconductor
Application Note 1858
John Woodward
November 4, 2009



GENERAL DESCRIPTION

The LM26484 is a multi-function, configurable Power Management Unit. This device integrates two highly efficient 2.0A step-down DC/DC converters, one LDO Controller, a POR (Power On Reset) circuit, and thermal overload protection circuitry. All regulator output voltages are externally adjustable. The LDO controller is a low voltage NMOS voltage regulator. The LM26484 is offered in a 5 x 4 x 0.8 mm 24-pin LLP package.

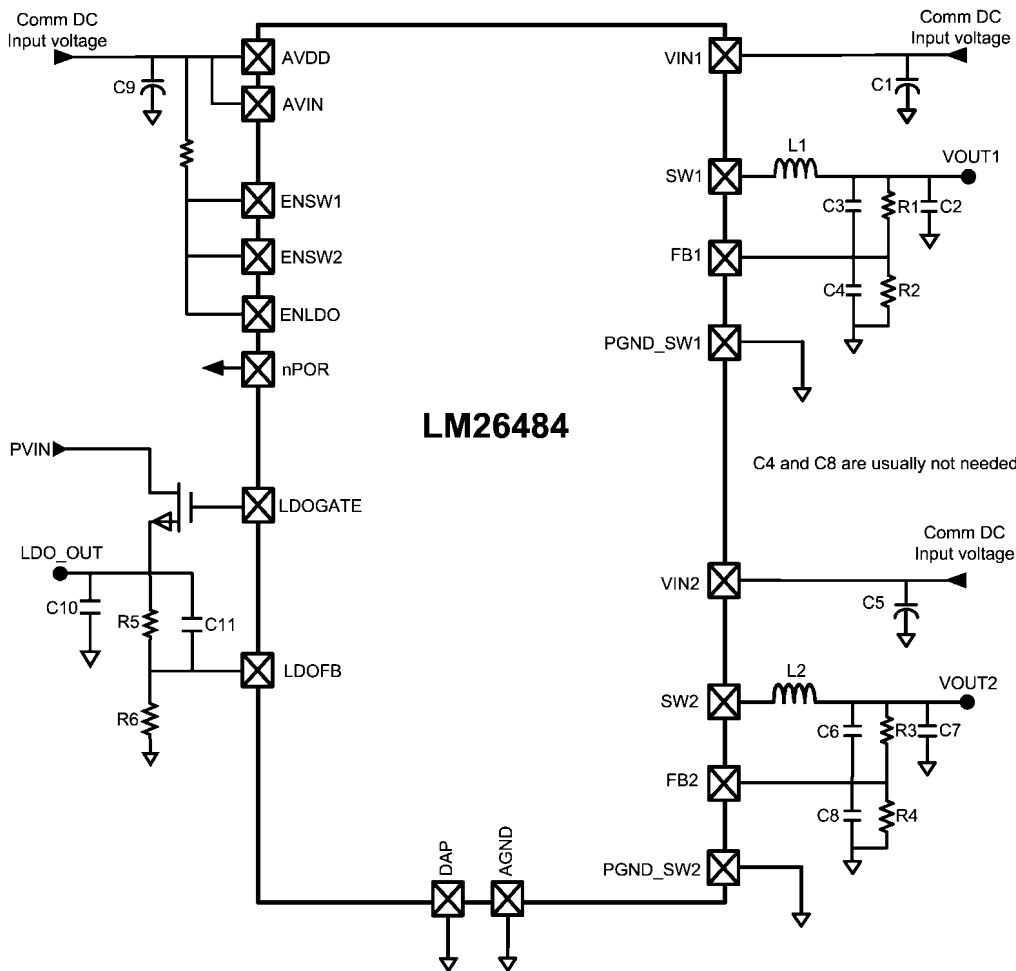
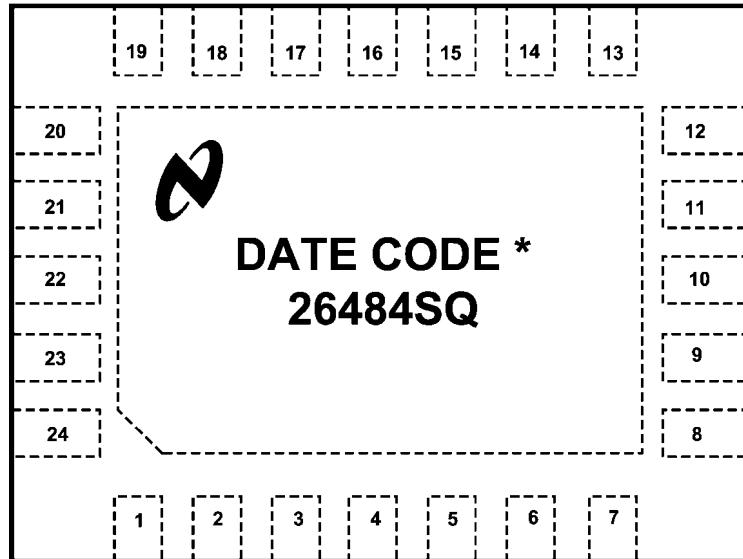


FIGURE 1. LM26484 Evaluation Board

30066001

Package Drawing of LM26484



30066002

Pin Descriptions

Pin #	Name	I/O	Type	Description
1	VIN1	I	PWR	Power in DC source Buck1 PMOS
2	ENSW1	I	D	Enable for Buck1 switcher, a logic HIGH enables Buck1
3	FB1	I	A	Buck1 feedback terminal
4	AVIN	I	PWR	Analog power for internal circuits
5	FB2	I	A	Buck2 feedback terminal
6	ENSW2	I	D	Enable for Buck2 switcher, a logic HIGH enables Buck2
7	VIN2	I	PWR	Power in DC source Buck2 PMOS
8	VIN2	I	PWR	Power in DC source Buck2 PMOS
9	SW2	O	A	Buck2 switcher output
10	SW2	O	A	Buck2 switcher output
11	PGND_SW2	G	G	Buck2 NMOS Power Ground
12	PGND_SW2	G	G	Buck2 NMOS Power Ground
13	ENLDO	I	D	Enable for LDO, a logic HIGH enables LDO
14	LDOGATE	O	A	LDO Controller output to NMOS power transistor Gate
15	LDOFB	I	A	LDO Controller input to feedback terminal
16	AGND	G	G	Analog GND
17	GND	G	G	Ground
18	nPOR	O	D	nPOR Active low Reset output. nPOR remains LOW while the input supply is below threshold, and goes HIGH after the threshold is reached and timed delay
19	AVDD	I	PWR	Analog Power Pin
20	PGND_SW1	G	G	Buck1 NMOS Power Ground
21	PGND_SW1	G	G	Buck1 NMOS Power Ground
22	SW1	O	A	Buck1 switcher output
23	SW1	O	A	Buck1 switcher output
24	VIN1	I	PWR	Power in DC source Buck1 PMOS
DAP	DAP	GND	GND	Connection isn't necessary for electrical performance, but it is recommended for better thermal dissipation.

A: Analog Pin **D:** Digital Pin **G:** Ground Pin **PWR:** Power Pin

Evaluation Board Description

From a common input voltage the user has access to two DC-DC step-down converters and one LDO controller. The output voltages of the two converters are configured via the feedback network which is external to the LM26484. From [Table 1](#), select the feedback network components that correlate to the desired output voltage and solder to the board.

It is very important to clean the board after assembly of the feedback network. The FB pin is a high impedance node, and any leakage caused by the flux remaining on the board could cause errors in the output voltage.

TABLE 1. Buck1/2 Configuration and Component Selection Guide

Target $V_{OUT}(V)$	Ideal Resistor Values		Common R Values		Actual V_{OUT} with Com/R (V)	Actual V_{OUT} Delta from Target (V)	Feedback Capacitors	
	R1/R3 (K Ω)	R2/R4 (K Ω)	R1/R3 (K Ω)	R2/R4 (K Ω)			C3/C6 (pF)	C4/C8 (pF)
0.8	120	200	121	200	0.803	0.002	15	none
0.9	160	200	162	200	0.905	0.005	15	none
1	200	200	200	200	1	0	15	none
1.1	240	200	240	200	1.1	0	15	none
1.2	280	200	280	200	1.2	0	12	none
1.3	320	200	324	200	1.31	0.01	12	none
1.4	360	200	357	200	1.393	-0.008	10	none
1.5	400	200	402	200	1.505	0.005	10	none
1.6	440	200	442	200	1.605	0.005	8.2	none
1.7	427	178	432	178	1.713	0.013	8.2	none
1.8	463	178	464	178	1.803	0.003	8.2	none
1.9	498	178	499	178	1.902	0.002	8.2	none
2	450	150	453	150	2.01	0.01	8.2	none
2.1	480	150	475	150	2.083	-0.017	8.2	none
2.2	422	124	422	124	2.202	0.002	8.2	none
2.3	446	124	442	124	2.282	-0.018	8.2	none
2.4	471	124	475	124	2.415	0.015	8.2	none
2.5	400	100	402	100	2.51	0.01	8.2	none
2.6	420	100	422	100	2.61	0.01	8.2	none
2.7	440	100	442	100	2.71	0.01	8.2	33
2.8	460	100	464	100	2.82	0.02	8.2	33
2.9	480	100	475	100	2.875	-0.025	8.2	33
3	500	100	499	100	2.995	-0.005	6.8	33
3.1	520	100	523	100	3.115	0.015	6.8	33
3.2	540	100	536	100	3.18	-0.02	6.8	33
3.3	560	100	562	100	3.31	0.01	6.8	33
3.4	580	100	576	100	3.38	-0.02	6.8	33
3.5	600	100	604	100	3.52	0.02	6.8	33

LDO Controller

The LDO controller must have its feedback network assembled before proper operation as well. Select the components

from [Table 2](#) that correspond to the desired output voltage. Make sure to clean the board after soldering the feedback network for reasons described above.

TABLE 2. LDO Configuration and Component Selection Guide

Target V_{OUT} (V)	Ideal Resistor Values		Common R Values		Actual V_{OUT} with Com R (V)	Feedback Capacitor
	R5 (K Ω)	R6 (K Ω)	R5 (K Ω)	R6 (K Ω)		C11 (pF)
0.8	120	200	120	200	0.8	15
0.9	160	200	162	200	0.905	15
1	200	200	200	200	1	15
1.1	240	200	240	200	1.1	15
1.2	280	200	280	200	1.2	12
1.3	320	200	324	200	1.31	12
1.4	360	200	357	200	1.393	10
1.5	400	200	402	200	1.505	10

Jumper Settings

In order for the board to function properly there are certain jumpers that must be in place. Please refer to for jumper descriptions.

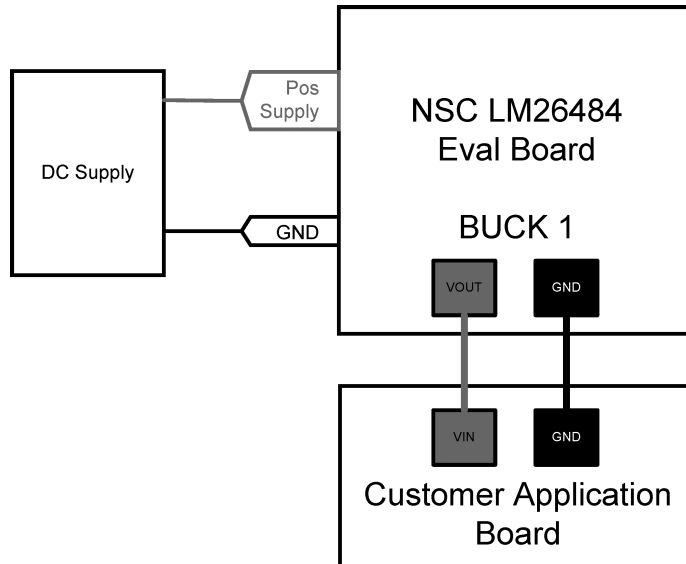
TABLE 3. Jumper Descriptions

JP1	Must be in place	Connects Vin1 to board power
JP2	Must be in place	Connects Vin2 to board power
JP3	Must be in place	Connects AVDD to board power
JP4	Must be in place	Connects AVIN to board power
JP5	Must be in place	This alternates between GND and board power to enable Buck2
JP6	Must be in place	This alternates between GND and board power to enable Buck1
JP7	Must be in place	This alternates between GND and board power to enable the LDO
JP9	Must be in place	Connects GND to board GND
JP10	Optional	Changes the output voltage of Buck2
JP11	Optional	Changes the output voltage of the LDO
JP12	Optional	Changes the output voltage of Buck1
JP14	Must be in place	Alternates the FET Drain voltage between Buck 2 and board power

Using Evaluation Board to Supply Power

It is important to connect the LM26484 Buck and LDO using proper ground returns. This will enable the output voltage to

be as clean as possible. As seen below, connect each V_{OUT} and its corresponding ground to the input and ground on the application board. Each LM26484 Buck output has a ground associated with it, and its ground needs to be connected for proper ground current flow.

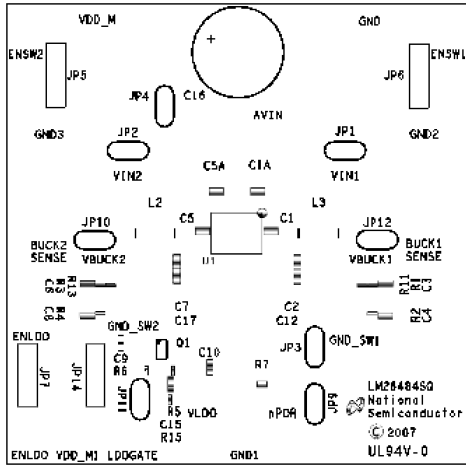


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Bill of Materials

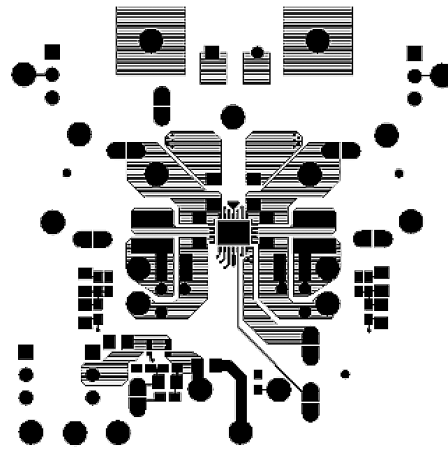
Item	Designator	Vendor	Part Number	Qty.	Comp. Type	Value
1		NSC	551600140-001	1	LM26484SQ Eval Board PCB, Rev A	
2	U1	NSC	LM26484SQ	1		
3	C1, C1A, C2, C5, C5A, C7, C12, C17	Taiyo Yuden	JMK316B7226ML-T	8	CAP CER 22 μ F 6.3V X7R 1206	22 μ F
4	C9, C10, C11, C14	Murata	GRM21BR71A106KE51L	4	CAP CER 10 μ F 10V X7R 0805	10 μ F
5	C3	Murata	ERB21B5C2E8R2CDX1L	1	CAP CER 8.2F 250V 0805	8.2 pF
6	C6,C15	Murata	ERB21B5C2E150JDX1L	2	CAP CER 15F 250V 0805	15 pF
7	C4, C8	NO LOAD	NO LOAD	5	NO LOAD	
8	C16	Murata	GRM32ER61A476KE20L	1	CAP CER 47 μ F 10V X5R 1210	47 μ F
9	L2, L3	Coilcraft	LPS4414-501MLB	2	LPS4414 Series Low Profile Shielded Power Inductors	0.5 μ H
10	Q1	Vishay	SI1450DH	1	MOSFET N-CH 20V 1.6A SOT-363	20V, 1.6A
11	R2	Panasonic	ERJ-3EKF1783V	1	RES 178 k Ω 1/10W 1% 0603 SMD	178K
12	R1	Panasonic	ERJ-3EKF4643V	1	RES 464 k Ω 1/10W 1% 0603 SMD	464K
13	R3, R4, R5, R6	Panasonic	ERJ-3EKF2003V	4	RES 200 k Ω 1/10W 1% 0603 SMD	200K
14	R11, R13, R15	NO LOAD	NO LOAD	9	NO LOAD	
15	R7	Panasonic	ERJ-3EKF1003V	1	RES 100 k Ω 1/10W 1% 0603 SMD	100K
16	JP1, JP2, JP3, JP4, JP9	Tyco/AMP	9-146285-0-02	5	2-pin header 100 mil pitch	
17	JP10, JP11, JP12	NO LOAD	NO LOAD	3	NO LOAD	
18	JP5, JP6, JP7, JP14	Tyco/AMP	9-146285-0-03	4	3-pin header 100 mil pitch	
19	AVIN, BUCK1_SENSE, BUCK2_SENSE, ENLDO, ENSW1, ENSW2, GND, GND1, GND2, GND3, GND_SW1, GND_SW2, LDOGATE, NPOR, VBUCK1, VBUCK2, VDD_M, VDD_M1, VIN1, VIN2, VLDO	Keystone	1573-2	21	silver plated turret 70 mil drill	
20	JP1_SH, JP2_SH, JP3_SH, JP4_SH, JP5_SH, JP6_SH, JP7_SH, JP9_SH, JP14_SH	Tyco/AMP	881545-2	9	Jumper Shunt, 0.100" 30 uin AU (with handle)	

LM26484 Board Layout



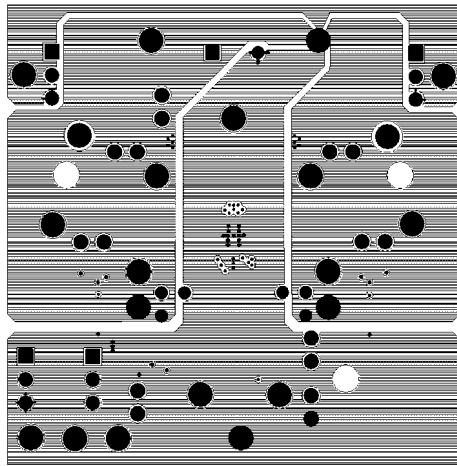
Silkscreen Top

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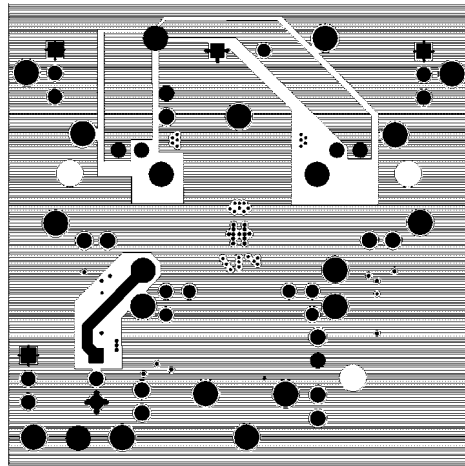
Signal Top Layer

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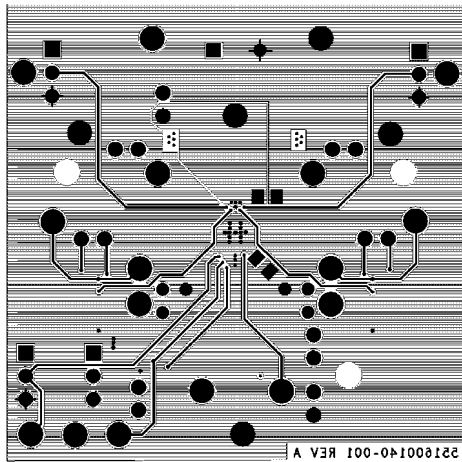
Signal Plane Ground

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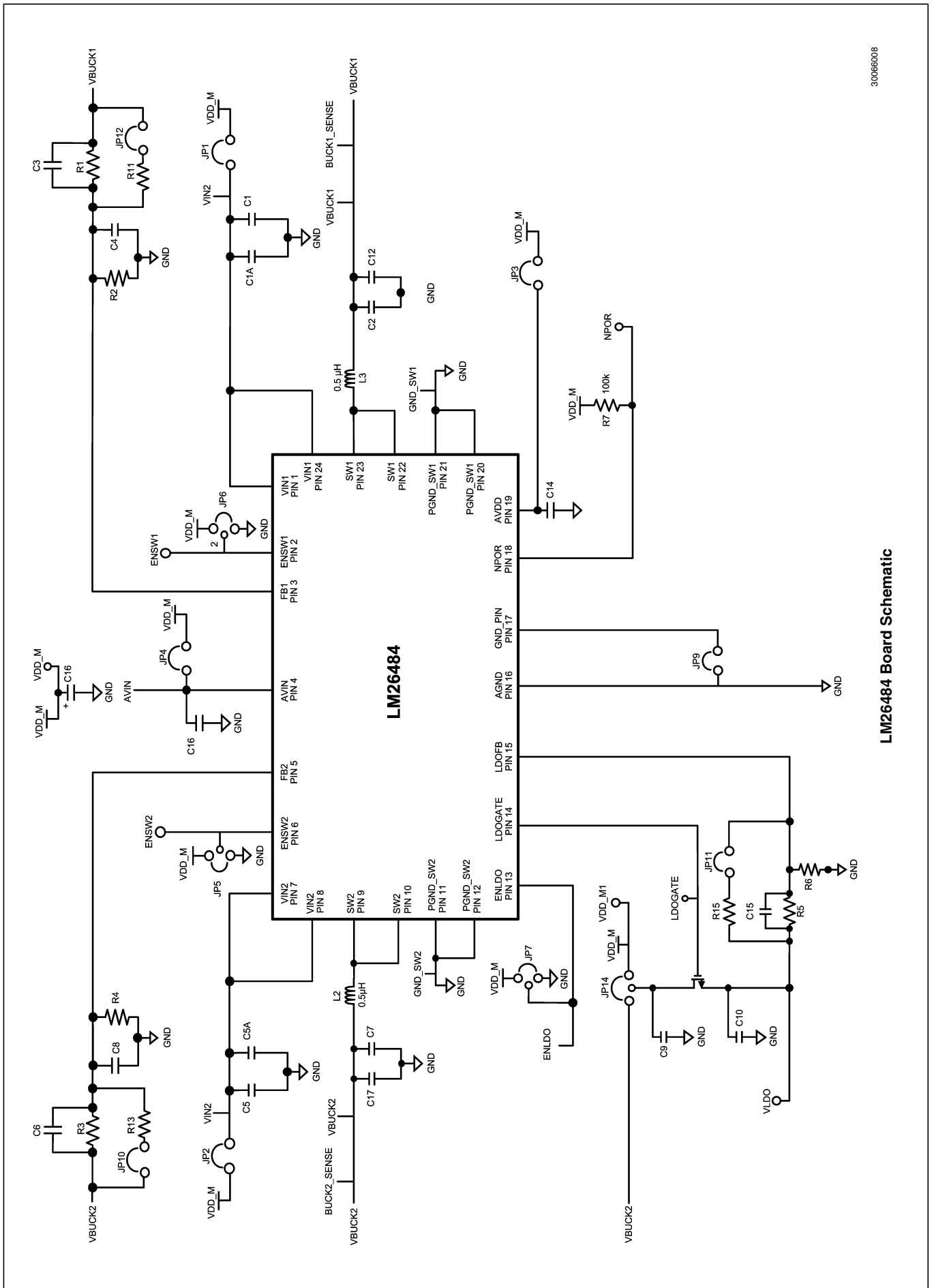
Signal Plan VDD_M (Board Power)

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Signal 4 Bottom

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LM26484 Board Schematic

Notes

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