LM3205 Evaluation Board

National Semiconductor
Application Note 1413
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Introduction

The LM3205 evaluation board is a working demonstration of a step down DC-DC converter. This application note contains information about the evaluation board and board layout considerations. For further information on buck converter topology, device electrical characteristics, and component selection please refer to the LM3205 datasheet.

General Description

The LM3205 is a DC-DC converter optimized for powering RF power amplifiers (RFPAs) from a single Lithium-Ion cell, however the device may be used in many other applications. The LM3205 steps down an input voltage range from 2.7V to 5.5V to a variable output voltage range from 0.8V to 3.6V. Output voltage is set using a V_{CON} analog input for controlling power levels and efficiency of the RFPA.

The LM3205 offers superior performance for mobile phones and similar RFPA applications. Fixed-frequency PWM operation minimizes RF interference. Shutdown function turns the device off and reduces battery consumption to 0.01 µA (typ).

The LM3205 is available in a 8-pin lead free micro SMD package. A high switching frequency (2 MHz) allows use of tiny surface-mount components. Only three small external components are required, an inductor and two ceramic capacitors.

Operating Conditions

- V_{IN} range: 2.7V ≤ V_{IN} ≤ 5.5V
- V_{CON} range: 0.32V ≤ V_{CON} ≤ 1.44V
- V_{OUT} equation: V_{OUT} = 2.5 x V_{CON}
- I_{OUT} range: 0 mA≤ I_{OUT} ≤ 650 mA

Typical Application

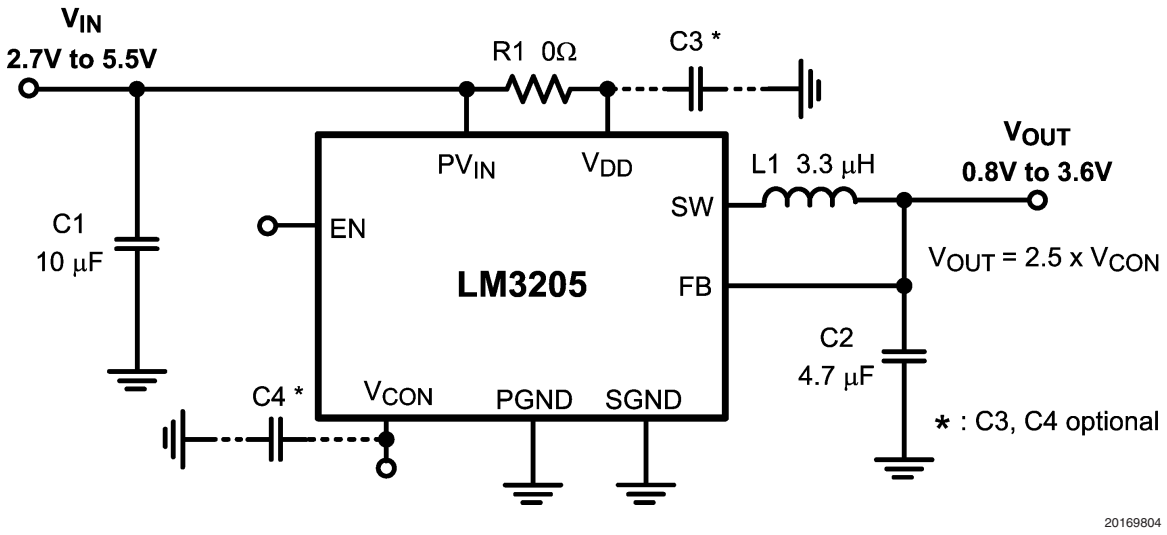

FIGURE 1. Typical Application Circuit

Evaluation Board Layout

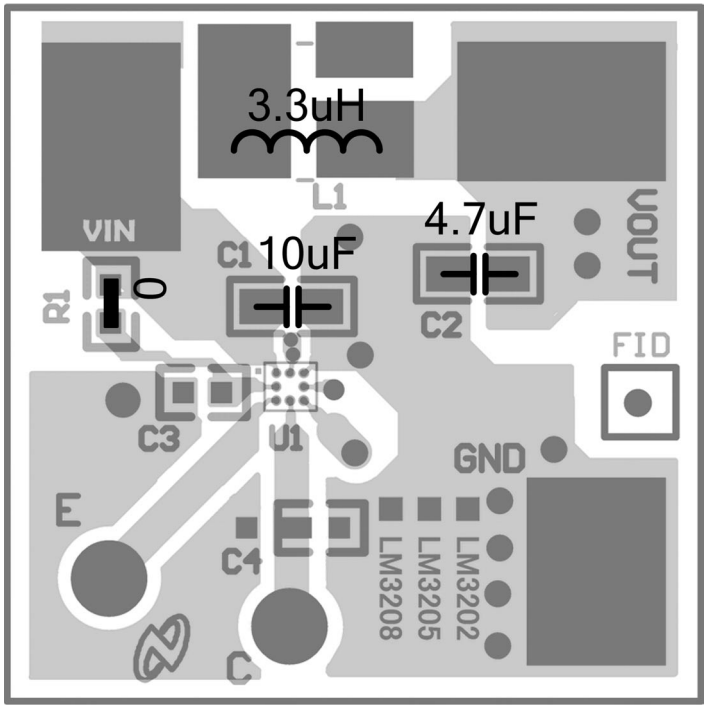

FIGURE 2. Top Layer

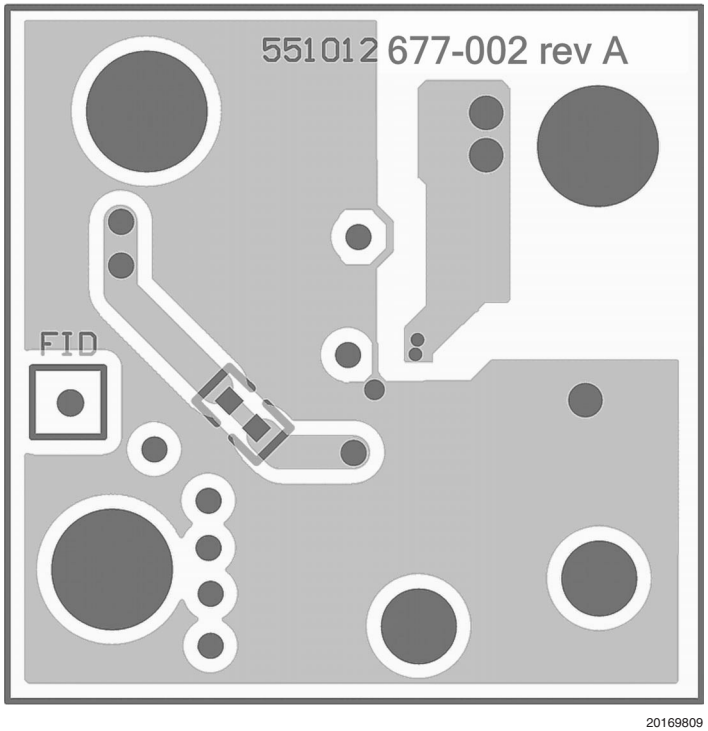

FIGURE 3. Bottom Layer

Connection Diagram and Package Mark Information

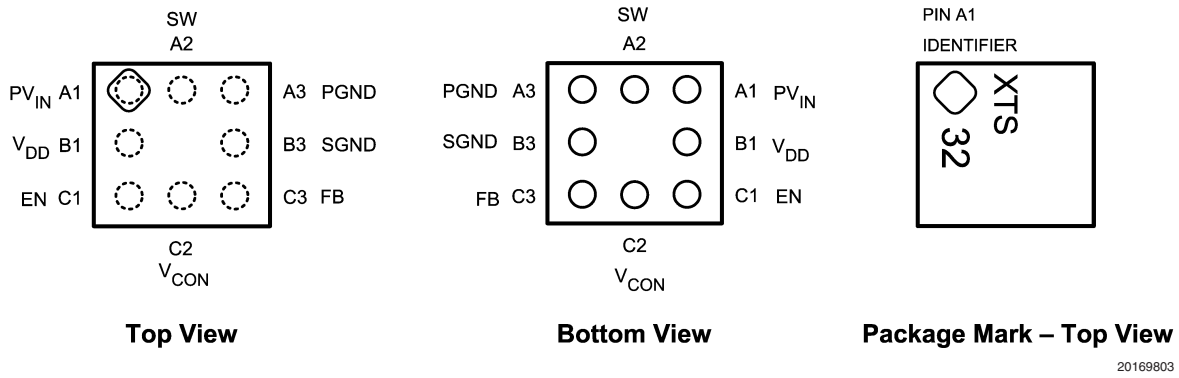

FIGURE 4.
8–Bump Thin Micro SMD Package, Large Bump
NS Package Number TLA08GNA

Pin Descriptions

Pin #	Name	Description
A1	PV_{IN}	Power Supply Voltage Input to the internal PFET switch.
B1	V_{DD}	Analog Supply Input.
C1	EN	Enable Input. Set this digital input high for normal operation. For shutdown, set low.
C2	V_{CON}	Voltage Control Analog input. V_{CON} controls V_{OUT} in PWM mode.
C3	FB	Feedback Analog Input. Connect to the output at the output filter capacitor.
B3	SGND	Analog and Control Ground
A3	PGND	Power Ground
A2	SW	Switch node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the LM3205.

BOM For Common Configurations

	Manufacture	Manufacture #	Description
C1 (input C)	TDK	C2012X5R0J106M	10 µF,6.3V,20%,0805
C2 (output C)	TDK	C1608X5R0J475M	4.7 µF,6.3V,20%,0603
C3 (optional, input C)			0.1 µF,25V , 0402(Note 1)
C4 (optional, filter for V_{CON})			10 - 100 pF, 25V , 0402(Note 1)
L1 (inductor)	Taiyo-Yuden	NR3015T3R3M	3.3 µH, 1210mA, 3x3x1.5 mm
R1 (jumper PV_{IN} to V_{DD})	Vishay	CRCW04020R00F	0Ω, 0402
V_{IN} banana jack - red	Johnson Components	108-0902-001	connector, insulated banana jack (red)
V_{out} banana jack - yellow	Johnson Components	108-0907-001	connector, insulated banana jack (yellow)
GND banana jack - black	Johnson Components	108-0903-001	connector, insulated banana jack (black)

Note 1: C3 and C4 are recommended for a better noise performance.

Board Layout Considerations

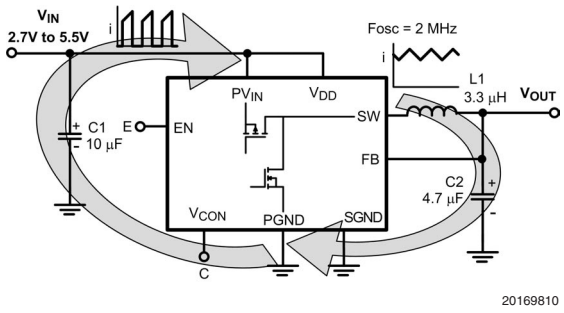

FIGURE 5. Current Loop

The LM3205 converts higher input voltage to lower output voltage with high efficiency. This is achieved with an inductor-based switching topology. During the first half of the switching cycle, the internal PMOS switch turns on and the input voltage is applied to the inductor in which the current flows from P_{VDD} line to the output capacitor (C2) through the inductor. During the second half cycle, the PMOS turns off and the internal NMOS turns on. The inductor current continues to flow via the inductor from the device PGND line to the output capacitor (C2) .

Referring to *Figure 5*, the LM3205 has two major current loops where pulse and ripple current flow. The loop shown in the left hand side is important because pulse current flows in this path. In the loop on the right hand side, the current waveform in this path is triangular. Pulse current has many high-frequency components due to fast di/dt. Triangular ripple current also has wide high-frequency components. Board layout and circuit pattern design of these two loops are key factors for reducing noise radiation and achieiving stable operation. Other lines, such as input and output terminals are DC current, therefore pattern width (current capability) and DCR drop considerations are needed.

BOARD LAYOUT FLOW

1. Minimize C1, PV_{IN}, and PGND loop. These traces should be as wide and short as possible.
2. Minimize L1, C2, SW and PGND loop. These traces also should be as wide and short as possible.
3. The layout patterns should be placed on the component side of the PCB to minimize parasitic inductance and resistance due to via-holes. SW to L1 path should be routed between C2(+) and C2(-) land patterns. If vias are used in these large current paths, multiple via-holes should be used if possible.
4. Connect C1(-), C2(-) and PGND with wide GND pattern. This pattern should be short, so C1(-), C2(-), and PGND are as close as possible. Then connect to a PCB common GND pattern with as many via-holes as possible.
5. SGND should not be connect directly to PGND. Connecting these pins under the device should be avoided. (If possible, connect SGND to the common port of C1(-), C2(-) and PGND.)
6. V_{DD} should not be connected directly to PV_{IN}. Connecting these pins under the device should be avoided. It is recommended to connect V_{DD} to the C1(+) to avoid switching noise injection to the V_{DD} line.
7. FB line should be protected from noise. It is recommended to use an inner GND layer (if available) as a shield.

Note: The evaluation board shown in *Figure 2* and *Figure 3* for the LM3205 was designed with the considerations mentioned above, and it shows good performance. However some aspects have not been optimized because of limitations due to evaluation-specific requirements. The board can be used as a reference. For specific questions, please refer to a National representative.

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