Using the ISL8105BEVAL1Z, ISL8105BEVAL2Z PWM Controller Evaluation Board

Application Note | October 30, 2008 | AN1288.1

Introduction

The ISL8105B is a simple single-phase PWM controller for a synchronous buck converter that operates from +5V or +12V bias supply voltage. With integrated linear regulator, boot diode, and gate drivers, the ISL8105B reduces external component count and board space requirements.

The ISL8105BEVAL1Z, ISL8105BEVAL2Z evaluation board highlights the operations of the controller in a DC/DC application.

ISL8105BEVAL1Z , ISL8105BEVAL2Z Reference Design

The ISL8105BEVAL1Z, ISL8105BEVAL2Z evaluation board is designed to optimize for the output voltage and current specifications shown in Table 1.

TABLE 1. ISL8105BEVAL1Z, ISL8105BEVAL2Z EVALUATION BOARD DESIGN PARAMETERS

PARAMETER	MIN	TYP	MAX
Input Voltage (V_{IN})	9.6V	12V	14.4V
Output Voltage (V_{OUT})		1.8V	
Output Voltage Ripple (V_{RIPPLE})		30mV_{P-P}	
Continuous Load Current			15A
Efficiency		90	

Two versions of the evaluation board, based on the package type, are listed in Table 2.

TABLE 2. EVALUATION BOARDS

BOARD NAME	IC	PACKAGE
ISL8105BEVAL1Z	ISL8105BIBZ	8 Ld SOIC
ISL8105BEVAL2Z	ISL8105BIRZ	10 Ld DFN

Design Procedure

The following sections illustrate simple design steps and component selections for a converter using the ISL8105BEVAL1Z, ISL8105BEVAL2Z.

Output Inductor Selection

The output inductor is chosen by the desired inductor ripple current, which is typically set to be approximately 40% of the rated output current. The desired output inductor can be calculated using Equation 1:

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{SW}} = \frac{14.4 - 1.8}{0.4 \cdot 15} \times \frac{1.8}{14.4} \times \frac{1}{300 \times 10^3} = 0.875\mu H \quad \text{(EQ. 1)}$$

In the evaluation board, a 1µH inductor with 1.87mΩ DCR (Cooper Bussmmann's HC9-1R0-R) is employed. This yields approximately 0.44W conduction loss in the inductor.

Output Capacitor Selection

The output capacitors are generally selected by the output voltage ripple and load transient response requirements. ESR and capacitor charge are major contributions to the output voltage ripple. Assuming that the total output capacitance is sufficient, then the output voltage ripple is dominated by the ESR, which can be calculated using Equation 2.

$$V_{RIPPLE} = \Delta I_L \cdot ESR \quad \text{(EQ. 2)}$$

To meet the 30mV_{P-P} output voltage ripple requirement, the effective ESR should be less than 5mΩ.

The output voltage response to a transient load is contributed from ESL, ESR and the amount of output capacitance. With V_{IN}>>V_{OUT}, the amplitude of the voltage excursions can be approximated using Equation 3:

$$\Delta V = \frac{L \cdot I_{tran}^2}{C_{OUT} \cdot V_{OUT}} \quad \text{(EQ. 3)}$$

With 1µH inductor and 0A to 15A step load, the total output capacitance of 1560µF is required for 80mV output voltage transient. In the ISL8105BEVAL1Z, ISL8105BEVAL2Z evaluation board, four of Sanyo's 2R5TPF470ML are employed.

Input Capacitor Selection

The input bulk capacitors selection criteria are based on the capacitance and RMS current capability. The RMS current rating requirement for the input capacitor is approximated in Equation 4:

$$I_{IN,RMS} = \sqrt{I_O^2(D - D^2) + \frac{\Delta I^2}{12}D} \qquad D = \frac{V_O}{VIN} \quad \text{(EQ. 4)}$$

In this application, the RMS current for the input capacitors is 5.4A; therefore, three of Sanyo's 35ME330AX are used.

Small ceramic capacitors for high frequency decoupling are also required to control the voltage overshoot across the MOSFETs.

MOSFET Selection

The ISL8105B requires two N-Channel power MOSFETs as the main and the synchronous switches. These should be selected based in $r_{DS(ON)}$, gate supply requirements and thermal management requirements.

The total power loss in MOSFET consists of conduction loss and switching loss, as shown in Equation 5:

$$P_{MOSFET(TOT)} = P_{cond} + P_{sw} \quad \text{(EQ. 5)}$$

In this relatively small duty cycle design, the low-side MOSFET conducts current most of the time. To optimize the converter efficiency, select the high-side MOSFET with low gate charge for fast switching transition and low-side MOSFET with low $r_{DS(ON)}$.

To achieve the target efficiency, the budget power losses in high-side and low-side MOSFETs are 0.5W and 1W, respectively.

LOW-SIDE MOSFET SELECTION

The low-side MOSFET's RMS current is approximated in Equation 6:

$$I_{L(RMS)} = I_{OUT} \cdot \sqrt{1-D} \cdot \sqrt{1 + \frac{1}{12} \cdot \left(\frac{\Delta I_L}{I_{OUT}}\right)^2} \approx 13.9A \quad \text{(EQ. 6)}$$

Therefore, the ON-resistance of the low-side MOSFET must be less than 5mΩ. Infineon's BSC030N03LS is employed in the ISL8105BEVAL1Z, ISL8105BEVAL2Z evaluation board. The conduction loss in the low-side MOSFET is calculated using Equation 7:

$$P_{LFET(cond)} = I^2_{L(RMS)} \cdot r_{DS(ON)}\Big|_{LFET} = 0.58W \quad \text{(EQ. 7)}$$

The switching loss in the low-side MOSFET is dominated by the loss in body diode which can be calculated using Equation 8:

$$P_{diode} = I_O \cdot t_D \cdot V_F \cdot F_{SW} = 0.3W \quad \text{(EQ. 8)}$$

Where t_D is the total dead time in each switching period (~60µs) and V_F is the forward voltage drop of MOSFET's body diode.

The total power dissipation in the low-side MOSFET is calculated using Equation 9:

$$P_{LFET(TOT)} = 0.88W \quad \text{(EQ. 9)}$$

HIGH-SIDE MOSFET SELECTION

For the high-side MOSFET selection, first we assume that the conduction loss and the switching loss contribute evenly to the total power dissipation.

The high-side MOSFET's RMS current is approximated using Equation 10:

$$I_{H(rms)} = I_{OUT} \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{12} \cdot \left(\frac{\Delta I_L}{I_{OUT}}\right)^2} \approx 5.85A \quad \text{(EQ. 10)}$$

Hence, the required ON-resistance of the high-side MOSFET is 7.3mΩ. Infineon's BSC080N03LS is selected. The conduction loss in the high-side MOSFET is calculated using Equation 11:

$$P_{HFET(cond)} = I^2_{H(RMS)} \cdot r_{DS(ON)}\Big|_{HFET} = 0.27W \quad \text{(EQ. 11)}$$

The switching loss in the high-side MOSFET can be approximated using Equation 12:

$$P_{HFET(SW)} = \frac{1}{2} \cdot I_O \cdot V_{IN} \cdot t_{tr} \cdot F_{SW} + \frac{1}{2} \cdot C_{OSS} \cdot V^2_{IN} \cdot F_{SW} = 0.17W \quad \text{(EQ. 12)}$$

where t_{tr} is the combined ON and OFF MOSFET transition times.

The total power dissipation in high-side MOSFET is shown in Equation 13:

$$P_{HFET(TOT)} = 0.44W \quad \text{(EQ. 13)}$$

Overcurrent Protection Setting

The overcurrent function protects the converter from a shorted output by using the low-side MOSFET's $r_{DS(ON)}$ to monitor the current. A resistor, R_{BSOC}, programs the overcurrent trip level. If overcurrent is detected, the output immediately shuts off, it cycles the soft-start function in a hiccup mode (2 dummy soft-start time-outs, then up to one real one) to provide fault protection. If the shorted condition is not removed, this cycle will continue indefinitely.

The overcurrent function will trip at a inductor current (I_{trip}) is determined using Equation 14:

$$I_{trip} = \frac{2 \bullet I_{OCSET} \bullet R_{BSOC}}{r_{DS(ON)}} \quad \text{(EQ. 14)}$$

where I_{OCSET} is the internal 21.5µA (typ.) OCSET current source.

The OC trip point varies mainly due to the MOSFET's $r_{DS(ON)}$ variations. To avoid overcurrent tripping in the normal operating load range, calculate the R_{BSOC} resistor from Equation 14 using:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature.
2. The minimum I_{OCSET} from the specification table of the datasheet.

Determine I_{trip} for $I_{trip} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

With Infineon's BSC030N03LS as the low-side MOSFET and R_{BSOC} of 1.74kΩ. The overcurrent trip point on the evaluation board has been set to 21A for 12V_{BIAS} (17A for 5V_{BIAS}).

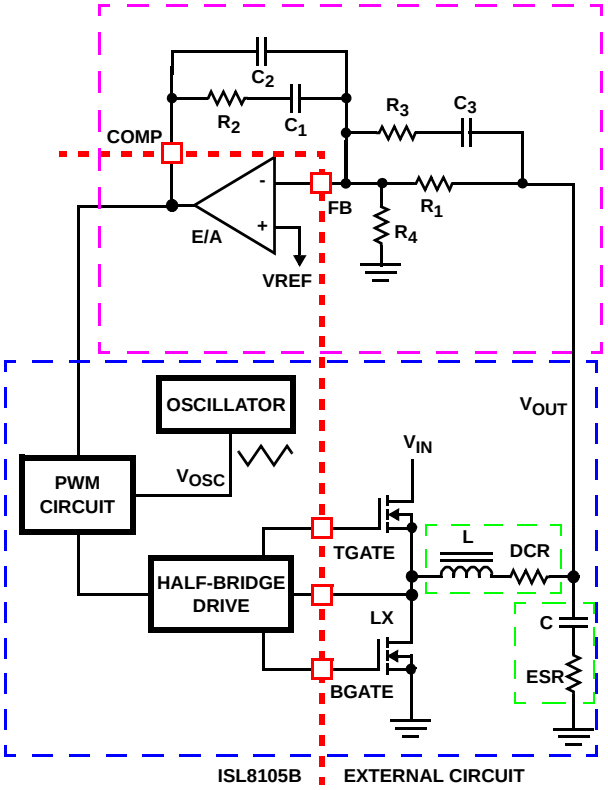


FIGURE 1. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

Feedback Compensator

Type-III network is recommended for compensating the feedback loop. Figure 1 shows Type-III compensation configuration for ISL8105B.

With the inductor and output capacitor selected as described in the previous sections, the poles and zero of the power stage can be summarized in Equation 15:

$$F_0 = \frac{1}{2\times\pi\times\sqrt{L\times C}} = 3.7\text{kHz}$$
$$F_{ESR} = \frac{1}{2\times\pi\times C\times ESR} = 33.9\text{kHz} \quad \text{(EQ. 15)}$$

1. With a value of 11.8kΩ for R_1, select R_4 for the target output voltage of 1.8V using Equation 16:

$$R_4 = R_1\times\frac{V_{ref}}{V_{OUT}-V_{ref}} = 5.9\text{k}\Omega \quad \text{(EQ. 16)}$$

2. With the desired feedback loop bandwidth of 30kHz, R_2 can be calculated using Equation 17:

$$R_2 = \frac{V_{OSC}\cdot R_1\cdot F_0}{d_{max}\cdot V_{IN}\cdot F_{LC}} = 12\text{k}\Omega \quad \text{(EQ. 17)}$$

3. Select C_1 such that F_{Z1} is located at 1.5kHz (~50% of F_{LC}):

$$C_1 = \frac{1}{2\pi\cdot R_2\cdot 1.5\times10^3} \approx 10\text{nF} \quad \text{(EQ. 18)}$$

4. Select C_2 such that F_{P1} is located at F_{ESR}:

$$C_2 = \frac{C_1}{2\pi\cdot R_2\cdot C_1\cdot F_{ESR}-1} \approx 390\text{pF} \quad \text{(EQ. 19)}$$

5. Select R_3 such that F_{Z2} is located at F_{LC}:

$$R_3 = \frac{R_1}{\frac{150\times10^3}{F_{LC}}-1} \approx 301\Omega$$
$$C_3 = \frac{1}{2\pi\cdot R_3\cdot 150\times10^3} \approx 3.3\text{nF} \quad \text{(EQ. 20)}$$

A more detailed explanation of designing compensation networks for buck converters with voltage mode control can be found in TB417 entitled "Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators".

Evaluation Board Performance

Figure 2 shows a photograph of the ISL8105BEVAL1Z.

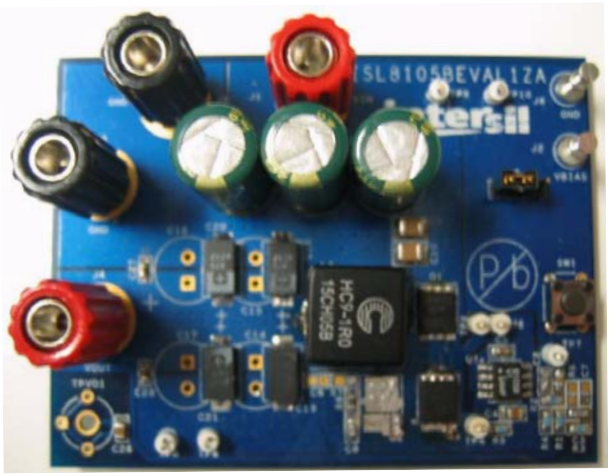


FIGURE 2. ISL8105BEVAL1Z

Power and Load Connections

Terminals J1 and J2 are connected to the input of the power stage. The IC bias supply and the converter input supply can be together through pin 2 and 3 of the Jumper J7 to provide single rail supply application. When using separate supplies, provide the IC bias voltage to terminal J2 with pin 2 and pin 1 of J7 connected together. The load can be connected to terminal J4 and J5. TP6 and TP3 can be used for DMM to measure output voltage. The scope probe terminal (TPV01) can be used to monitor V_{OUT} with an oscilloscope. The push switch, SW1, can be used to disable the controller.

Start-up

The ISL8105B starts up when V_{BIAS} rises above POR threshold and the COMP/EN rises above $V_{DISABLE}$ level. The entire start-up time sequence from POR typically takes up to 23.8ms; up to 10.2ms for the delay and the Overcurrent Protection (OCP) sample and hold operation. The initial delay is added to allow the bias voltage to rise/exceed 6.5V, so that the internal bias regulator can turn on cleanly. When the OCP sampling and hold operations are done, the soft-start function internally ramps the reference on the non-inverting terminal of the error amp from 0V to 0.6V in 13.6ms (typ).

Figure 3 shows the start-up profile of the ISL8105BEVAL1Z, ISL8105BEVAL2Z in relation to the start-up of the 12V input supply and the bias supply.

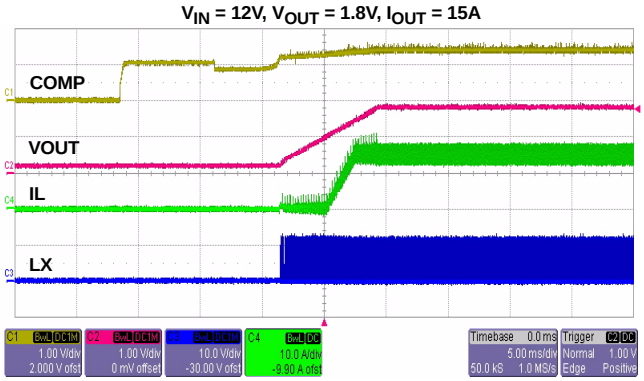


FIGURE 3. SOFT-START

Soft-Start with Pre-Biased Output

If the output is pre-biased to a voltage less than the expected value, the ISL8105BEVAL1Z, ISL8105BEVAL2Z will detect that condition. Neither MOSFETs will turn on until the soft-start ramp voltage exceeds the FB voltage; V_{OUT} starts seamlessly ramping from there.

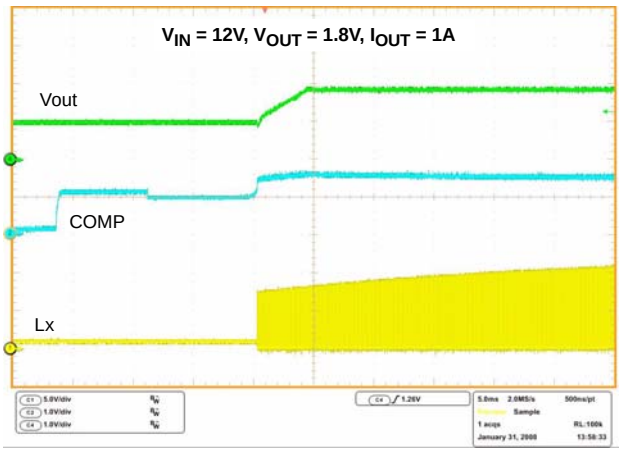


FIGURE 4. SOFT-START WITH PRE-BIASED OUTPUT

Output Ripple

Figure 5 shows the ripple voltage on the output of the regulator.

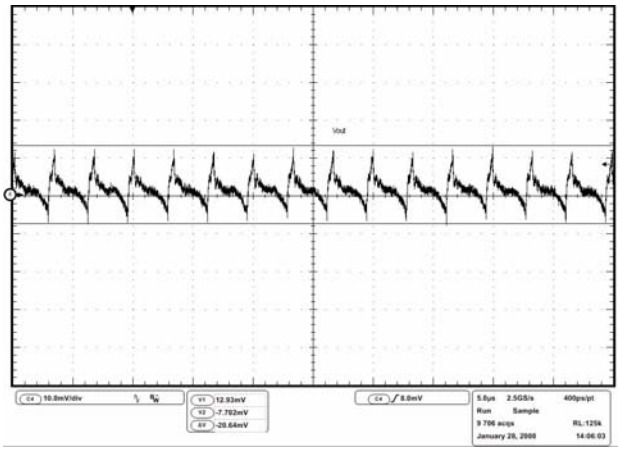


FIGURE 5. OUTPUT RIPPLE (20MHz BW)

Verifying Loop Gain

Figure 6 shows the measurement of loop gain of the converter with feedback network design in the previous sections.

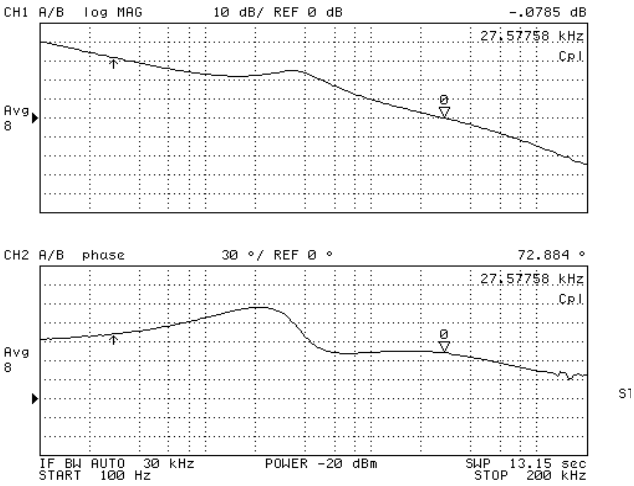


FIGURE 6. LOOP GAIN MEASUREMENT AT +25°C

Transient Performance

Figures 7, 8, and 9 show the response of the output when subjected to transient loading from 0A to 15A at 1A/µs.

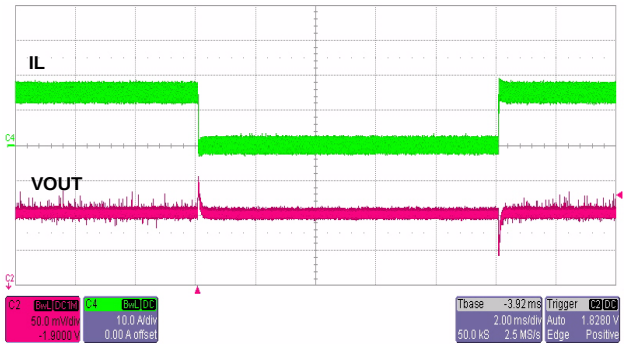


FIGURE 7. TRANSIENT RESPONSE

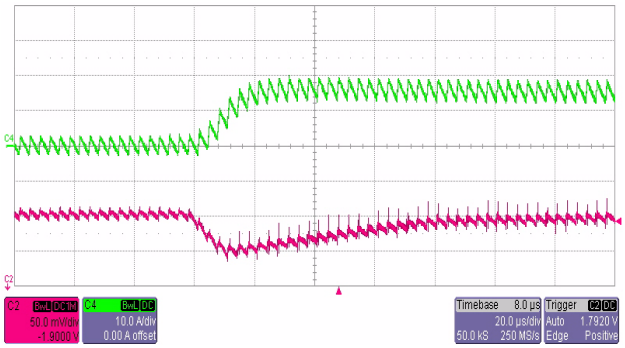


FIGURE 8. TRANSIENT RESPONSE

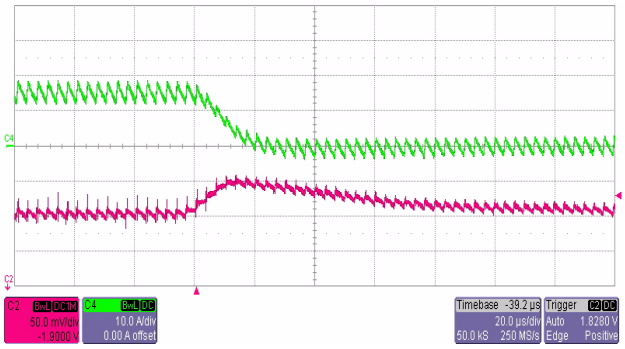


FIGURE 9. TRANSIENT RESPONSE

Efficiency

ISL8105BEVAL1Z, ISL8105BEVAL2Z based regulators enable the design of highly efficient systems. The efficiency of the evaluation board using a 12V input supply is shown in Figure 10.

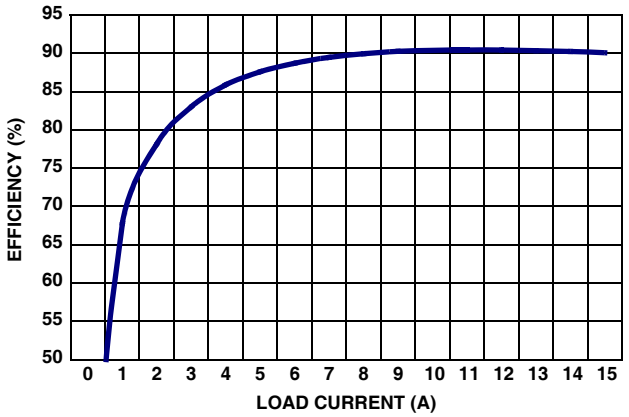


FIGURE 10. EVALUATION BOARD EFFICIENCY (V_{OUT} = 1.8V)

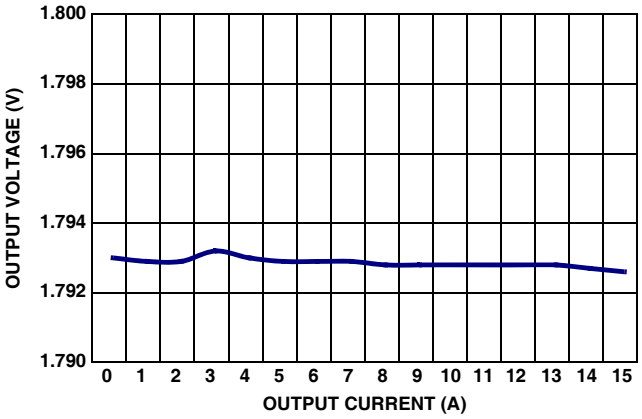


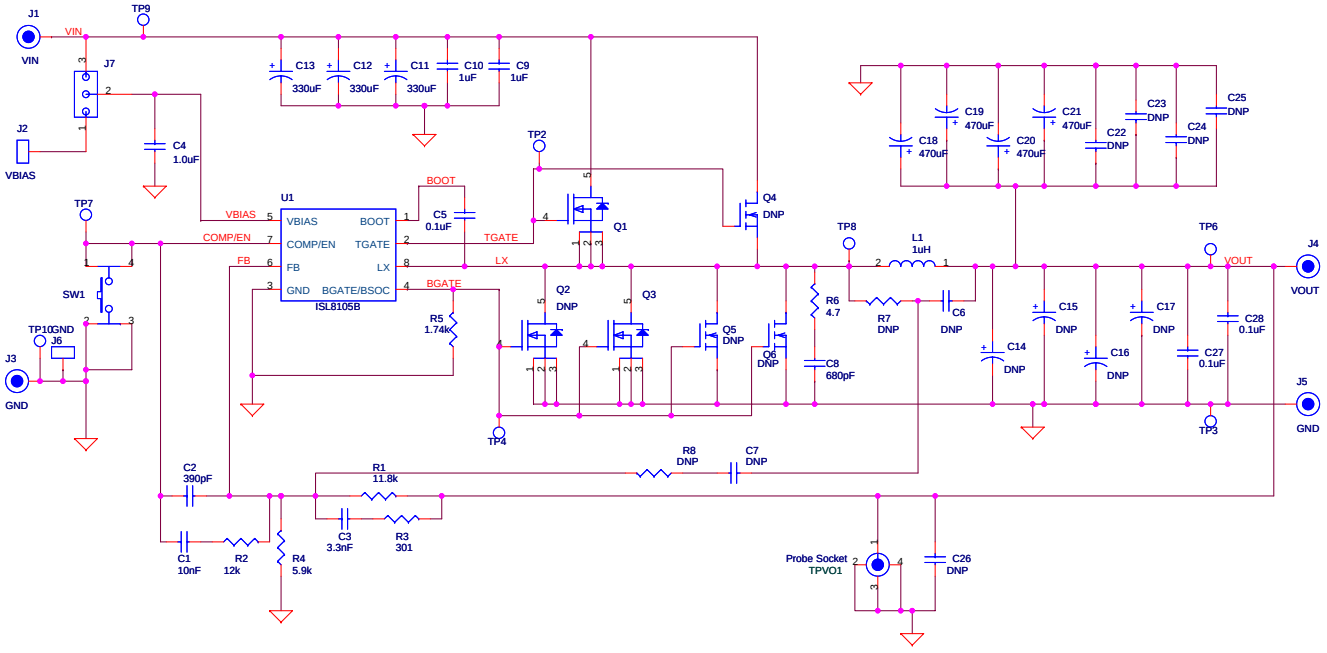
FIGURE 11. EVALUATION BOARD LINE REGUALTION

References

For Intersil documents available on the web, go to http://www.intersil.com/.

1. ISL8105, ISL8105B Data Sheet, FN6306, “+5V or +12V Single-Phase Synchronous Buck Converter PWM Controller with Integrated MOSFET Gate Drivers”, Intersil Corporation
2. Tech Brief TB417, “Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators”, Intersil Corporation

ISL8105BEVAL1Z Schematic



ISL8105BEVAL1Z Bill of Materials

ID	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
1	U1	1	ISL8105BIBZ	IC, Linear	IC, Single PWM Controller	8 LD SOIC	Intersil
2	Q1	1	BSC080N30LS G	MOSFET	30V N-Channel MOSFET	TDSON-08	Infineon
3	Q3	1	BSC030N03LS G	MOSFET	30V N-Channel MOSFET	TDSON-08	Infineon
4	Q2, Q4, Q5, Q6	DNP		MOSFET			
5	L1	1	HC9-1R0-R	Inductor	1.0µH, high current inductor	SMD	Cooper Bussmann
6	SW1	1	EVQ-PAD04M	Push Switch	SWITCH-PUSH, TH, 6mm, 1P, PUSHB MOM-SPST		PANASONIC
CAPACITORS							
7	C1	1		Capacitor, Ceramic, X7R	10nF, 50V, 10%, ROHS	SM_0603	TDK/Generic
8	C2	1		Capacitor, Ceramic, X7R	390pF, 50V, 10%, ROHS	SM_0603	TDK/Generic
9	C3	1		Capacitor, Ceramic, X7R	3.3nF, 50V, 10%, ROHS	SM_0603	TDK/Generic
10	C4, C9, C10	3		Capacitor, Ceramic, X7R	1µF, 25V, 10%, X7R, ROHS	SM_0805	TDK/Generic
11	C5, C27, C28	3		Capacitor, Ceramic, X7R	0.1µF, 16V, 10%, ROHS	SM_0603	TDK/Generic
12	C8	1		Capacitor, Ceramic, X7R	680pF, 50V, 10%, ROHS	SM_0603	TDK/Generic
13	C11, C12, C13	3	35ME330AX	Aluminum Capacitor	330µF, 35V	RAD 10x20	Sanyo
14	C18, C19, C20, C21	4	2R5TPF470ML	Organic Alumium Capacitor	470µF, 2.5V, 20%, ROHS	Case D3L	Sanyo
15	C6, C7, C14, C15, C16, C17, C22, C23, C24, C25, C26	DNP					
RESISTORS							
16	R1	1		Resistor, Film	11.8kΩ, 1%, 1/16W	SM_0603	Panasonic/Generic
17	R2	1		Resistor, Film	12kΩ, 1%, 1/16W	SM_0603	Panasonic/Generic
18	R3	1		Resistor, Film	301Ω, 1%, 1/16W	SM_0603	Panasonic/Generic
19	R4	1		Resistor, Film	5.9kΩ, 1%, 1/16W	SM_0603	Panasonic/Generic
20	R5	1		Resistor, Film	1.74kΩ, 1%, 1/16W	SM_0603	Panasonic/Generic
21	R6	1		Resistor, Film	4.7Ω, 1%, 1/16W	SM_0603	Panasonic/Generic
22	R7, R8	DNP				SM_0603	
OTHERS							
23	TPVO1	DNP		Terminal, Scope Probe	CONN-PIN RECEPTACLE, 0.086 DIA, 0.200 L, ROHS		MILL-MAX
24	J1, J4	2	111-0702-001	Blinding Post	CONN-GEN, BIND. POST, RED, THMBNUT-GND		JOHNSON COMPONENTS
25	J3, J5	2	111-0703-001	Blinding Post	CONN-GEN, BIND. POST, BLACK, THMBNUT-GND		JOHNSON COMPONENTS
26	J2, J6	2	1514-2	Turrett Post	CONN-TURRET, TERMINAL POST, TH, ROHS		Keystone
27	J7	1	68000-236-1X3		3-pin Jumper		Berg/FCI
28	TP3, TP6, TP9, TP10	4	5002	Test Point	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS		Keystone
29	TP2, TP4, TP7, TP8	DNP	5002	Test Point	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS		Keystone

ISL8105BEVAL1Z Printed Circuit Board Layers

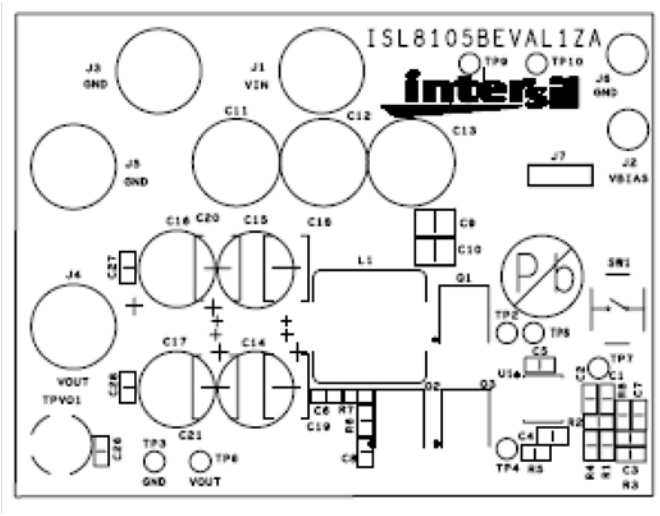


FIGURE 12. ISL8105BEVAL1Z - TOP LAYER (SILKSCREEN)

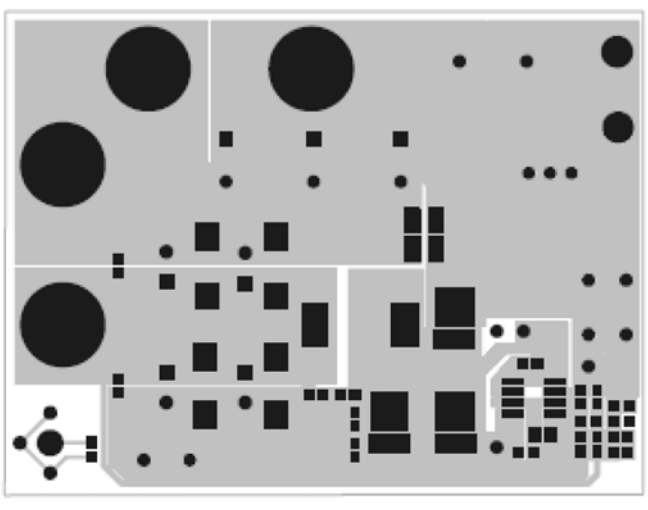


FIGURE 13. ISL8105BEVAL1Z - TOP LAYER (COMPONENT SIDE)

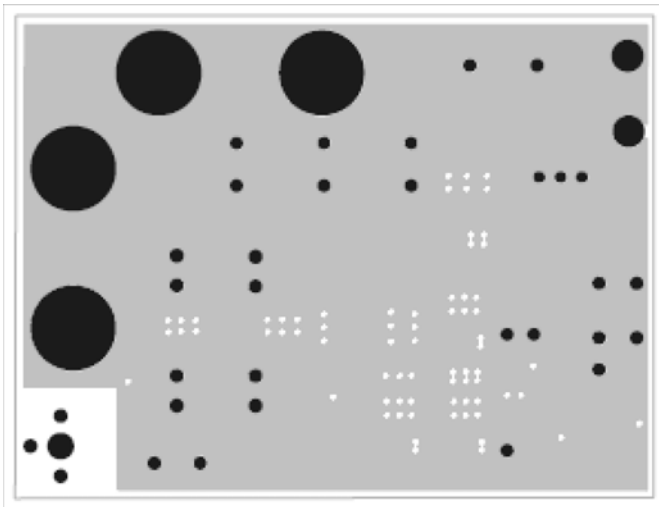


FIGURE 14. ISL8105BEVAL1Z - LAYER 2

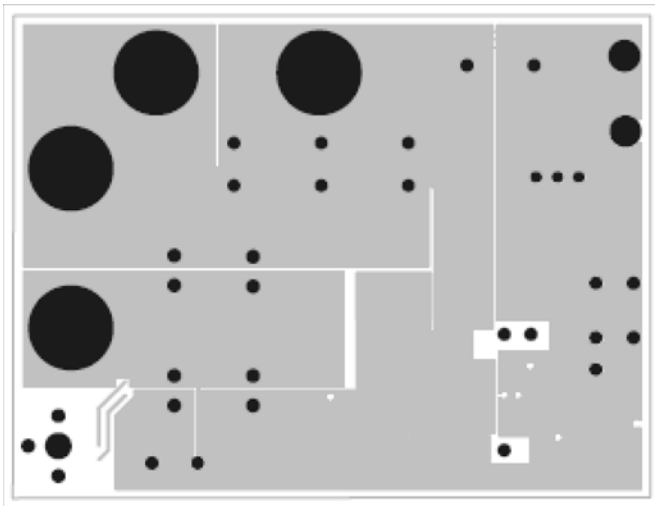


FIGURE 15. ISL8105BEVAL1Z - LAYER 3

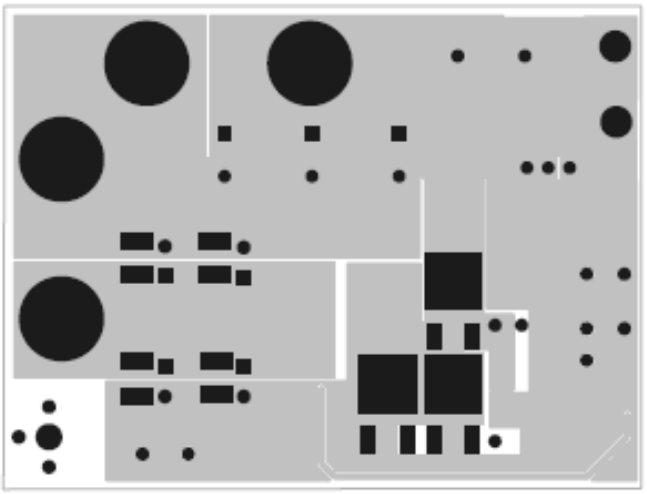


FIGURE 16. ISL8105BEVAL1Z - BOTTOM LAYER

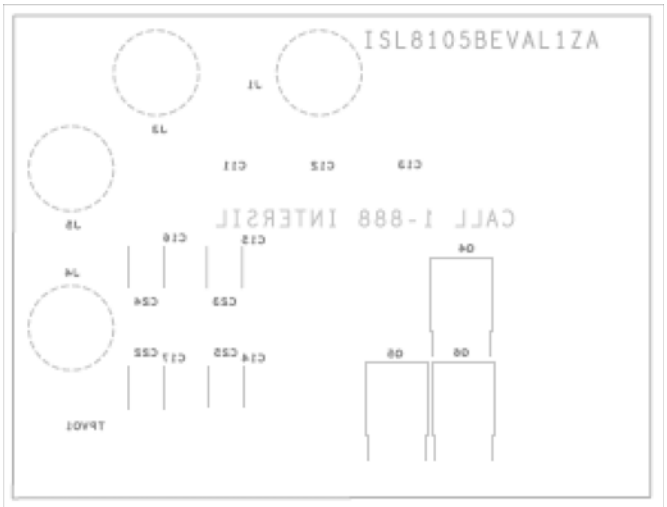
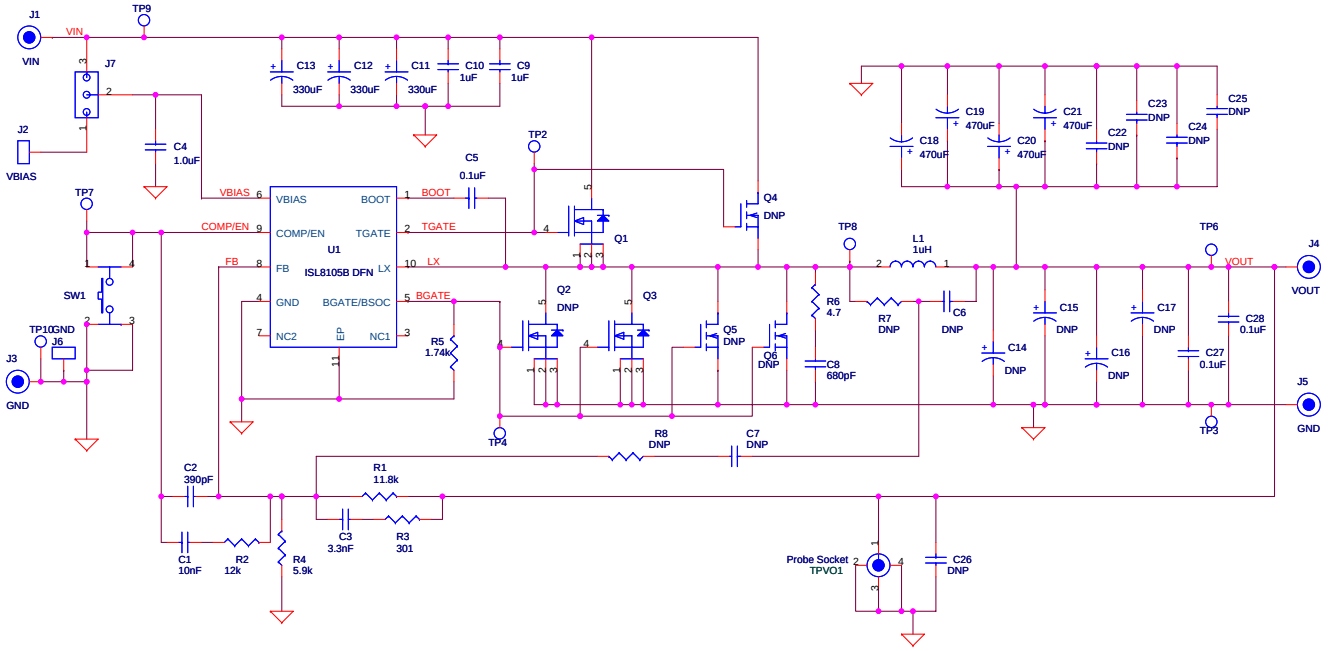


FIGURE 17. ISL8105BEVAL1Z - BOTTOM LAYER (SOLDER SIDE)

ISL8105BEVAL2Z Schematic



ISL8105BEVAL2Z Bill of Materials

ID	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
1	U1	1	ISL8105BIRZ	IC, Linear	IC, Single PWM Controller	10 LD DFN	Intersil
2	Q1	1	BSC080N30LS G	MOSFET	30V N-Channel MOSFET	TDSON-08	Infineon
3	Q3	1	BSC030N03LS G	MOSFET	30V N-Channel MOSFET	TDSON-08	Infineon
4	Q2, Q4, Q5, Q6	DNP		MOSFET			
5	L1	1	HC9-1R0-R	Inductor	1.0µH, high current inductor	SMD	Cooper Bussmann
6	SW1	1	EVQ-PAD04M	Push Switch	SWITCH-PUSH, TH, 6mm, 1P, PUSHB MOM-SPST		PANASONIC
CAPACITORS							
7	C1	1		Capacitor, Ceramic, X7R	10nF, 50V, 10%, ROHS	SM_0603	TDK/Generic
8	C2	1		Capacitor, Ceramic, X7R	390pF, 50V, 10%, ROHS	SM_0603	TDK/Generic
9	C3	1		Capacitor, Ceramic, X7R	3.3nF, 50V, 10%, ROHS	SM_0603	TDK/Generic
10	C4, C9, C10	3		Capacitor, Ceramic, X7R	1µF, 25V, 10%, X7R, ROHS	SM_0805	TDK/Generic
11	C5, C27, C28	3		Capacitor, Ceramic, X7R	0.1µF, 16V, 10%, ROHS	SM_0603	TDK/Generic
12	C8	1		Capacitor, Ceramic, X7R	680pF, 50V, 10%, ROHS	SM_0603	TDK/Generic
13	C11, C12, C13	3	35ME330AX	Aluminum Capacitor	330µF, 35V	RAD 10x20	Sanyo
14	C18, C19, C20, C21	4	2R5TPF470ML	Organic Alumium Capacitor	470µF, 2.5V, 20%, ROHS	Case D3L	Sanyo
15	C6, C7, C14, C15, C16, C17, C22, C23, C24, C25, C26	DNP					
RESISTORS							
16	R1	1		Resistor, Film	11.8kΩ, 1%, 1/16W	SM_0603	Panasonic/Generic
17	R2	1		Resistor, Film	12kΩ, 1%, 1/16W	SM_0603	Panasonic/Generic
18	R3	1		Resistor, Film	301Ω, 1%, 1/16W	SM_0603	Panasonic/Generic
19	R4	1		Resistor, Film	5.9kΩ, 1%, 1/16W	SM_0603	Panasonic/Generic
20	R5	1		Resistor, Film	1.74kΩ, 1%, 1/16W	SM_0603	Panasonic/Generic
21	R6	1		Resistor, Film	4.7Ω, 1%, 1/16W	SM_0603	Panasonic/Generic
22	R7, R8	DNP				SM_0603	
OTHERS							
23	TPVO1	DNP		Terminal, Scope Probe	CONN-PIN RECEPTACLE, 0.086 DIA, 0.200 L, ROHS		MILL-MAX
24	J1, J4	2	111-0702-001	Blinding Post	CONN-GEN, BIND. POST, RED, THMBNUT-GND		JOHNSON COMPONENTS
25	J3, J5	2	111-0703-001	Blinding Post	CONN-GEN, BIND. POST, BLACK, THMBNUT-GND		JOHNSON COMPONENTS
26	J2, J6	2	1514-2	Turrett Post	CONN-TURRET, TERMINAL POST, TH, ROHS		Keystone
27	J7	1	68000-236-1X3		3-pin Jumper		Berg/FCI
28	TP3, TP6, TP9, TP10	4	5002	Test Point	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS		Keystone
29	TP2, TP4, TP7, TP8	DNP	5002	Test Point	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS		Keystone

ISL8105BEVAL2Z Printed Circuit Board Layers

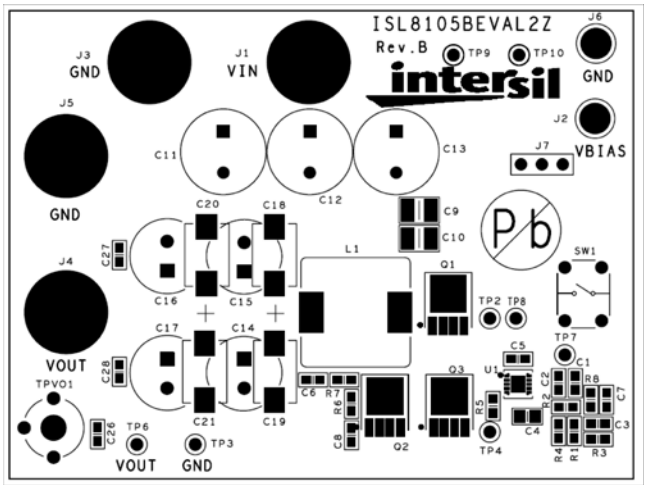


FIGURE 18. ISL8105BEVAL2Z - TOP LAYER (SILKSCREEN)

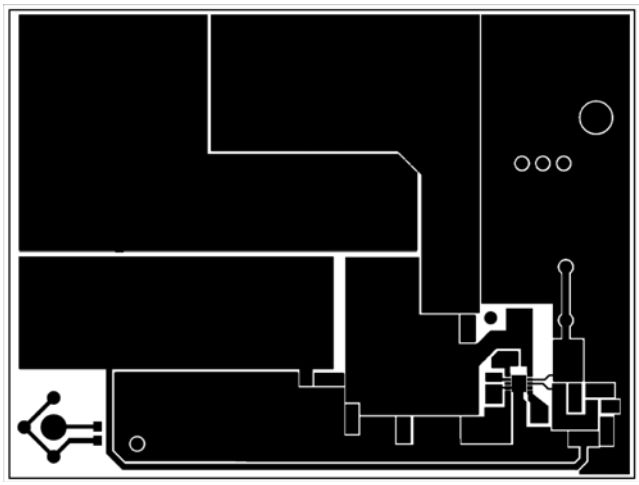


FIGURE 19. ISL8105BEVAL2Z - TOP LAYER (COMPONENT SIDE)

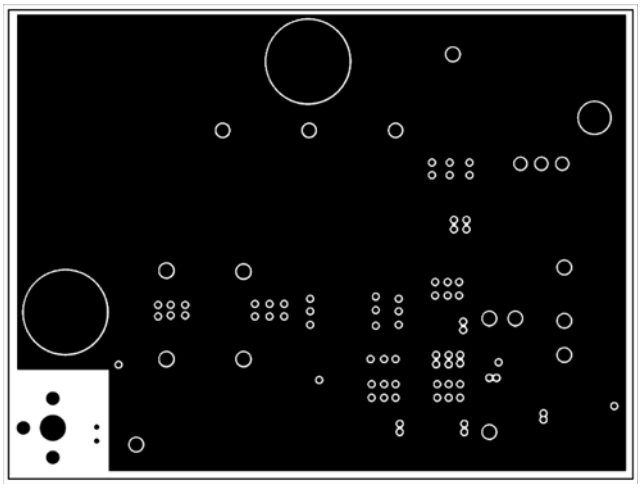


FIGURE 20. ISL8105BEVAL2Z - LAYER 2

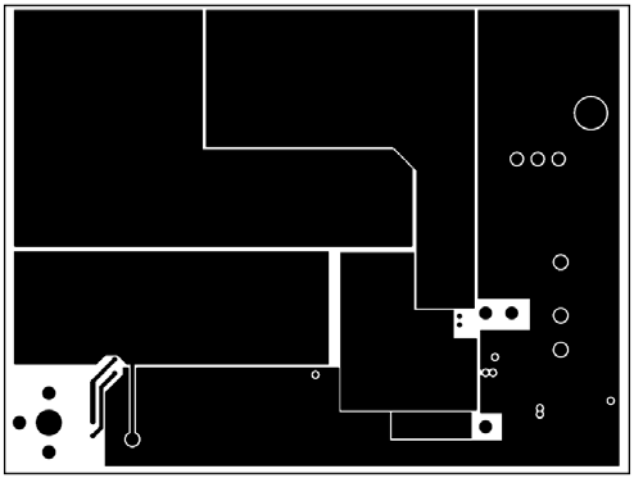


FIGURE 21. ISL8105BEVAL2Z - LAYER 3

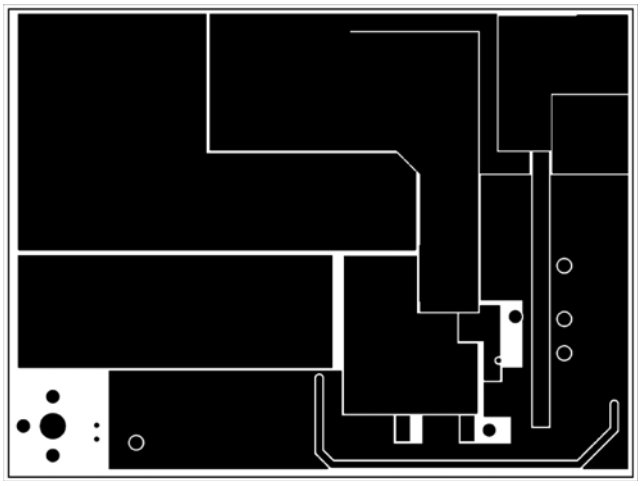


FIGURE 22. ISL8105BEVAL2Z - BOTTOM LAYER

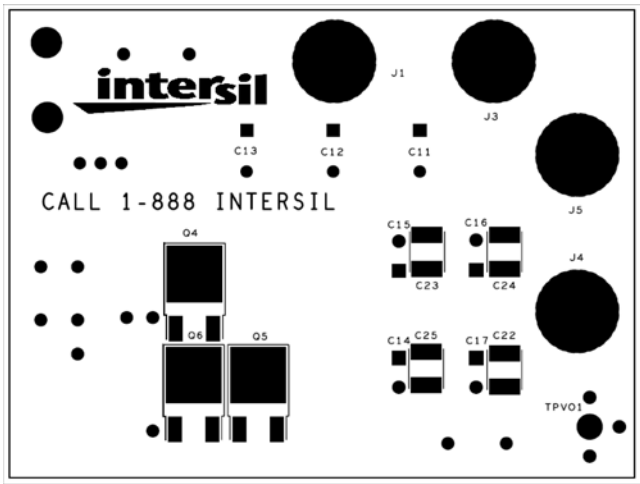


FIGURE 23. ISL8105BEVAL2Z - BOTTOM LAYER (SOLDER SIDE)