200W, 470kHz, Telecom Power Supply Using ISL6551 Full-Bridge Controller and ISL6550 Supervisor and Monitor

Application Note | August 2002 | AN1002

Author: Chun Cheung

Abstract

This application note highlights design considerations for a 200W, 470kHz, telecom power supply using Intersil's ISL6551 ZVS Full-Bridge Controller and ISL6550 Supervisor And Monitor. The zero-voltage switching technique of the ISL6551 is presented in detail. A step-by-step design procedure for a 48V-to-3.3V@60A with 88% efficiency converter based on these two chips, incorporating both ZVS full bridge and current doubler topologies, is described. A few tips for design and debugging are then listed. Finally, experimental results with discussion gives users a deeper understanding of the performance of the reference design and the advantages of the ISL6550 and ISL6551.

Introduction

In medium to high power applications with extreme efficiency requirements, the full-bridge topology is probably the best choice. Besides great transformer utilization with this topology, higher efficiency and lower EMI levels are the major benefits if utilizing circuit parasitics, which include output capacitance of the bridge FETs, primary capacitance of the transformer, and leakage inductance, to achieve zero-voltage transitions (ZVT). In the conventional full bridge converter, these advantages cannot be realized without employing a significant amount of soft-switching/resonant circuitry which adds cost and circuit board real estate. Intersil's ISL6551 full-bridge controller implements a unique control algorithm, rather than the traditional phase-shifted control technique introduced by TI's UC3875, to achieve ZVS with few components. In addition, the ISL6551 integrates additional sophisticated features such as Leading Edge Blanking, Latching Shutdown Input, Enable Input, Current Share Support, Fast Short-Circuit Shutdown, Synchronous Drive Signals, and Power Good Indication that the UC3875 does not provide. The ISL6551 enables a complete and sophisticated power supply solution and can save board space and engineering effort as well as cost.

This application note provides detailed design considerations of a 200W telecom power supply reference design employing both Intersil's ISL6551 full-bridge controller and ISL6550 Supervisor and Monitor while taking advantage of both ZVS full-bridge and current doubler topologies, as shown in Figure 1.

An alternative secondary rectification technique for push-pull and bridge converters is introduced by Laszlo Balogh in his paper [2]. This technique offers potential benefits of better distributed power dissipation in densely packed power supplies and in medium to high power and/or high output current applications [2].

This converter is designed to meet the specification of an industry-standard half brick. Most of the converter circuits are placed in the central 2.50"x2.45" area and limited within 0.5" height, and all other unnecessary components such as test point connectors and I/O connectors are placed beyond this area. To easily modify the evaluation board for a broader base of applications, additional circuits are designed in and magnetics components are not integrated with the PCB. This expands the area of the evaluation board when compared to a standard half-brick design. This DC/DC converter accepts a wide range input of 36V to 75V and generates a DAC-adjustable wide range output of 2.64V to 3.63V with 31.918mV step. An ultra high efficiency of 88% at 3.312V with a fully loaded 60A output has been achieved.

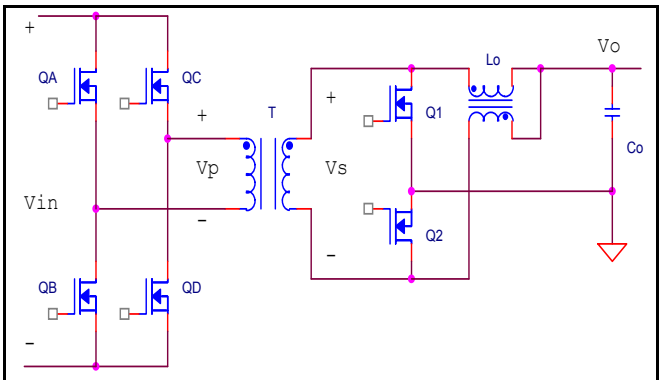


FIGURE 1. FULL BRIDGE + CURRENT DOUBLER TOPOLOGIES

This application note first introduces the unique ZVS technique of the ISL6551. The Supervisor and Monitor ISL6550 chip is then briefly introduced. Thereafter, a step-by-step design procedure for the reference design is followed, including power train component selection, component power dissipation calculations, magnetics design parameter calculations, and control loop design. A few tips for design and debugging are listed. Finally, experimental results of the evaluation board are discussed. Term Definitions, Block Diagram, Schematics, Layout, Bill of Materials, References, and Preliminary Specifications of the Reference Design are included at the end of this paper.

Intersil ZVS Full Bridge Controller: ISL6551

The diagonal bridge switches are turned on together in a conventional full bridge converter which alternatively places the input voltage, V_{IN}, across the primary of the transformer for a period of Ton, as shown in Figure 2. The limiting factor of achieving optimum efficiency in this circuit is the hard switching nature of the operation, which causes significant

switching losses in high frequency, high input voltage, and /or high current applications. The switching losses can be reduced by employing snubbers, or quasi- or fully resonant, soft-switching circuits [1].

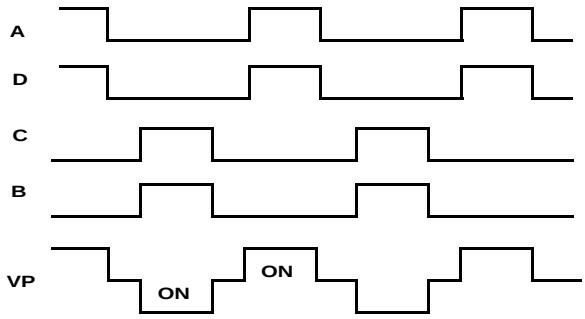


FIGURE 2. CONVENTIONAL FULL BRIDGE PWM WAVEFORMS

In the ISL6551, rather than driving both of the diagonal full bridge switches together, the two upper switches (QA & QC) are driven at a fixed 50% duty cycle and the two lower switches (QB & QD) are PWM-controlled on the trailing edge while the leading edge employs resonant delay. Figure 4 shows the drive signals of four bridge FETs and three options for synchronous rectification. The basic control principle of the ISL6551 is different from that of the UC3875's phase-shift control which varies the phase between two 50% duty cycle control signals [1], requiring additional circuitry to derive the synchronous control signals and therefore adding cost.

The ISL6551 is a ZVS full bridge controller that Intersil has designed for medium to high power AC/DC and DC/DC applications with ultra high efficiency requirements. The ISL6551 includes many integrated features for a more complete and sophisticated telecom or off-line power supply solution. The internal architecture of the IC is shown in Figure 4. Detailed ZVS operation of the ISL6551 will be presented by describing switching actions of the power train at each time interval in the following sections. Refer to the device datasheet for the operation of the integrated features.

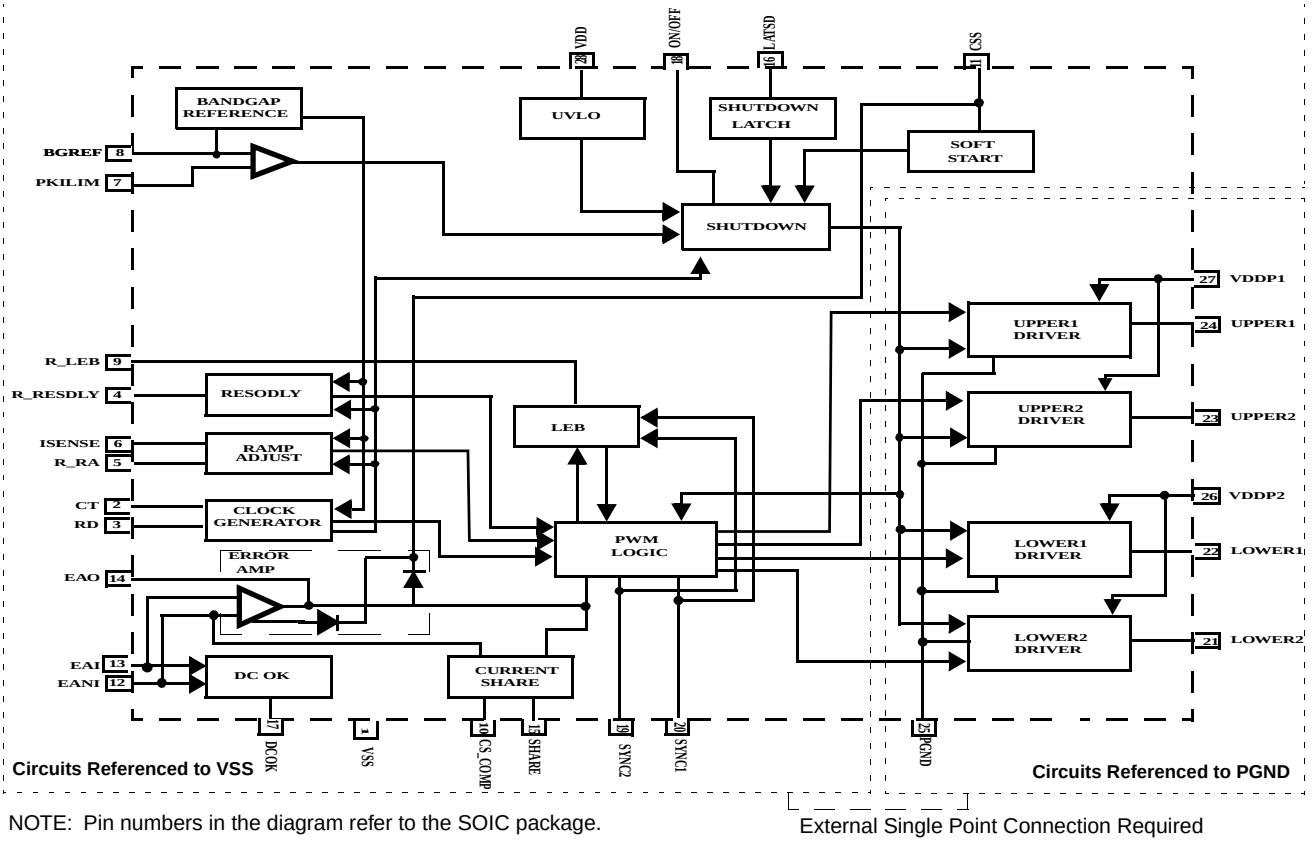
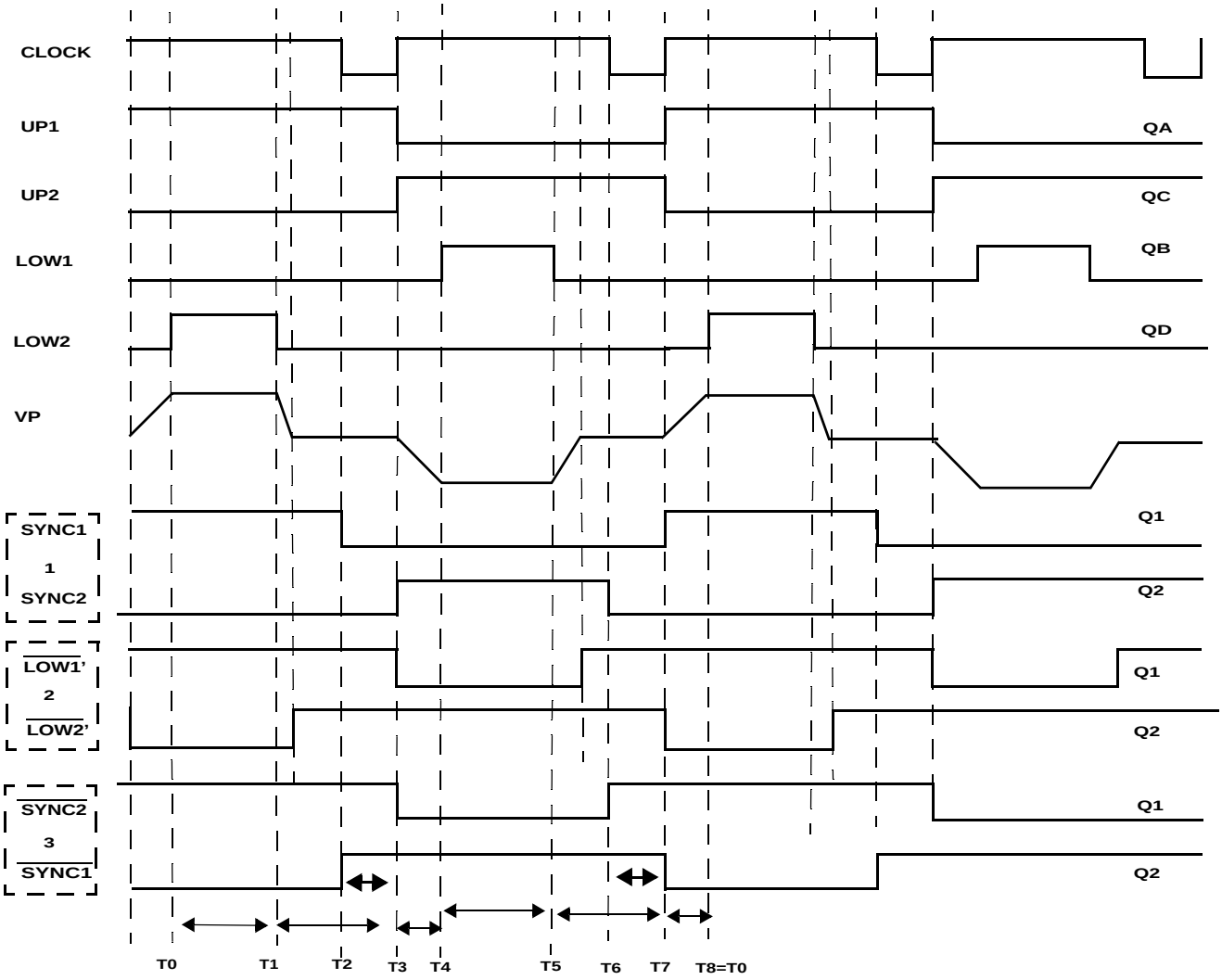


FIGURE 3. ISL6551 INTERNAL STRUCTURE

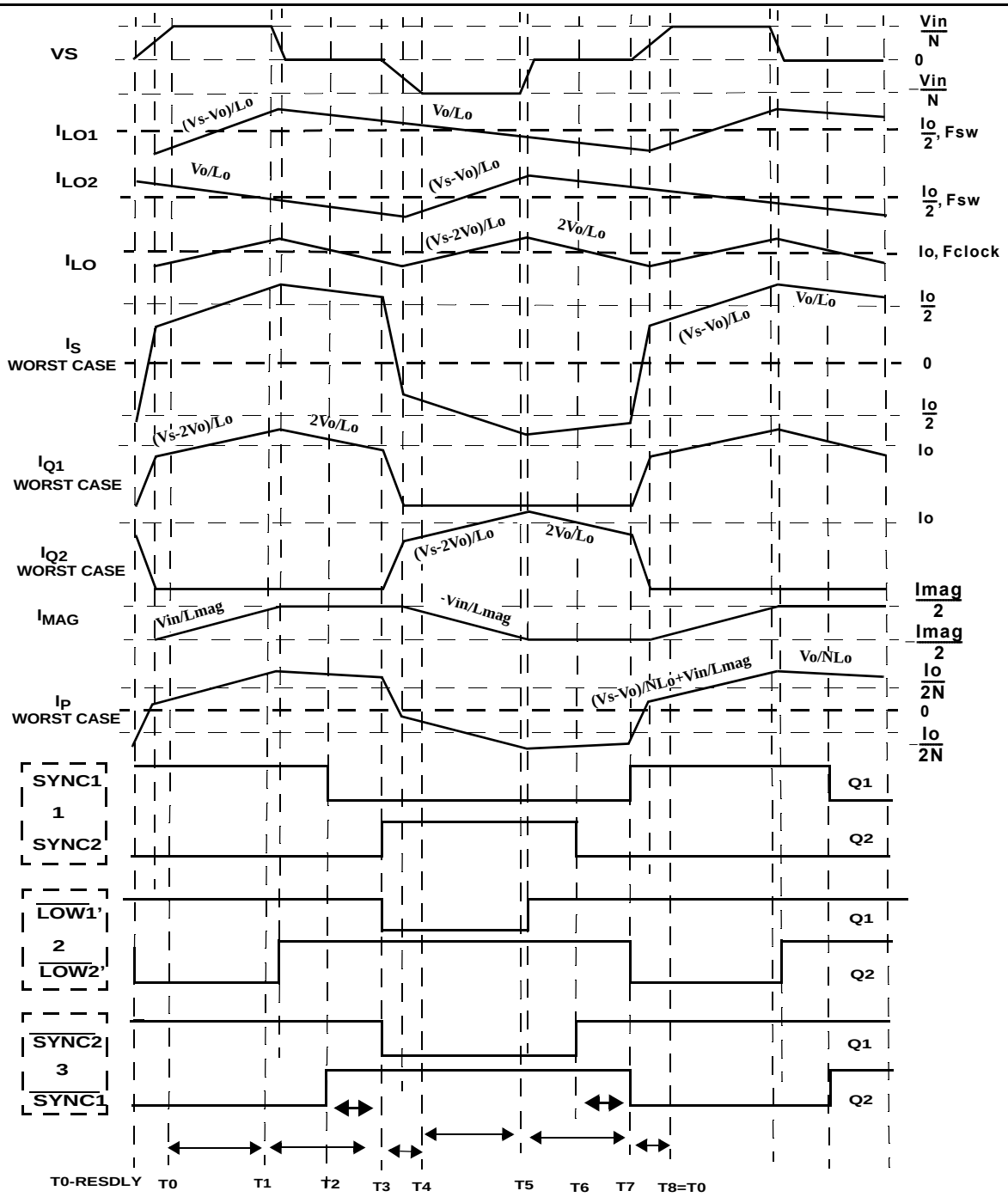


T0-T1=LOWER RIGHT-LEG POWER TRANSFER PERIOD
T1-T2=UPPER LEFT-TO-RIGHT FREEWHEELING PERIOD
T2-T3=Q1-TO-Q2 DEADTIME (FREEWHEELING)
T3-T4=LOWER LEFT-LEG RESONANT PERIOD
T4-T5=LOWER LEFT-LEG POWER TRANSFER PERIOD
T5-T6=UPPER RIGHT-TO-LEFT FREEWHEELING PERIOD
T6-T7=Q2-TO-Q1 DEADTIME (FREEWHEELING)
T7-T8=LOWER RIGHT-LEG RESONANT PERIOD

In the above Figure, T0 through T8 are exaggerated only for demonstration purposes. There are three possible synchronous rectification drive schemes:

1. Existing Synchronous Drive Signals (Sync1 & Sync2) + Non-inverting High Current Drivers (such as MIC4422)- The Synchronous Fets (Q1 & Q2) are turned off together at the dead time and turned on alternatively every clock period;
2. Lower Drive Signals + Proper Delay + Inverting High Current Drivers (such as MIC4421)- The corresponding synchronous FET is turned off whenever a voltage is across the secondary winding;
3. Existing Synchronous Drive Signals + Inverting High Current Drivers- The synchronous FETs are turned on together at the dead time and turned on alternately every clock period.

FIGURE 4. DRIVE SIGNALS TIMING DIAGRAM

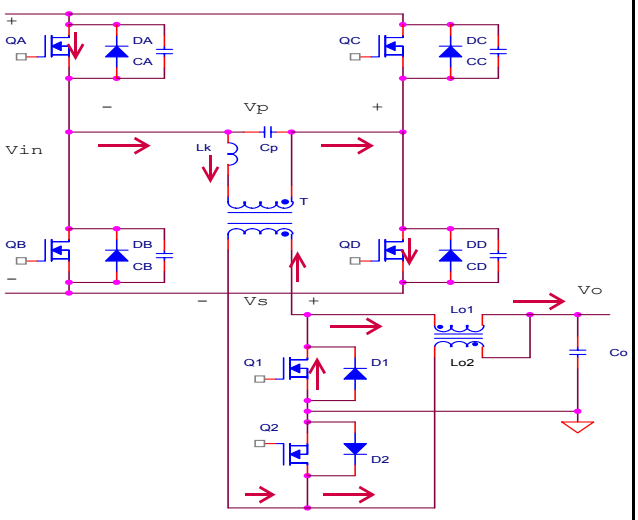


T0-T1=LOWER RIGHT-LEG POWER TRANSFER PERIOD
T1-T2=UPPER LEFT-TO-RIGHT FREEWHEELING PERIOD
T2-T3=Q1-TO-Q2 DEADTIME (FREEWHEELING)
T3-T4=LOWER LEFT-LEG RESONANT PERIOD
T4-T5=LOWER LEFT-LEG POWER TRANSFER PERIOD
T5-T6=UPPER RIGHT-TO-LEFT FREEWHEELING PERIOD
T6-T7=Q2-TO-Q1 DEADTIME (FREEWHEELING)
T7-T8=LOWER RIGHT-LEG RESONANT PERIOD

In the above figure, T0 through T8 are exaggerated only for demonstration purposes. The slope of each waveform is in an approximation. For a more accurate representation, losses should be included. The worst case happens at only Q1 or Q2 carrying the load current during the freewheeling period. The current distribution through Q1 and Q2 is different in these three drive schemes. Case 2 is the best option since both of its synchronous FETs are turned on during the free-wheeling period. Note that VS is in the case of no primary leakage inductance, otherwise, delay would be induced, as illustrated in the experimental results.

FIGURE 5. CURRENT WAVEFORMS

T0 -->T1, QA-to-QD Power Transfer (Active) Period [Figure 6]



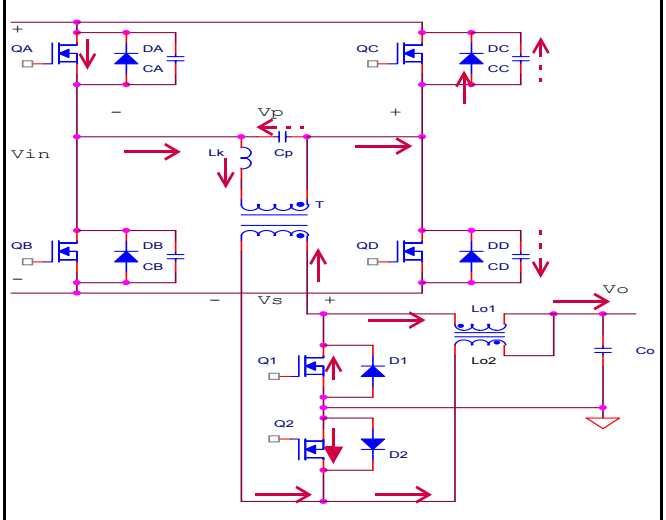
SYNCHRONOUS FETS	Q1	Q2
SYNC DRIVE	ON	OFF
INV_LOW DRIVE	ON	OFF
INV_SYNC DRIVE	ON	OFF

FIGURE 6. QA-TO-QD POWER TRANSFER PERIOD

When QD is turned on, QA has been already turned on in the previous period, the resonant delay. In this transfer (active) period, the full input voltage (V_{IN}) is across the primary of the transformer, and V_{IN}/N is across the secondary of the transformer once the primary current catches the reflected output current. The primary current first flows from QD to QA due to the prior resonant current and then reverses in direction until the current reaches zero and starts ramping up at a rate determined by V_{IN}, the magnetizing inductance, and the output inductance. Simultaneously, Q2 should stay off for eliminating shoot-through currents, and Q1 is turned on to reduce conduction losses; the current through the Lo2 is positive ramp, and the current through the Lo1 is negative ramp. The ON-time of QD is a function of V_{IN}, Vo, the transformer turns ratio N, and the output load Io. QD is turned off when the peak of the modified current ramp signal hits the error voltage, and the freewheeling period then begins.

T1 --> T2, QA-to-QC Clamped Freewheeling (Passive) Period [Figure 7]

Once QD is turned off by trailing edge pulse width modulation, the primary current continues flowing into the output capacitance (Coss) CD of QD, which will be charged up from the switch Rds(on) Drop to V_{IN} - Diode Drop. Simultaneously, the primary capacitance (Cp) of the transformer and the output capacitance CC of QC are discharged to from V_{IN} to zero voltage (~diode drop).



SYNCHRONOUS FETS	Q1	Q2
SYNC DRIVE	ON	OFF
INV_LOW DRIVE	ON	ON
INV_SYNC DRIVE	ON	OFF

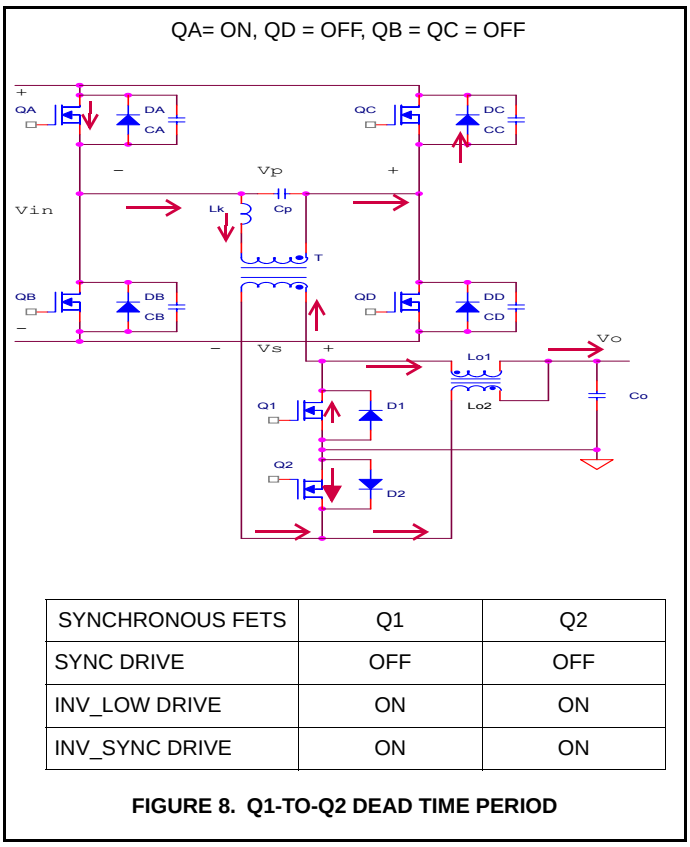
FIGURE 7. QA-TO-QC CLAMPED FREEWHEELING PERIOD

This transition is accomplished using the energy stored in the leakage inductance of the transformer, the magnetizing inductance, the reflected output inductance, and any external commutating inductance. After the transition, the primary current flows in the same direction and the real freewheeling period begins. One end of the transformer is shorted to V_{IN} by the channel of QA, and the other end is clamped to V_{IN} by the body diode of QC, which is the only path that the primary current can go through. The losses due to the body diode conduction at the freewheeling period could be significant if the primary current (the lumped sum of the magnetizing current and the reflected secondary winding freewheeling current), is relatively high. These conduction losses can be minimized by employing the maximum allowable turns ratio of the main transformer, i.e, the maximum allowable duty cycle in the design. In some applications, shunting upper switches with Schottky diodes might be another possible way to reduce the conduction losses. For a wide range input application, if a pre-regulator is implemented, then a fixed, high duty cycle (~100%) post full-bridge regulator can be achieved and the freewheeling time is minimized. The power dissipation of the upper FETs can be therefore reduced significantly.

Three different synchronous rectification drive schemes can be implemented with the ISL6551 as shown in Figures 4 and 5. The INV_LOW DRIVE scheme is the one that would provide an additional path for the secondary freewheeling

current since both Q1 and Q2 are turned on during the freewheeling time, which could reduce the conduction losses and the reflected output current in the primary. The amount of the load current split into Q1 and Q2 depends on the voltage drop across the secondary winding, the Rds(on) of Q1 & Q2, and/or the body diode drop of Q1 & Q2. The optimum performance of the converter happens when the load current is split into both turned-on Q1 and Q2 evenly. In reality, the body diode drop at one of upper FETs, the leakage inductance, and the shorted primary winding force one of the synchronous FETs to carry the majority of the output current while the other conducts a minority of the load.

T2 --> T3, Q1-to-Q2 Dead Time Period [Figure 8]

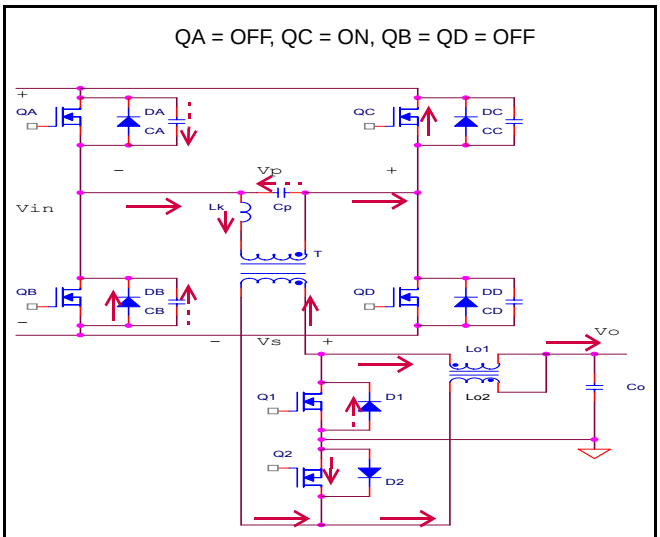


SYNCHRONOUS FETS	Q1	Q2
SYNC DRIVE	OFF	OFF
INV_LOW DRIVE	ON	ON
INV_SYNC DRIVE	ON	ON

FIGURE 8. Q1-TO-Q2 DEAD TIME PERIOD

The dead time is used to prevent simultaneous conduction of QC and QD, which would cause shoot-through currents. The dead time is still part of the freewheeling period. The drive control signals for the power switches therefore do not change states while the drive signals of the synchronous FETs change levels. In the SYNC DRIVE scheme, both Q1 and Q2 now are turned off and the load current freewheels through the body diodes of both FETs. This introduces high conduction losses in high output current applications. Shunting both synchronous FETs with schottky diodes can reduce the losses. In the INV_SYNC DRIVE scheme, both Q1 and Q2 are turned on, therefore, schottky diodes are not required, so are not in the INV_LOW DRIVE scheme.

T3 --> T4, Lower Left-Leg (QB) Resonant Period [Figure 9]



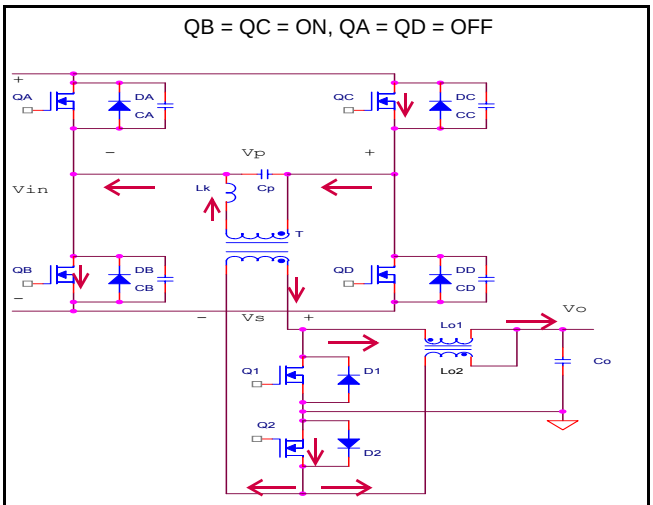
SYNCHRONOUS FETS	Q1	Q2
SYNC DRIVE	OFF	ON
INV_LOW DRIVE	OFF	ON
INV_SYNC DRIVE	OFF	ON

FIGURE 9. LOWER LEFT-LEG RESONANT PERIOD

The dead time period is followed by the lower left-leg resonant period. It begins with QA turned off and QC turned on. At the beginning of this transition, the input voltage is applied first across the commutating inductance (leakage and any external inductances), i.e, the real primary stays zero until the current through these inductors changes in direction in the next time interval. This can be seen in the voltage waveforms across the primary winding and the secondary winding, discussed in the *EXPERIMENTAL RESULTS* section on pages 24-25. The direction of the current through the primary winding remains the same as that in the previous time interval. The current flows into the transformer primary capacitance (Cp) and the output capacitance (Coss) CA of QA, which will be charged up from zero voltage (~Rds(on) Drop) to V_{IN}. Simultaneously, the output capacitance CB of QB is discharged to from V_{IN}- Rds(on) Drop to zero voltage (~diode drop). This transition is accomplished with the energy stored in the primary inductance (including leakage inductance, magnetizing inductance, and any external inductance). It takes a longer time to complete this transition than the one reaching the freewheeling period since the energy stored in the resonant inductances decreases due to the conduction losses of the power switches and the primary current is decaying in the freewheeling period. Once QB is clamped to zero voltage by its own body diode, QB is turned on at zero voltage (ZVS transition). Another power transfer period is followed by the other diagonal power switches (QC-to-QB). The rest of the

discussion (Figures 10 to 13) is just the repetition of another half cycle.

T4 --> T5, QC-to-QB Power Transfer Period [Figure 10]



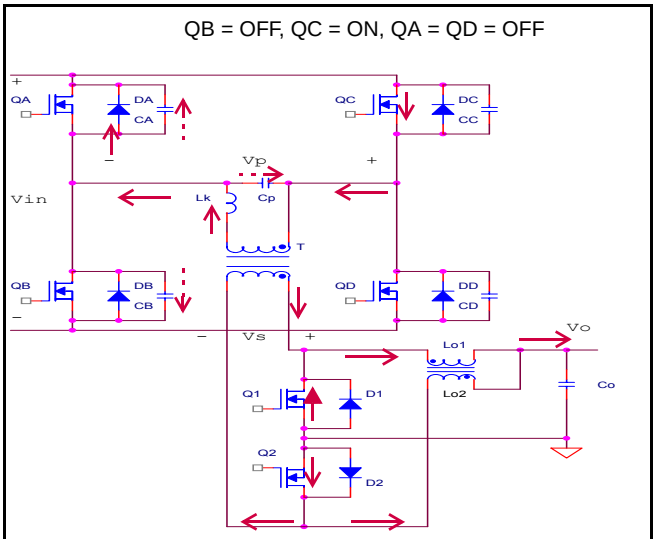
SYNCHRONOUS FETS	Q1	Q2
SYNC DRIVE	OFF	ON
INV_LOW DRIVE	OFF	ON
INV_SYNC DRIVE	OFF	ON

FIGURE 10. QC-TO-QB POWER TRANSFER PERIOD

When QB is turned on, QC has been already turned on in the previous period, the resonant delay. In this transfer (active) period, the full input voltage (V_{IN}) is across the primary of the transformer, and V_{IN}/N is across the secondary of the transformer once the primary current catches the reflected output active current. The primary current first flows from QB to QC due to the prior resonant current and then reverses in direction until the current reaches zero and starts ramping up at a rate determined by V_{IN}, the magnetizing inductance, and the output inductance. Simultaneously, Q1 should stay off for eliminating shoot-through currents, and Q2 is turned on to reduce conduction losses; the current through the Lo1 is a positive ramp, and the current through Lo2 is a negative ramp. The ON-time of QB is a function of V_{IN}, Vo, the transformer turns ratio N, and the output load Io. QB is turned off when the peak of the modified current ramp signal hits the error voltage, and another freewheeling period then begins.

T5 -->T6, QC-to-QA Clamped Freewheeling Period (Passive) [Figure 11]

Once QB is turned off, the primary current continues flowing into the output capacitance (Coss) CB of QB, which will be charged up from the switch Rds(on) Drop to V_{IN} + Diode Drop. Simultaneously, the primary capacitance (Cp) of the transformer and the output capacitance CA of QA are discharged from V_{IN} to zero voltage (~diode drop). This transition is accomplished using the energy stored in the leakage inductance of the transformer, the magnetizing inductance, the reflected output inductance, and any external commutating inductance. After the transition, the primary current flows in the same direction and the real freewheeling period begins. One end of the transformer is shorted to V_{IN} by the channel of QC, and the other end is clamped to V_{IN} by the body diode of QA, which is the only path that the primary current can go through. Refer to the T1-->T2 period for more detailed discussion.



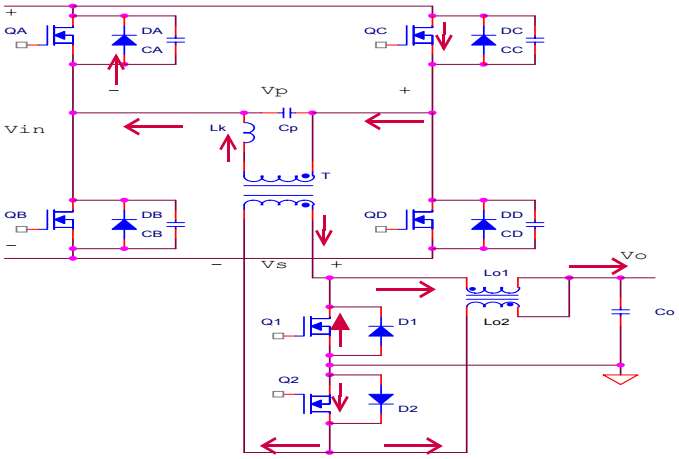
SYNCHRONOUS FETS	Q1	Q2
SYNC DRIVE	OFF	ON
INV_LOW DRIVE	ON	ON
INV_SYNC DRIVE	OFF	ON

FIGURE 11. QC-TO-QA CLAMPED FREEWHEELING PERIOD

T6 --> T7, Q2-to-Q1 Dead Time Period [Figure 12]

The dead time is used to prevent simultaneous conduction of QA and QB, which would cause shoot-through currents. The dead time period is still part of the freewheeling period, the drive control signals for the power switches therefore do not change states while the drive signals of the synchronous FETs change levels. In the SYNC DRIVE scheme, both Q1 and Q2 now are turned off, the load current free wheels through the body diodes of both FETs, which introduces high conduction losses in high output current applications. Shunting both synchronous FETs with schottky diodes can reduce the losses. In the INV_SYNC DRIVE scheme, both Q1 and Q2 are turned on, therefore, schottky diodes are not required, so are not in the INV_LOW DRIVE scheme.

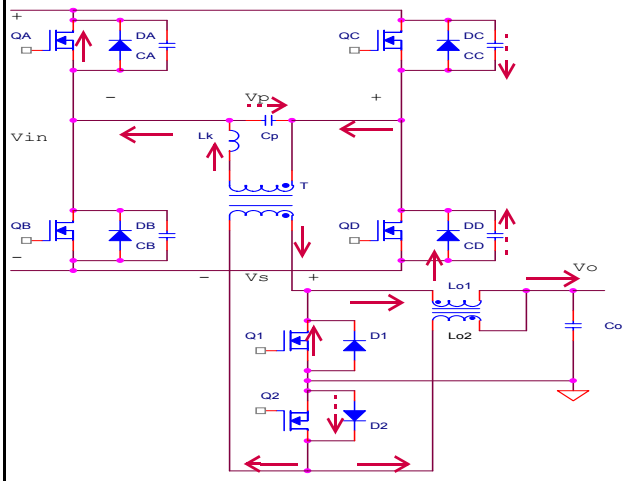
QB = OFF, QC = ON, QA = QD = OFF



SYNCHRONOUS FETS	Q1	Q2
SYNC DRIVE	OFF	ON
INV_LOW DRIVE	ON	ON
INV_SYNC DRIVE	ON	ON

FIGURE 12. DEAD TIME PERIOD

QC = OFF, QA = ON, QB = QD = OFF



SYNCHRONOUS FETS	Q1	Q2
SYNC DRIVE	ON	OFF
INV_LOW DRIVE	ON	OFF
INV_SYNC DRIVE	ON	OFF

FIGURE 13. LOWER RIGHT-LEG RESONANT PERIOD

T7 --> T8=To, Lower Right-Leg (QD) Resonant Period [Figure 13]

The previous dead time period is followed by the lower right-leg resonant period. It begins with QC turned off and QA turned on. At the beginning of this transition, the input voltage is applied first across the commutating inductance (leakage and any external inductances), i.e, the real primary stays zero until the current through these inductors changes in direction in the next time interval. This can be seen in the voltage waveforms across the primary winding and the secondary winding, discussed in the *EXPERIMENTAL RESULTS* section on page 24-25. The direction of the current through the primary winding remains the same as that in the previous time interval. The current flows into the transformer primary capacitance (Cp) and the output capacitance (Coss) CC of QC, which will be charged up from zero voltage (~Rds(on) Drop) to V_{IN}. Simultaneously, the output capacitance CD of QD is discharged to from V_{IN}- Rds(on) Drop to zero voltage (~diode drop). This transition is accomplished with the energy stored in the primary inductance (including leakage inductance, magnetizing inductance, and any external inductance). It takes a longer time to complete this transition than the one reaching the freewheeling period since the energy stored in the resonant inductance decreases due to the conduction losses of the power switches and the primary current is decaying in the freewheeling period. Once QD is clamped to zero voltage by its own body diode, QD is turned on at zero voltage (ZVS transition). At this point a full operating cycle is completed.

Intersil Supervisor and Monitor: ISL6550

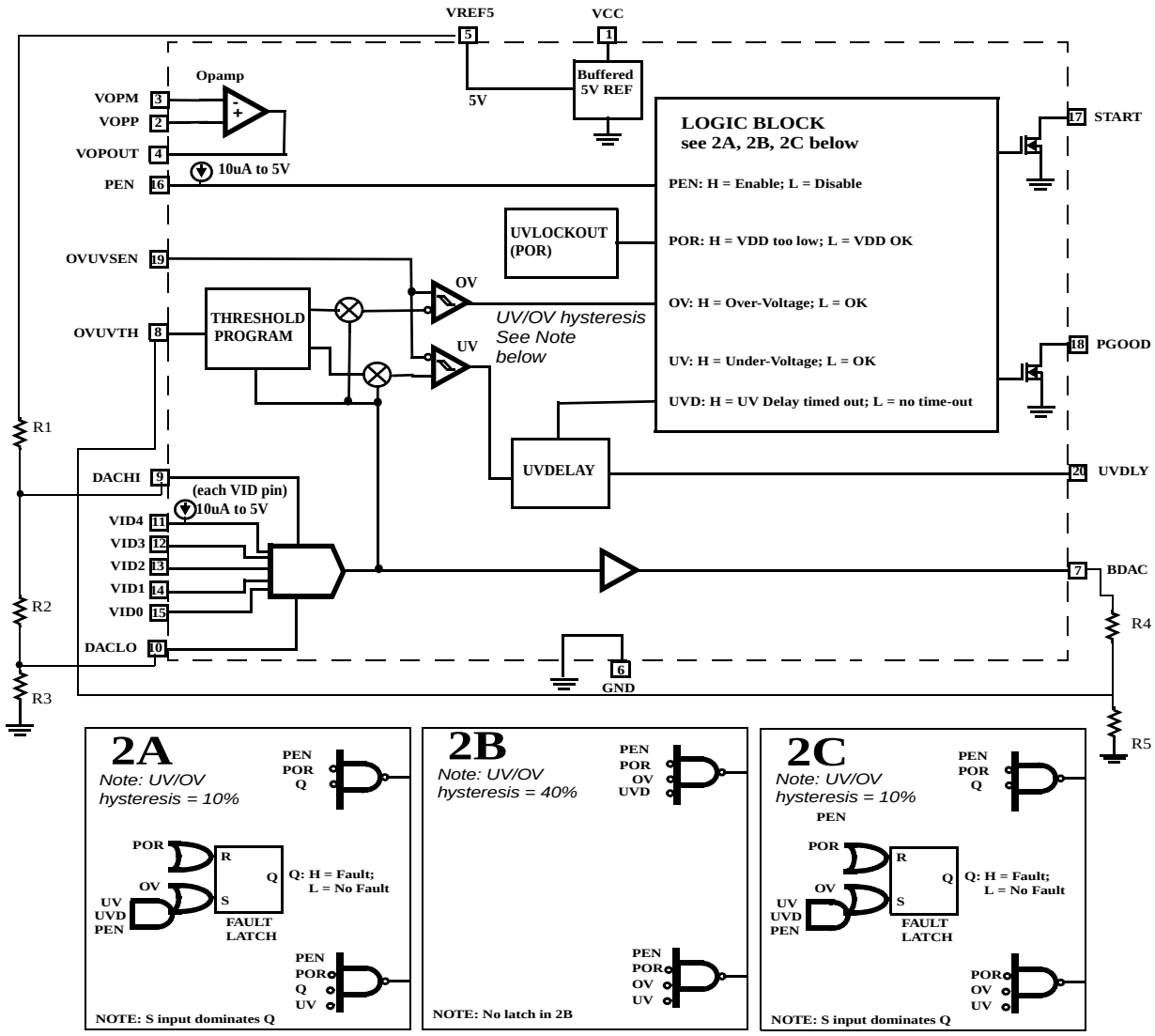
The ISL6550 is a precision flexible, VID-code-controlled reference and voltage monitor for high-end microprocessor and memory power supplies. It monitors various input signals, and supervises the systems with its outputs. The ISL6550 saves board space, design time, and system cost. The internal structure of the ISL550 is shown in Figure 14. The reference design is implemented with the MLFP-packaged ISL6550, **C** version. Refer to the device datasheet for operating details.

In the reference design, the ISL6550 monitors the output voltage and supervises the ISL6551 full bridge controller.

- The spare operational amplifier of the ISL6550 is used as a differential amplifier and its output (VOPOUT) is sent to the inverting input (EAI) of the error amplifier of the ISL6551. Note that the VOPOUT is limited to 5V.
- The under-voltage delay (UVDLY) prevents false triggering of the START output during startup, and the ISL6550 START output is fed to the ON/OFF input of the ISL6551. In output over-voltage (+8.33%) and under-voltage (-8.33%) conditions, the START is triggered and latches shutdown the ISL6551 controller. When the VCC of ISL6550 is below the turn-on/off threshold, the START is held low and disables the ISL6651 controller.
- The output reference BDAC, which is fed to the non-inverting input (EANI) of the error amplifier of the ISL6551, is programmed by the 5-bit VIDs and the resistor network that connects to DACHI and DACLO. Note that a 50k total resistance of the network is recommended and the overall

output error should include VREF5 error and external resistor divider error as well as the internal buffer offset. In the reference design, the output voltage can be programmed from 2.64V to 3.63V with 31.918mV step and +/-3% statics error over full operating conditions.

- The output voltage is sensed by the OVUVSEN, and the OV-UV windows is centered around the BDAC voltage and can be programmed with the OVUVTH pin from +/-5% to +/-40% about the BDAC voltage. In the reference design, the over/under voltage window is set at +/-8.33%.
- PEN is connected to a mechanical switch to turn on/off the converter manually. It is also controlled by the circuitries that monitor the input voltage level and the thermal condition of the converter.
- PGOOD provides an indication if the output voltage is within over/under voltage limits (+/-8.33%).



NOTE: Pin numbers in the diagram refer to the SOIC package.

FIGURE 14. ISL6550 INTERNAL STRUCTURE

Converter Design

This section presents a step-by-step design procedure for a 48V-to-3.3V, 200W, 470kHz with 88% efficiency converter using both ISL6551 and ISL6550 for telecom applications (i.e V_{IN}=36V-to-75V). The converter is designed with secondary-referenced, peak current-mode control, and both ZVS full bridge and current doubler topologies.

For simplicity, all calculations in this section neglect the transitions shown in Figure 5. The worst case current waveforms are used even in the INV_LOW DRIVE scheme, unless otherwise stated.

Select Synchronous DRIVE Scheme

The INV_LOW DRIVE scheme for synchronous rectification is employed in the reference design. This scheme induces less conduction losses in the synchronous FETs than both INV_SYNC and SYNC DRIVE schemes, which can be explained with a few equations (EQ. 1- 6). The terms used in all equations are defined later in the paper, unless otherwise stated in the text.

$$Io^2 = (IQ1 + IQ2)^2 = IQ1^2 + IQ2^2 + 2 \bullet IQ1 \bullet IQ2 \quad \text{(EQ. 1)}$$

$$IQ1^2 + IQ2^2 \leq IQ1^2 + IQ2^2 + 2 \bullet IQ1 \bullet IQ2 \quad \text{(EQ. 2)}$$

The power dissipation is the same in the active (transfer) period but different in the freewheeling period for the three drive schemes. In both INV_SYNC and SYNC DRIVE schemes, only one synchronous FET is turned on carrying all the load current during the freewheeling period. The conduction losses of each leg in the freewheeling period can be approximated with EQ. 3:

$$Psynfetfr = Io^2 \bullet \left(\frac{1-D}{2}\right) \bullet Rdsonsyn \quad \text{(EQ. 3)}$$

In the INV_LOW DRIVE scheme, both synchronous FETs are turned on and each one carries a portion of the load current during the freewheeling period. The power dissipation of each leg in this period is reduced to EQ. 4:

$$Psynfetfr = (IQ1^2 + IQ2^2) \bullet \left(\frac{1-D}{2}\right) \bullet Rdsonsyn \quad \text{(EQ. 4)}$$

Comparing EQ. 3 to EQ. 4, we note that the INV_LOW scheme induces less power dissipation in the synchronous FETs by an amount of EQ. 5:

$$\Delta Psynfetfr = 2 \bullet IQ1 \bullet IQ2 \bullet (1-D) \bullet Rdsonsyn \quad \text{(EQ. 5)}$$

In addition, the INV_LOW scheme also helps cut down the conduction losses in the primary FETs since the primary has less reflected secondary current, which decreases with the difference between IQ1 and IQ2, as shown in EQ. 6:

$$Ip \approx \frac{Is}{N} = \frac{IQ1 - IQ2}{2N} \quad \text{(EQ. 6)}$$

Although the INV_LOW scheme is a better choice from the power dissipation standpoint, the user should pay special attention to the impact of having on overlap between both synchronous FETs during the freewheeling period in current share, light load, start up, and turn-off operations. Some discussions are presented in the *EXPERIMENTAL RESULTS* section.

Select Switching Frequency and Define Maximum Available Duty Cycle

Several things are considered when selecting an appropriate switching frequency for a particular application. The size of the converter (limited by sizes of magnetics components), the overall losses of magnetics components, the switching losses of power MOSFETs, the desired efficiency, the transient response, and the maximum achievable duty cycle are all considerations. An iterative process is required, monitoring changes of the above parameters, to obtain an optimum switching frequency for a particular application. Users can use equations presented in this paper to design a MathCAD worksheet, which will help obtain a rough idea of the range of optimum frequencies for their applications. Note that the higher the switching frequency is, the higher the loop bandwidth (typical 1/10 or higher of the switching frequency) can be realized, but the lower the maximum duty cycle is available.

In the initial design of the evaluation board, these parameters are pre-selected: Fsw=250kHz=Fclock/2, t_{DEAD}=200ns, and t_{RESDLY}=100ns. The maximum available duty cycle then can be calculated using EQ. 7 (Dmaxav=85%). The duty cycle defined in this application note is the ratio of the ON-time interval of a lower FET to one clock period.

$$Dmaxav = \left(1 - \frac{t_{DEAD} - t_{RESDLY}}{Fclock}\right) \quad \text{(EQ. 7)}$$

Define Turns Ratio

The primary-to-secondary turns ratio of the main transformer should be chosen as high as possible without exceeding the maximum available duty cycle (Dmaxav=0.85) at the minimum line (Vinmin=36V, or the input UV setpoint) and the rated load (Io=60A) situation. The higher the turns ratio is, the less the load current is reflected to the primary side, and the less the power losses are induced by the primary MOSFETs. The maximum allowable turns ratio can be calculated with EQ. 8 (Nmax=3.79).

$$Dmaxav = \frac{2 \bullet (Vomax + Vmisc + Vsynfet) \bullet N}{\left(Vinmin - Rdsonpri \bullet \frac{Io}{N}\right) - Vsynfet \bullet N} \quad \text{(EQ. 8)}$$

where Vsynfet = Io x Rdsonsyn/2 is the channel drop of the synchronous FETs at half of the load (assuming that the output load is split evenly into both synchronous FETs during the freewheeling period), Vomax is the maximum output voltage (3.63V), and Vmisc is the sum of the miscellaneous voltage drops including contact resistance, winding resistance, PCB copper resistance. The initial guess of Vmisc is 0.3V for having a safe margin. If the load (Io) conducts through only one synchronous FET during the freewheeling period, then EQ. 8 can be simplified to EQ. 9 (Nmax=3.77):

$$Dmaxav = \frac{2 \bullet (Vomax + Vmisc + 2 \bullet Vsynfet) \bullet N}{Vinmin - Rdsonpri \bullet \frac{Io}{N}} \quad \text{(EQ. 9)}$$

With the assumptions of Rdsonpri=25 x1.2mΩ (Tj=50^{0}C) and Rdsonsyn=1.125x1.13mΩ (Tj=50^{0}C), EQ. 9 produces Nmax=3.77. Since the size and height of the converter are limited to that of a telecom half brick, a planar transformer with a low number of turns on both the primary and secondary sides is required. Therefore, 7/2 and 11/3 turns ratio are preferred choices. A transformer with 7 primary turns and 2 secondary turns has been used in the reference design due to the availability of magnetic cores in stock. In fact, a transformer with 11/3 turns ratio is generally recommended.

Output Filter Design (Current Doubler)

The output L-C filter is normally defined based on requirements of the output ripple voltage (70mV) and the transient response (dVtr=150mV). In general, if the requirement of the transient response is met, then the output ripple voltage will be within the limit.

As a rule of thumb, the overall ripple current (dIo) should be no more than 20% of the rated load, and the output inductor value (for each one) can be defined by EQ. 10:

$$Lo = \frac{2 \bullet (Vo + 2 \bullet Vsynfet) \bullet (1 - D)}{dIo \bullet Fclock} \quad \text{(EQ. 10)}$$

The ripple current (dI) through each inductor can be calculated with EQ. 11:

$$dI = \frac{(Vo + 2 \bullet Vsynfet) \bullet (2 - D)}{Lo \bullet Fclock} \quad \text{(EQ. 11)}$$

The requirement of the transient response is the major factor of defining the maximum overall ESR of the output capacitors in EQ. 12. Note that this converter is designed to meet 150mV transients (dip/overshoot) for a 25% rated load step (ESR < 10mΩ).

$$ESR < \frac{dVtr}{Istep} \quad \text{(EQ. 12)}$$

The minimum required output capacitance (Co) can be estimated by EQ. 13 when limiting the output ripple voltage contributed by output capacitance to be no more than dV_{Co}.

$$Co = \frac{1}{dV_{Co}} \bullet \frac{dIo}{8 \bullet Fclock} \quad \text{(EQ. 13)}$$

In addition to meeting the requirements of ESR and Co, the output capacitors should be able to absorb the output RMS current, as defined in EQ. 14.

$$Iorms = \frac{dIo}{\sqrt{12}} \quad \text{(EQ. 14)}$$

The output voltage ripple can be conservatively approximated by EQ. 15. The first two terms (dV_{ESR} and dV_{ESL}) contributed by the equivalent series resistance (ESR) and the equivalent series inductance (ESL) of the output capacitors are the dominant ones and are normally accurate enough to estimate the ripple voltage. The last term (dV_{Co}) contributed by the output capacitance (Co) is normally much smaller and can be neglected since the peak of the dV_{Co} happens at the ripple current across zero and does not align with the peak of dV_{ESR}, as shown in Figure 15. The positive and negative peaks of the overall ripple voltage (sum of all three components) relative to the DC level is not symmetric (caused by dV_{Co} and dV_{ESL}) unless the converter operates at 50% duty cycle. This asymmetry between positive and negative peaks is not a big concern in most applications since both dV_{Co} and dV_{ESL} are generally very small compared to the ESR portion. Note that the DC level remains constant. Refer to [6] for more details.

$$Voripple \approx dIo \bullet ESR + \frac{ESL}{Lo} Vs + \frac{1}{Co} \bullet \frac{dIo}{8 \bullet Fclock} \quad \text{(EQ. 15)}$$

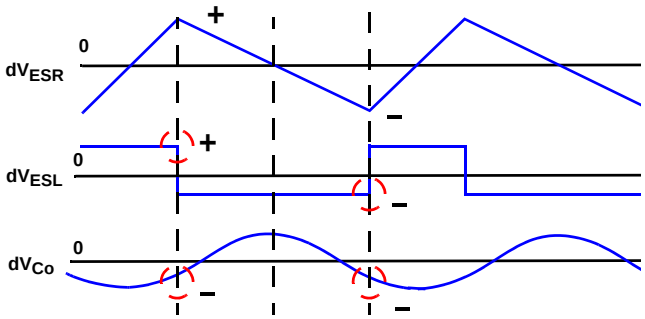


FIGURE 15. OUTPUT RIPPLE VOLTAGE COMPONENTS

The ESL of a capacitor is not usually listed in databooks. It can be practically approximated with EQ. 16:

$$ESL = \frac{1}{Co} \bullet \frac{1}{(2\pi \bullet Fres)^2} \quad \text{(EQ. 16)}$$

where Fres is the resonant frequency that produces the lowest impedance of the capacitor.

At the very edge of the transient, the equivalent ESL of all output capacitors induces a spike, as defined in EQ. 17 for a

given dI/dt, that adds on the top of the existing voltage undershoot/overshoot due to the ESR and capacitance.

$$\Delta V_{ESL} = ESL \bullet \frac{dI}{dt} \quad \text{(EQ. 17)}$$

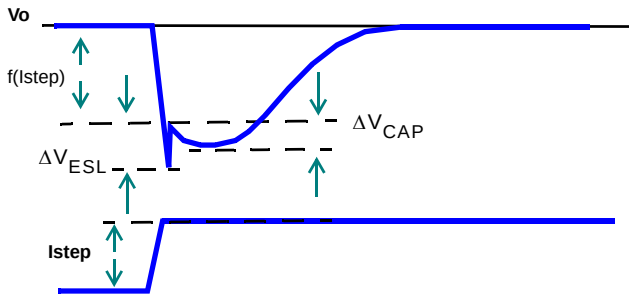


FIGURE 16. TYPICAL TRANSIENT RESPONSE WAVEFORM

Thus, the overall output voltage undershoot/overshoot due to load transients can be summarized in EQ. 18, in which the last term can be normally dropped out if the very edge of the transient is the dominant peak, as shown in Figure 16.

$$dVtr \approx f(Istep) + \Delta V_{ESL} + \Delta V_{CAP} \quad \text{(EQ. 18)}$$

where

$$f(Istep) = Istep \frac{\sqrt{1 + (2\pi \bullet f_c \bullet Co \bullet ESR)^2}}{2\pi \bullet f_c \bullet Co}$$

$$f(Istep) \approx Istep \bullet ESR \quad \text{for} \quad fc \geq \frac{1}{2\pi \bullet ESR \bullet Co}$$

$$f(Istep) \approx \frac{Istep}{2\pi \bullet f_c \bullet Co} \quad \text{for} \quad fc \leq \frac{1}{2\pi \bullet ESR \bullet Co}$$

$$\Delta V_{CAP} = \Delta V_{HUMP} \quad \text{for} \quad \text{step-up transients}$$

$$\Delta V_{CAP} = \Delta V_{SAG} \quad \text{for} \quad \text{step-down transients}$$

The last term in EQ. 18 is a direct consequence of the amount of output capacitance. After the initial spike, all the excessive charge is dumped into the output capacitors on step-down transients causing a temporary hump at the output, and the output capacitors deliver extra charge to meet the load demand on step-up transients causing a temporary sag before the output inductors catch the load. The approximate response time intervals for removal and application of a transient load are defined by dTn and dTp, respectively.

$$\Delta V_{HUMP} = \frac{Istep \bullet dTn}{2 \bullet Co} \quad \text{(EQ. 19)}$$

where $dTn = Lo\frac{Istep}{2Vo}$

$$\Delta V_{SAG} = \frac{Istep \bullet dTp}{2 \bullet Co} \quad \text{(EQ. 20)}$$

where $dTp = Lo\frac{Istep}{Vs - 2Vo}$

In low-profile, high current density, and high frequency applications, the required output capacitance defined in EQ. 13 might not be enough to deliver or absorb energy due to load transients. This could cause a significantly large undershoot/overshoot at the output. In the reference design, the loop bandwidth (f_c) is lower than the zero [1/(2π*ESR*Co)] of the output capacitors, which have low ESL transient component due to low dI/dt(1A/us), therefore, the required output capacitance can be roughly approximated with EQ. 21 [7].

$$Co \approx \frac{Istep}{2\pi \bullet f_c \bullet dVtr} \qquad fc \leq \frac{1}{2\pi \bullet ESR \bullet Co} \quad \text{(EQ. 21)}$$

Several lower-profile TAIYO YUDEN 100u, 6.3V capacitors (JMK212F107MM) have been used in the evaluation board to meet the electrical requirements of the above discussion and the height constraint of the converter.

Besides ESL, ESR, and capacitance of the output capacitors, other system parasitics such as board resistance and inductance should be included in the load transient analysis [6], which will not be discussed in this paper.

Electrical design parameters of the output inductors are summarized in EQs. 11, 22, & 23, which specify the ripple current, the peak current, and the RMS current of each inductor.

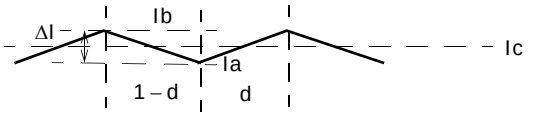
$$Iindpeak = \frac{Io + dI}{2} \quad \text{(EQ. 22)}$$

$$Iindrms = \frac{Io}{2} + \frac{dI}{\sqrt{12}} \quad \text{(EQ. 23)}$$

Calculations for Synchronous FETs (Q1 & Q2)

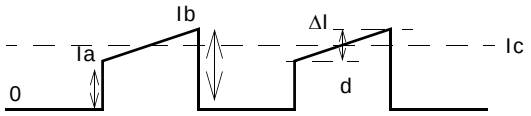
Some fundamental formulas that are used to calculate RMS values of triangular and trapezoid waveforms and to derive most equations in this paper are defined below.

CASE 1



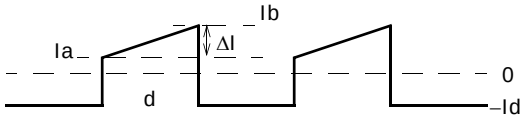
$$Irms1 = \sqrt{Ic^2 + \frac{\Delta I^2}{12}}$$

CASE 2



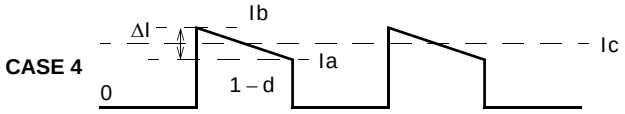
$$Irms2 = \sqrt{\left(Ic^2 + \frac{\Delta I^2}{12}\right) \bullet d}$$

CASE 3



$$Irms3 = \sqrt{Ic^2 \bullet (d - d^2) + \frac{\Delta I^2}{12} \bullet d}$$

In the power transfer period, one synchronous FET is turned off, and the other one is turned on conducting all the load



$$Irms4 = \sqrt{\left(Ic^2 + \frac{\Delta I^2}{12}\right) \bullet (1-d)}$$

WHERE $Ic = \frac{Ia + Ib}{2}$ $Id = Ic \bullet d$ $\Delta I = Ib - Ia$

current. The peak current through the FET is defined by the load current plus half of the output ripple current in EQ. 24. In this period, the RMS current through each FET can be calculated with EQ. 25 using Case 2 formula. Note that the duty cycle (D) is defined as the ratio of the ON-time interval of a lower FET over one clock period (twice of the switching period), which explains the 1/2 factor in the equation.

$$Isynpeak = Io + \frac{dIo}{2} \quad \text{(EQ. 24)}$$

$$Isynrmstr = \sqrt{\left(Io^2 + \frac{dIo^2}{12}\right) \bullet \frac{D}{2}} \quad \text{(EQ. 25)}$$

In the worst case, all the load current flows through one of the synchronous FETs during the freewheeling period (including the resonant and dead periods for simplicity), the RMS current through the FET can be estimated by EQ. 26.

$$Isynrmsfr = \sqrt{\left(Io^2 + \frac{dIo^2}{12}\right) \bullet \frac{1-D}{2}} \quad \text{(EQ. 26)}$$

Thus, the overall RMS current through one synchronous FET can be defined in EQ. 27, while the conduction losses of each synchronous FET can be calculated with EQ. 28.

$$Isynrms = \sqrt{Isysrmstr^2 + Isysrmsfr^2} \quad \text{(EQ. 27)}$$

$$Psynfet = Isynrms^2 \bullet Rdsonsyn \quad \text{(EQ. 28)}$$

As shown in EQs. 25 and 26, the higher the ripple current is, i.e., the lower the output inductances are, the higher the RMS currents are, and the higher the conduction losses of the synchronous FETs are.

In addition, the distribution factor (F_{DIST}) for IQ1 and IQ2 currents during the freewheeling period for the INV_LOW DRIVE scheme can be included in EQ. 26 for an accurate calculation:

$$F_{DIST} = \sqrt{(1-p)^2 + p^2} \quad \text{(EQ. 29)}$$

where p is the percentage of load current through one of the synchronous FETs. A guess of p can made by looking at the primary freewheeling current, as shown in the EXPERIMENTAL RESULTS section. For the other two drive schemes, F_{DIST} is one.

In the SYNC DRIVE scheme, both synchronous FETs are turned off during the dead time period. The freewheeling current flows through the body diodes of the FETs, and any external schottky diodes. In the worst case, the freewheeling current flows through only one leg, and the average current for the dead time can be estimated by EQ. 30, where t_{DEAD} is the dead time and t_{RESDLY} is the resonant time.

$$Isyndeadavg = \frac{t_{DEAD}}{4 \bullet T}\left(Io + \frac{dIo(t_{DEAD} + t_{RESDLY} - 0.5T(1-D))}{(1-D) \bullet T}\right) \quad \text{(EQ. 30)}$$

An additional term "*Isyndeadavg x Vdsyn*" should be added to EQ. 28 if the SYNC DRIVE scheme is implemented. *Isynrmsfr* however would be slightly smaller.

The maximum voltage across the synchronous FET can be approximated with EQ. 31, adding 30% margin for the ringing on the rising edge.

$$Vsynmax = \frac{Vinmax}{N}(1 + 0.3) \quad \text{(EQ. 31)}$$

The synchronous FETs should be selected such that the V_{DS} rating and power rating of the MOSFETs are greater than *Vsynmax* and *Psynfet,* respectively. Four 30V Siliconix Si4842DY MOSFETs are used for each leg. Note that any switching losses, which will be discussed later, should be included in the calculation to define the maximum power dissipation.

Calculations for Primary Switches (QA, QB, QC, & QD)

The peak current through the primary winding happens at the end of the active period, as defined in EQ. 32

$$Ipripeak = \frac{Io + dI}{2N} + \frac{Imag}{2} \quad \text{(EQ. 32)}$$

$$Imag = \frac{(Vin - 2 \bullet Ip \bullet Rdsonpri) \bullet D}{Lmag \bullet Fclock} \quad \text{(EQ. 33)}$$

EQ. 33 defines the peak-to-peak magnetizing current. The RMS current through the power switches in the active period can be estimated by EQ. 34, which also defines the overall RMS current through a lower FET.

$$Iprirmstr = \sqrt{\left(\left(\frac{Io}{2N}\right)^2 + \frac{dIp^2}{12}\right) \bullet \frac{D}{2}} \quad \text{(EQ. 34)}$$

where $dIp = \frac{dI}{N} + Imag$

If there is a time delay Td to turn on the lower FET after its output capacitance is completely discharged, i.e, the resonant delay is set longer than is necessary, then the current will flow through the body diode of the lower FET, which has an average value defined in EQ. 35.

$$Ipriavgres = \left(\frac{Io}{2N} + \frac{Imag}{2} + \frac{dI(D + Td/T)}{2N(2-D)}\right) \bullet \frac{Td}{2T} \quad \text{(EQ. 35)}$$

The freewheeling current flows through the channel and the body diode of upper FETs in alternate freewheeling periods and at alternate directions. The RMS current through the channel can be calculated with EQ. 36. The average current through the body diode of the upper FET can be estimated with EQ. 37.

$$Iprirmsfr = \sqrt{\left(\left(\frac{Io}{2N} + \frac{dI}{2N(2-D)} + \frac{Imag}{2}\right)^2 + \frac{dI^2(1-D)^2}{12N^2(2-D)^2}\right) \bullet \frac{1-D}{2}} \quad \text{(EQ. 36)}$$

$$Ipriavgfr = \left(\frac{Io}{2N} + \frac{Imag}{2} - \frac{dI}{2N(2-D)}\right) \bullet \frac{1-D}{2} \quad \text{(EQ. 37)}$$

Thus, the overall RMS current through the channel of each upper FET is defined in EQ. 38:

$$Iprirms = \sqrt{Iprirmstr^2 + Iprirmsfr^2} \quad \text{(EQ. 38)}$$

With all the above RMS and average current information, the conduction losses of each power switch can be roughly estimated with EQs. 39 and 40. As shown in EQs. 34 and 36, the higher the inductor ripple current and the magnetizing current are, i.e., the lower the output inductance and the magnetizing inductance are, the larger the RMS currents are, the higher the power losses would be induced by the primary switches.

$$Pupfet = Iprirms^2 \bullet Rdsonpri + Ipriavgfr \bullet Vd \quad \text{(EQ. 39)}$$

$$Plowfet = Iprirmstr^2 \bullet Rdsonpri + Ipriavgres \bullet Vd \quad \text{(EQ. 40)}$$

Four 100V Siliconix SUD40N10 MOSFETs are selected for the bridge switches such that the ratings of the device are greater than *Pupfet, Plowfet,* and the *maximum input voltage.* Note that any switching losses, which will be discussed later, should be included in EQs. 39 and 40 to define the maximum power dissipation of the primary switches, which limits the MOSFET selection.

Input Filter Design

The input pulsating current filtered by the input capacitors has an RMS value in EQ. 41, while the minimum required input capacitance is defined in EQ. 42.

$$Iinrms = \sqrt{\left(\frac{Io}{2N}\right)^2 \bullet (D - D^2) + \frac{(dIp)^2}{12} \bullet D} \quad \text{(EQ. 41)}$$

$$Cin = \frac{Io}{2N} \bullet (D - D^2) \bullet \frac{T}{dVincap} \quad \text{(EQ. 42)}$$

The $dV_{IN}cap$ is the acceptable input ripple voltage contributed by the amount of input capacitance, of which is the input capacitors (ITW Patron capacitors in the reference design) that filter most of pulsating currents. The maximum value of EQ. 41 happens at D~0.5, while the maximum value of EQ. 42 happens at D=0.5. Several lower-profile ITW Paktron capacitors (105K100ST2814) and an external capacitor have been used in the evaluation board. If a hold up time (t_{HOLDUP}) is required when the input line is momentarily disconnected, then EQ. 43 helps define the required hold up capacitance:

$$Cin = \frac{2Po \bullet t_{HOLDUP}}{\eta \bullet (Vin^2 - V^2_{HOLDUP})} \quad \text{(EQ. 43)}$$

or

$$Cin \approx \frac{Po \bullet t_{HOLDUP}}{\eta \bullet Vin \bullet \Delta Vin}$$

where

$$\eta = \text{Efficiency}$$

$$\Delta Vin = Vin - V_{HOLDUP}$$

The overall input voltage ripple induced by the ESR and capacitance of the input capacitors can be estimated with EQ. 44. In addition, the spikes caused by the ESL of the input capacitors should be decoupled with lower ESL ceramic capacitor.

$$Vinripple = \frac{Io}{2N} \bullet (D - D^2) \bullet \frac{T}{Cin} + ESRin \bullet Ipripeak \quad \text{(EQ. 44)}$$

Furthermore, for a low EMI level performance, an additional L-C filter might be required in the front end. However, the combination of both ZVS full bridge and current doubler topologies helps reduce the size of this input EMI filter.

Switches Losses and Driver Losses

In general, switching losses are an insignificant portion compared to conduction losses of the power switches if ZVS transitions are achieved. Since the commutating inductances store the peak energy to swing the output capacitance of the upper FET from V_{IN} to zero volt at the beginning of the freewheeling period before the upper FET is turned on, therefore, the upper FETs are lossless at turn on transitions. At the end of freewheeling period, the commutating inductances store the least energy, which might not be enough (especially in high line and/or low load conditions) to swing the output capacitance of the lower FET to zero volt before they are turned on. The turn-on losses of the lower FETs can be approximated with EQ. 45. The turn-off losses of primary switches can be minimized with a high speed driver such as Intersil HIP2100.

$$Ppriswon = \frac{1}{2} V_{on} \bullet I_{on} \bullet t_{on} \bullet Fsw \quad \text{(EQ. 45)}$$

When the lower FET is turned off, its corresponding upper FET is clamped to V_{IN} in a very short time. The corresponding synchronous FET is turned on when the voltage across the secondary winding vanishes, therefore, there are no turn-on switching losses for the synchronous FETs. The resonant delay and the delay caused by the leakage inductance to have any voltage across the

secondary winding, as illustrated in EXPERIMENTAL RESULTS, prior to turn off the synchronous FET, help to achieve ZVT for the synchronous FETs at turn off. To achieve ZVT as discussed in previous lines, the synchronous FET drivers however should have high current capability with little propagation delays such as MICREL 9A MIC4421 inverting drivers or better. The conduction losses and reverse recovery losses of body diodes of the synchronous FETs at turn on or off are not discussed here, but they do show up in Figure 35.

Note that the drivers with high current capability can shorten the transition time and reduce the switching losses.

The driver losses due to the gate charge of the MOSFETs should be investigated thoroughly to prevent over stressing. The switching losses of both primary and secondary drivers and its corresponding average driver current due to the gate charge can be estimated with EQs. 46 and 47, respectively,

$$Pdr = \frac{Qg}{V_{GS}} \bullet Vcc^2 \bullet Fsw \quad \text{(EQ. 46)}$$

$$Idr = \frac{Qg}{V_{GS}} \bullet Vcc \bullet Fsw \quad \text{(EQ. 47)}$$

where Qg and V_{GS} are defined in the MOSFET datasheet.

Define Requirements of Main Transformer

This section summarizes major design requirements of the main transformer at the switching frequency.

The turns ratio of the transformer is derived from EQ. 9 while EQ. 32 defines the peak current through the primary winding. The RMS current through the primary winding is defined in EQ. 48.

$$Iprms = \sqrt{2} \bullet Iprirms \quad \text{(EQ. 48)}$$

The current through the secondary winding is only half of the load, and its RMS currents in both transfer and freewheeling periods can be defined by EQs. 49 and 50, respectively. The overall RMS current through the secondary winding can be calculated with EQ. 51.

$$Isrmstr = \sqrt{\left(\frac{Io^2}{4} + \frac{dI^2}{12}\right) \bullet D} \quad \text{(EQ. 49)}$$

$$Isrmsfr = \sqrt{\left(\left(\frac{Io}{2} + \frac{dI}{2(2-D)}\right)^2 + \frac{dI^2(1-D)^2}{12(2-D)^2}\right) \bullet (1-D)} \quad \text{(EQ. 50)}$$

$$Isrms = \sqrt{Isrmstr^2 + Isrmsfr^2} \quad \text{(EQ. 51)}$$

The magnetizing inductance (Lmag) is determined by the number of turns of primary winding, the core geometry, and the air gap. The Lmag however should not be designed too low. If it is too low, high power dissipation will be introduced in the primary switches, and too much ramp will be added to the current ramp signal, which makes the supply look voltage mode. A reasonable small Lmag can assist ZVS and decrease any noise sensitivity problems. Around 100uH is a start point for telecom brick applications. In addition, it is recommended to have a small gap in the transformer stabilizing the magnetizing inductance so that the magnetizing current can be within a controllable range.

The leakage inductance is not an issue in the design. In fact, it is part of the commutating inductance to assist ZVS using its stored energy. Too much leakage inductance however will lower the effective duty cycle, resulting in a lower turns ratio.

The primary-to-secondary capacitance should be minimized since it robs energy from the ZVS elements increasing the resonant time and decreasing the maximum available duty cycle and the ZVS load range.

As far as the size of the transformer is concerned, it varies with applications. In the reference design, the transformer is limited to less than 0.5 inch height, being able to fit into a telecom half brick.

Determine Commutating Inductance

The required external commutating inductance is determined by the slower transition (from passive to active period) since the commutating inductance stores the least energy for ZVS. The ZVS condition is that the energy stored in the commutating inductance, defined in EQ. 52, should be greater than the energy stored in the primary capacitance, defined in EQ. 53. Thus, the required external commutating inductance can be roughly estimated with EQ. 54. Refer to [1] for detailed discussion.

$$E_L = \frac{1}{2}(L_{ext} + L_k) \bullet (Imag + Ip)^2 \quad \text{(EQ. 52)}$$

$$E_C = \frac{1}{2}(2Coss + Cp) \bullet Vin^2 \quad \text{(EQ. 53)}$$

$$L_{ext} < \frac{Vin^2 \bullet (2 \bullet Coss + Cp)}{(Imag + Ip)^2} - L_k \quad \text{(EQ. 54)}$$

Note that the output capacitance (Coss) of the MOSFET varies with the drain to source voltage, and the primary current (Ip) at the end of the freewheeling period determined by the turns ratio and current distribution factor F_{DIST}. The external commutating inductor however would be better defined in the real circuits by trial and errors.

Control Loop Design

The secondary-referenced, peak current control is implemented in the converter design. Two pulse transformers pass the PWM information of the full-bridge controller (ISL6551) to two high current half-bridge drivers (HIP2100s) in the primary. A current transformer is to feed the primary current information to the full-bridge controller, as a feed-forward loop. The control loop is closed by an error amplifier, for loop compensation purpose, cascaded with a

differential amplifier, for remote sense purpose. Figure 17 shows the block diagram of the overall closed-loop system.

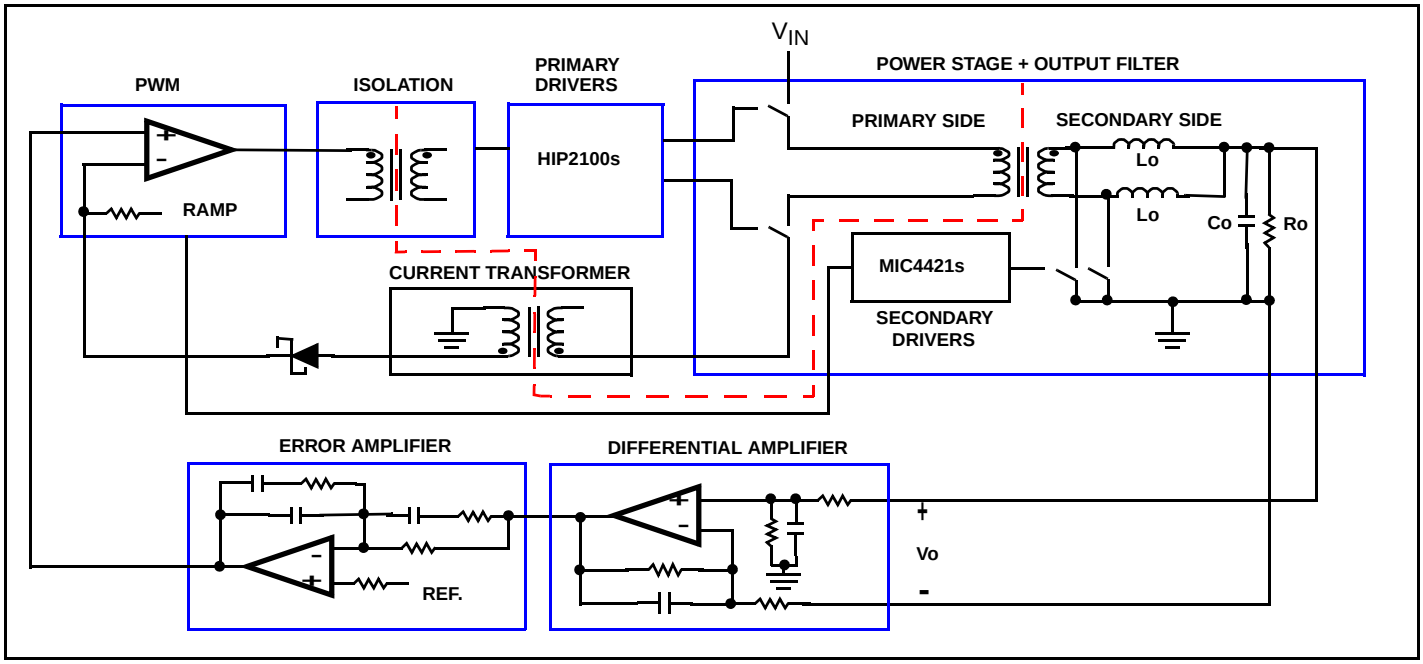


FIGURE 17. BLOCK DIAGRAM OF CLOSED-LOOP SYSTEM

This peak current mode controlled system can be simplified as shown in Figure 18, for setting up an initial feedback compensation, and EQ. 55 defines the approximate open-loop transfer function. The factor “2” in the equation is due to that only half of the load is sensed by the current transformer.

$$Hopen(S) = \frac{2N \bullet Ncs}{Rcs} \bullet Hd(S) \bullet He(S) \bullet Zo(S) \qquad \text{(EQ. 55)}$$

Designers should initially set a low cut-off frequency, such as 1kHz, system loop with this simplified model as a start point and then continue to modify the loop under a stable condition with a design tool such as a Venable System. Note that the model does not include the slope compensation component and does not account for subharmonic oscillation phenomenon in current-mode controlled converters. The high-frequency correction term given by EQ. 56 will account for the phenomenon [4].

$$Hs(S) = \frac{1}{1 + \frac{S}{Wn \bullet Qp} + \frac{S^2}{Wn^2}} \qquad \text{(EQ. 56)}$$

$$Wn = \pi \bullet Fsw \qquad Qp = \frac{1}{\pi \bullet \left(Mc \bullet \left(1 - \frac{D}{2}\right) - 0.5\right)}$$

$$Mc = 1 + \frac{Se}{Sn}$$

$$Se = Sm + Sin \qquad Sn = \frac{Vs(2 - D)}{2Lo} \bullet \frac{Rcs}{N \bullet Ncs}$$

A better representation of the open loop transfer function for the overall system is defined in EQ. 57:

$$Hopen2(S) = Hopen(S) \bullet Hs(S) \qquad \text{(EQ. 57)}$$

Refer to Vatché’s Article [3] for another way of modeling the loop.

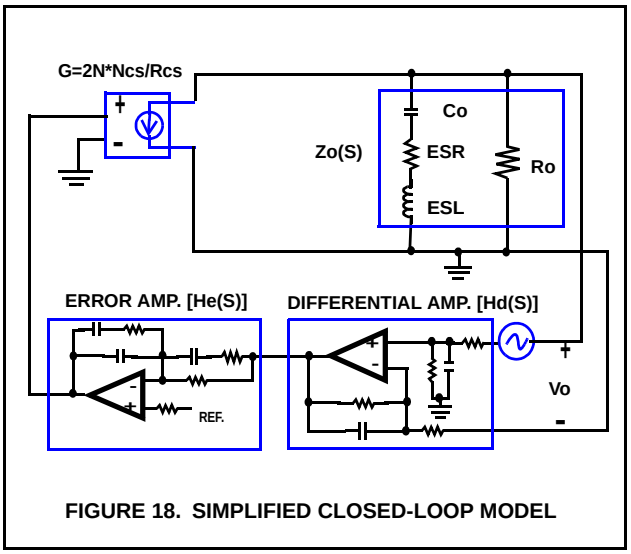


FIGURE 18. SIMPLIFIED CLOSED-LOOP MODEL

Special Notes for Configuring the ISL6551

The controller can be easily configured using Table 1 in the ISL6551 datasheet. In this section, several things that require the users' attention are highlighted. For a detailed configuration, please refer to the device datasheet.

- For a tighter tolerance of operating frequency, a 5% NPO ceramic capacitor is recommended for CT.
- The resonant delay should not be too long, otherwise, the residual resonant current will flow through the body diode of the lower FET and additional losses are generated. The maximum available duty cycle will also be decreased.
- The amount of slope contributed by the magnetizing current is given by EQ. 58, while the amount of slope contributed by the internal circuit of the IC is given by EQ. 59. The overall slope added to the current ramp signal is the sum of these two equations. An internal ramp (programmed by a R_RA resistor) might not be required if the ramp contributed by the Lmag is enough for the slope compensation.

$$Sm = \frac{Vin}{Lmag} \bullet \frac{Rcs}{Ncs} \quad \text{(EQ. 58)}$$

$$Sin = \frac{BGREF}{R\neg RA} \bullet \frac{1}{500 \cdot 10^{-12}} \quad \text{(EQ. 59)}$$

- The voltage at ISENSE pin should be scaled appropriately such that the desired peak current equals or less than Vclamp-200mV-Vramp, as defined in EQ. 60. In addition, the turns ratio of the current transformer, *Ncs*, should be selected so that power losses at Rcs (current sense resistor) at the lowest line and the maximum output load is less than the power rating of one or two SMT0805 resistors so that minimum losses are induced by the Rcs and less board space is required.

$$Rcs \leq \frac{(Vclamp - 200mV) - \frac{Sin \bullet D}{Fclock}}{\frac{Ipripeak}{Ncs}} \quad \text{(EQ. 60)}$$

- The peak current limit set by the PKILIM is lower than the cycle-by-cycle current limit controlled by the Vclamp in the reference design for two reasons: 1) ISENSE (at full load) has to be designed no greater than the minimum reference voltage (2.64V) at EANI pin, otherwise, the monotonic output startup at full load cannot be achieved; and 2) high losses can be introduced if ISENSE (at full load) is pushed up to the Vclamp (3.75V) with a low turns ratio (150:1) current transformer. In the reference design, the ISL6550 would latch the ISL6551 off in overload conditions.
- The voltage at EANI and EAO should be designed lower than the Vclamp, otherwise the output will be regulated at Vclamp and the output load will be limited to the equivalent current voltage. Since both EANI and EAO are clamped by the same voltage (Vclamp), the output voltage would dip if the current ramp exceeds the EAO during the startup, especially for applications with constant current load. Hence, the EANI should be set higher than EAO, otherwise, the output voltage cannot have a monotonic startup. (This problem could be solved by setting the soft start at the EANI pin instead of the CSS pin allowing the clamping voltage to come up at a very high speed.) In the reference design, the synchronous FETs are turned off during start up achieving monotonic rise for resistive load applications. The FETs are turned on after a certain load and then cannot be turned off even back to no-load, which achieves a better dynamic performance. Users however can completely remove the current peak detecting circuits (D23..., they are only handy circuits for users to turned off the synchronous FETs whenever necessary) and rely on the R134 and C132 to achieve monotonicity for the output voltage startup.
- The BGREF should be kept as clean as possible, otherwise, the over current trip point set at the PKILIM would be lower than is expected due to the noise/ripple at the bandgap reference. A low ESR 0.1uF ceramic capacitor is recommended for decoupling. Due to an internal race condition, the ISL6551 cannot work properly without a 399kW resistor connecting between BGREF and VDD pins. For additional reference load (no more than 1mA), this pull-up resistor should be scaled accordingly such that the converter can start up properly. In other words, VDD should source at least the amount of BGREF external load current through the pull-up resistor.
- The SHARE pin requires a 30kΩ load. A low ESR 0.1uF or higher ceramic capacitor should be connected to the CS_COMP pin to design a much lower current loop bandwidth than that of the voltage regulation loop in current share operation.
- It is critical that the input signal to ISENSE decays to zero prior to or during the clock dead time, otherwise, it could cause severe errors in the signal reaching the PWM comparator. Examine the current ramp tail of the converter at maximum duty cycle and full load operations, and extend the dead time to reset the current ramp tail if oscillations occur. The C61 in the peak current detecting circuits (page 6 of the schematics) causes a tail at the current ramp. If it is removed, a smaller dead time can be used while maintaining proper operations.

Layout Considerations

- When doing the layout, users should pay special attention to the VSS and PGND returns (Analog Ground and Power Ground). VSS is the reference ground, the return of VDD, of all control circuits and must be kept as clean as possible from all switching noises. It should be connected to the PGND in only one location as close to the IC as practical. For a secondary control system, it should be connected to the net after the output capacitors, i.e., the output return pinouts. For a primary control system, it should be

connected to the net before the input capacitors, i.e., the input return pinouts.

- Heavy copper traces should be connected to the bias pins (VDD, VDDP1, VDDP2) and the ground pins (VSS and PGND) for heat spreading.
- The copper routings from the drivers to the FETs should be kept short and wide, especially in very high frequency applications, to reduce the inductance of the traces so that the drive signals can be kept clean, no bouncing.
- In the MLFP package, the pad underneath the center of the IC is a “floating” thermal substrate. The PCB “thermal land” design for this exposed die pad should include thermal vias that drop down and connect to buried copper plane(s). This combination of vias for vertical heat escape and buried planes for heat spreading allows the MLFP to achieve its full thermal potential. It is recommended to connect this pad to the low noise copper plane Vss.
- For additional tips, please refer to *“PCB Design Guidelines For Reduced EMI”* [5].

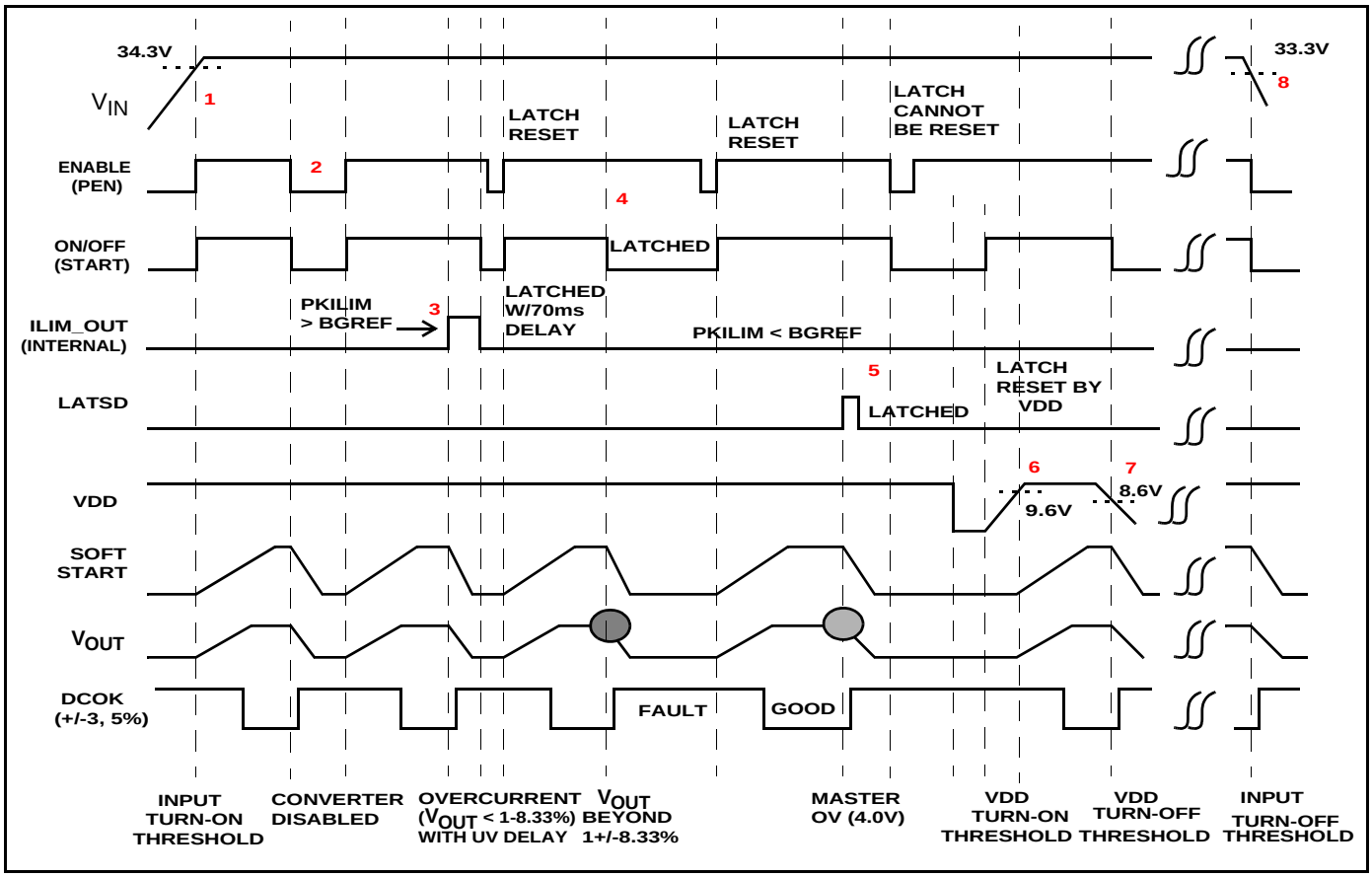


FIGURE 19. SHUTDOWN TIMING DIAGRAM OF THE CONVERTER

Shutdown Timing Diagram of the Converter

INPUT UV (1): With all the biases powered up and the mechanical switch at the PEN pin turned on, the converter is enabled after the input reaches its turn-on threshold (34.3V). The output voltage rises to its regulation point following the soft start. The soft start capacitor continues to be charged up to the clamping voltage (Vclamp). The DCOK is pulled low indicating “GOOD” once the output reaches within -3% of the set point.

ENABLE (2): When the PEN pin is pulled low, the soft start capacitor is discharged very quickly and all the drivers are disabled. The DCOK is pulled high indicating “FAULT” when the output voltage is discharged below -5% of the set point. When the PEN pin is released, a soft start is initiated.

OVER CURRENT (3): If the output of the converter is over loaded, i.e, the PKILIM is above the bandgap reference (BGREF), the soft start capacitor is discharged quickly and all the drivers are turned off. Once the output voltage is below -8.33% of the regulation point, the capacitor of the under-voltage delay set at ISL6550 is then charged up, and the START is latched when the voltage at the capacitor reaches 5V. The ISL6551 controller is quickly shut down by the START. If the over load is removed and the converter can return to normal operation within the under-voltage delay

(around 70mS), then the START will not be latched. The latch can be reset by the PEN signal, which is controlled by the input voltage, the mechanical switch, and the thermal condition of the converter. If latching the converter off in overload conditions is not allowed, then version B of ISL6550 can be used. Then the converter would be running in hiccup mode in overload conditions.

OUPUT UV & LOCAL OV (4): If the output voltage is beyond +/-8.33% of the set point and does not reach the master OV setpoint (4.19V) for any reason, the START is then latched, so is the converter. The latch can be reset by the PEN.

OUPTUT MASTER OV (5): If the master OV circuit is triggered, the LATSD is pulled high and latches the controller off. The latch can be reset ONLY by cycling VDD. It CANNOT be reset by toggling ENABLE (PEN).

RESET LATCH (6): The soft start capacitor starts to be charged after the VDD increases above the ISL6551 and ISL6550 turn-on thresholds.

VDD UV LOCKOUT (7): The IC is turned off when the VDD is below the ISL6551 and ISL6550 turn-off thresholds. The soft start is reset.

INPUT UV LOCKOUT (8): When the input voltage is below its turn-off threshold 33.3V, the converter is disabled and latched off. The soft start is reset.

Summary of Design

Table 1 is the BDAC output programming code.

TABLE 1. BDAC OUTPUT PROGRAMMING CODE

#	VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
0	1	1	1	1	1	2.642
1	1	1	1	1	0	2.674
2	1	1	1	0	1	2.706
3	1	1	1	0	0	2.738
4	1	1	0	1	1	2.770
5	1	1	0	1	0	2.801
6	1	1	0	0	1	2.833
7	1	1	0	0	0	2.865
8	1	0	1	1	1	2.897
9	1	0	1	1	0	2.929
10	1	0	1	0	1	2.961
11	1	0	1	0	0	2.993
12	1	0	0	1	1	3.025
13	1	0	0	1	0	3.057
14	1	0	0	0	1	3.089
15	1	0	0	0	0	3.121
16	0	1	1	1	1	3.153
17	0	1	1	1	0	3.185
18	0	1	1	0	1	3.216
19	0	1	1	0	0	3.248
20	0	1	0	1	1	3.280
21	**0**	**1**	**0**	**1**	**0**	**3.312**
22	0	1	0	0	1	3.344
23	0	1	0	0	0	3.376
24	0	0	1	1	1	3.408
25	0	0	1	1	0	3.440
26	0	0	1	0	1	3.472
27	0	0	1	0	0	3.504
28	0	0	0	1	1	3.536
29	0	0	0	1	0	3.568
30	0	0	0	0	1	3.599
31	0	0	0	0	0	3.631

Table 2 summarizes major design parameter requirements. Most components are selected or designed based on these values. Users should generate a similar table for their applications and select components with derating guideline of the datasheet or their own companies.

TABLE 2. DESIGN PARAMETER REQUIREMENTS

PARAMETER	CONDITION	VALUE	UNIT
DUTY CYCLE AND SWITCHING FREQUENCY			
Dmaxav	t_{DEAD}=200ns, t_{RESDLY}=100ns, Fsw=250kHz	85	%
Fsw	CT=180pF	235	kHz
INPUT CAPACITORS			
Cin	D=0.5, dVincap=1.65V	3	uF
Iinrms	Vin=48V, D~0.5, Vo=3.63V	5.4	A
OUTPUT CAPACITORS			
Co	f_c=Fsw/10=23.5kHz	677	uF
dIo	Lo=0.8uH, Vin=75V, Vo=3.63V	12.9	A
Iorms	Vin=75V, Lo=8uH, Vo=3.63V	3.4	A
ESR	dVtr = 150mV @ 25% Load Step	10	mΩ
OUTPUT INDUCTORS			
dI	Lo=0.8uH, Vin=75V, Vo=3.63V	16.3	A
Iindpeak	Io=60A, Vin=75V, Vo=3.63V assuming the load evenly distributed between both output inductors	38.2	A
Iindrms	Io=60A, Vin=75V, Vo=3.63V assuming the load evenly distributed between both output inductors	34.7	A

TABLE 2. DESIGN PARAMETER REQUIREMENTS (Continued)

PARAMETER	CONDITION	VALUE	UNIT
MAIN TRANSFORMER			
Imag	Lmag=60uH (Limited by Core), Vo=3.63V, Fsw	0.92	A
Ipripeak	Vin=75V, Vo=3.63V	11.4	A
Iprms	VIN=75V, Vo=3.63V	9.9	A
Isrms	Vin=75V, Vo=3.63V	33.4	A
N	Limited by Core	7:2	-
Nmax	Vin=36V, Vomax=3.63V, Vmisc=0.3V, Dmaxav=0.85	3.77	-
CURRENT TRANSFORMER			
Ncs		150:1	-
PRIMARY SWITCHES			
Ipriavgfr	Vin=75V, Vo=3.63V	3.6	A
Ipriavgres	Vin=36V, Vo=3.63V	0.095	A
Iprirms	Vin=75V, Vo=3.63V	4.94	A
Iprirsmtr	Vin=75V, Vo=3.63V	2.57	A
Iprirsmtr	Vin=36V, Vo=3.63V	3.71	A
Pdr	Each Primary Driver Vcc(max)=13.2, Qg=50nC x 2 at V_{GS}=10V, Two Siliconix SUD40N10-25	0.42	W
Pupfet	Vin=75V, Vd=0.78V, Vo=3.63V	4.1	W
Plowfet	Vin=36V, Vd=0.75V, Vo=3.63V with Td=40n. The worse case could be at Vin=75 due to switching losses	0.90	W
SYNCHRONOUS FETs			
Isynpeak	Vin=75V, Vo=3.63V	66.4	A
Isynrms	Vin=75V, Vo=3.63V	42.5	A
Pdr	Each Secondary Driver Vcc(max)=13.2V, Qg=30nC x 4 at V_{GS}=4.5V Four Siliconix Si4842DY	1.09	W
Psynfet	Vin=75V, Four Siliconix Si4842DYs. Body Diode Conduction and Recovery Losses are not Included Here	2.3	W

Table 3 summarizes a rough full load power losses analysis for 3.3V output of the reference design.

TABLE 3. FULL LOAD POWER LOSSES ANALYSIS

ELEMENTS	POWER DISSIPATION AT 60A LOAD		
	36V	48V	75V
CALCULATION CONDITIONS			
Clock Dead Time	175ns		
Resonant Time	50ns		
Td	40ns		
Switching Frequency	235kHz		
Transformer Turns Ratio	7:2		
Magnetizing Inductance	60uH		
Output Inductor	0.8uH		
MOSFET Rds(on) Value	at Tj=50^0C		
PRIMARY SIDE			
Upper FETs Conduction	2.616W	3.371W	4.179W
Lower FETs Conduction	0.819w	0.630W	0.427W
Primary Winding Copper	1.023W	1.087W	1.155W
Current Sense Winding	0.110W	0.082W	0.053W
Pinouts of Current Sense Transformer	***1.521W***	***1.141W***	***0.731W***
Full Bridge Drivers	0.677W	0.677W	0.677W
SECONDARY SIDE			
Synchronous FETs Conduction	2.290W	2.293W	2.296W
Secondary Winding Copper	1.005W	1.054W	1.106W
Output Inductors Copper	2.575W	2.642W	2.716W
Synchronous Drivers	1.805W	1.8056W	1.805W
Current Sense Resistor	0.122W	0.095W	0.063W
Current Sense Rectifiers	0.075W	0.055W	0.034W
OTHERS			
R22	**0.656W**	**0.697W**	**0.741W**
PCB Copper	1.096W	1.126W	1.157W
Biases other than Drivers	0.360W	0.360W	0.360W
Guess Overall Magnetics Core (20% of Conduction)	0.942W	0.973W	1.006w
Miscounted Switching Losses, Body Diodes Conduction and Reverse Recovery Losses at Bridge FETs and Synchronous FETs, Contact Resistance, Clamping Losses, and Error	3.914W	3.492W	5.625W
TOTAL	**27.33W**	**27.87W**	**31.03W**

Thoughts After Design

Users can use these thoughts to make some possible improvements of the reference design.

1. The input capacitors (C13-C15) can be replaced with ceramic capacitors with smaller footprints such as TDK SMT1812 C4532X7R2A105M.
2. The output capacitors (2220 footprint) can be replaced with smaller footprint 1812 capacitors such as the TDK new product, C4532X5R0J107M.
3. The main transformer (T2) and output chokes (L2 and L3) are too tall for brick applications with current design form factors. They can be integrated with the PCB to save board space and reduce losses. An external inductance however might be required for ZVS operation because an integrated PCB transformer would have a very low leakage inductance, which could not store enough energy to swing the primary capacitance.
4. The current sense transformer (T4) runs hot due to its high pinout resistance (more than 10mΩ) and it eats up too much space, users should redesign the current sense transformer for better form factor (like J-lead) and thermal performance. In addition, it cannot be placed symmetrically in the board due to space constraint. In the applications of no space limitation, it should be relocated.
5. The overall layout can be improved by removing test point connectors (TP1-TR34), which are not required in the real design.
6. The peak current limit set by the PKILIM is lower than the cycle-by-cycle current limit controlled by the Vclamp, i.e., the PKILIM is triggered earlier than the cycle-by-cycle limit.Thus, the reference-based clamp circuit, for the cycle-by-cycle current limit accuracy, is not necessary.
7. Users can completely remove the current peak detecting circuits (D23, C61..., they are only handy circuits for users to turned off the synchronous FETs whenever necessary) and rely on the R134 and C132 to achieve monotonicity for the output voltage startup. The dead time then can be cut down.
8. R22 can be replaced with a wire for users to look at the primary current. It is not an ideal zero Ohm, couple milli-Ohms could induce 0.2% or higher less efficiency.
9. For a narrower range input (48V+/-10%) and/or a lower output voltage application, a higher turns ratio (4:1) can improve the efficiency as much as 1%.

Design Tips For Using ISL6551

1. Since the upper FETs carry not only active currents through their channels but also freewheeling currents through their body diodes, the power dissipation of the upper FETs (QA and QD) is higher than the lower FETs (QC and QB), which can be replaced with smaller size of MOSFETs such as SO-8 in moderate primary current applications. The switching losses however should be taken into account.
2. With assistance of a pre-regulator, the post full-bridge regulator can be designed to operate at a fixed maximum duty cycle (~100%). Thus, the freewheeling currents flow through the body diodes of the upper FETs in the shortest period. The power dissipation of the upper FETs therefore can be reduced significantly in high primary current applications. The narrower the input line range is, the higher the turns ratio of the main transformer can be chosen, and the higher the efficiency can be achieved. The power losses and cost of the pre-regulator however should be taken into account for overall performance evaluation.
3. An external commutating inductor can be added in series with the primary side of the transformer to assist ZVS transitions if the energy stored in the leakage inductance and the magnetizing inductance is less than the energy stored in the output capacitance (2*Coss) of the power switches, the primary capacitance (Cp), and any external capacitance. Extending the ZVS range with an external inductor is at the penalties of additional component cost and less effective duty cycle resulting in a lower turns ratio, which adds power losses to the primary side.
4. An external capacitor in parallel with the primary side of the transformer can help lower the dV/dt and the noise level without introducing additional losses when the zero-voltage switching is still retained. The penalties, as discussed above, still hold.
5. External high current bridge drivers cascading with the ISL6551 drivers help absorb the power that supposed to dissipate in the controller so that the controller is not over stressed in high gate capacitive load applications, which extends the application range in a much higher power level.
6. The higher the switching frequency is, the higher the system closed-loop bandwidth can be realized, and the lower the input and output capacitances are required for overcoming load transients. This, however, comes at the cost of the efficiency.
7. The current ramp signal to ISENSE should decay to zero prior to or during the clock dead time. Hence, the dead time should be set long enough to reset the trailing-edge tail of the current ramp at the maximum duty cycle operation, otherwise, oscillations could occur.
8. The leakage inductance of pulse transformers would induce propagation delay depending on the drive current through it. The higher the energy through the pulse transformer is, the longer the delay would be.
9. To save board space, the silk screen text can be deleted, as some brick manufacturers do today.
10. In the initial design, use a SOD123 diode (such as MBR0530T1) in series with VDD and VDDP pins to protect the ISL6551 from being damaged by reverse biasing, especially for the design with the MLF package, which cannot to be replaced easily. At the end of the design, the diode can be substituted with a zero Ohm 805 resistor.
11. For a high current density and multi-layer design, buried vias can be used to save space, but cost is added.
12. The current share support is for paralleling operation but not for redundancy. When it is used in redundant systems, it requires OR'ing circuit inserting between the converter and the common output bus.

Debugging TIPS

This section discusses some easy ways to bring up the power train in the least amount of time.

Before/After Build

1. Before building the board, it is wise to check if all magnetics components such as current transformer, main transformer, output inductors, input inductor, and commutating inductor are designed properly using magnetics design tools or waveforms across the magnetics method. In addition, all components, especially the power train components, should be checked if their power/thermal derating guidelines are met.
2. After the build, check if pin 1 of all ICs is placed properly.

Apply Biases with Current and Voltage Limiting

Before applying the input voltage to the converter, a quick check of all control circuits is always the first step.

1. Use Table 1 on page 15 of the ISL6551 datasheet design checklist.
2. Disable anything that prevents both ISL6551 and ISL6550 from free running. In the reference design, disconnecting the resistor (R6) between the START pin of the ISL6550 and the ON/OFF pin of ISL6551 will allow both chips to be free running.
3. In series forward diodes with the bias lines so that all ICs will not be damaged by reverse biasing. The reference design has built-in diodes.
4. Apply biases with current limiting.
5. Check if both DC and AC voltage levels of each ISL6550 pinout are correct. No noises and no over stressed.
6. Check if both DC and AC voltage levels of each ISL6551 pinout are correct. No noises and no over stressed.
7. Check if a nice sawtooth is in CT pin and equal pulse width is between upper drive signals.
8. Check if both DC and AC voltage levels of drive signals of bridge FETs and synchronous FETs are correct. No noises and no over stressed.
9. Check if the delays such as Dead Time, Resonant Delay, and LEB Delay are designed properly.
10. Check if the timing of the synchronous signals is designed properly. No shoot through.

Power Up Slowly with Current and Voltage Limiting

1. If possible, disconnect the secondary winding from the secondary side, then increase the input voltage slowly. Fix the primary timing until no (very low) current is drawn from the input line. And check if the magnetizing current is in a proper level.
2. Connect the secondary winding back to the circuit and disable the synchronous drivers such that the current conducts only through the body diodes of the synchronous FETs.
3. Increase the input voltage slowly with input and output current limiting and monitor the current through the main transformer or the current ramp signal that is fed into the ISL6551. No asymmetric behaviors should be seen and ten percent of load is a good start point.
4. If the converter is not stable, use a low ESR ceramic capacitor (say 0.1uF) at the feedback network to cut down the cut-off frequency until the converter becomes stable. Or use the simplified model in Figure 18 to design a low cut-off frequency system loop. Later, optimize the loop with a tool.
5. Enable the synchronous drivers. If the timing is not set properly, shoot-through currents between the secondary winding and the synchronous FETs would be induced and affect the converter's performance, especially in light load conditions. Start with some load (10% rated load) and work backward.
6. Check the current ramp signal at the ISENSE pin of ISL6551 and see if a longer blanking time is required.
7. Tune up. Design a proper resonant delay by programming the R_RESDLY resistor and changing (if possible) the ZVS elements such as, the magnetizing inductance, the leakage inductance, any external commutating inductor, the output capacitance of bridge FETs, and any external primary capacitance. Note that any loop that is used to measure the primary current can induce additional commutating inductance, depending upon the enclosed air area, and extends the ZVS load range. For instance, 5.0" of 14AWG wire can contribute as much as 80nH inductance.

Experimental Results

The evaluation board is intended to test the ISL6551 in a 200W half brick form factor. The specification of this converter is summarized at the end of this paper. Most of the converter circuitries are placed in the central 2.50"x2.45" area and limited within 0.5" height, and all unnecessary components such as test point connectors and Input/Output connectors are placed beyond the center.This DC/DC converter accepts a wide range input, 36V to 75V, and generates a wide range output, 2.64V to 3.63V with 31.918mV step and 60A full load. An ultra high efficiency, 88% efficiency at 3.3V fully loaded output, has been achieved. In the following sections, some critical aspects of the converter are examined with detailed experimental data.

Drive Signal Timing

The drive signals are taken when the ISL6551 is free running, which can be done by removing the input line and R6 that connects to the START pin of the ISL6550. The resonant delay to turn on the lower switch after the corresponding upper switch is turned off, as shown in Figure 20, helps achieve zero-voltage switching (ZVS). The dead time to turn on the upper FET after the corresponding lower switch is turned off, as shown in Figure 21, helps eliminate the shoot-through currents through the primary switches during switching transitions. Figures 22 and 23 show the resonant delay and the dead time set at the ISL6551 prior to be processed through pulse transformers (T3 andT5) and bridge drivers (Intersil HIP2100).

The dead time and the resonant delay, with 2V as the turn-on threshold of primary switches, of one converter is summarized in Table 3. The real delays at the primary switches are shorter than the “delays” set at the ISL6551 due to long propagation delays of falling edges of both upper and lower drive signals. Furthermore, the leakage inductances of pulse transformers also would induce additional propagation delays depending on the drive current through it. The higher the energy through the pulse transformer is, the longer the delay would be.

TABLE 4. RESONANT DELAY AND DEAD TIME

DELAY	AT SWITCH’S GATE	AT ISL6551
Resonant Delay	32 ns	36 ns
Dead Time	157 ns	186 ns

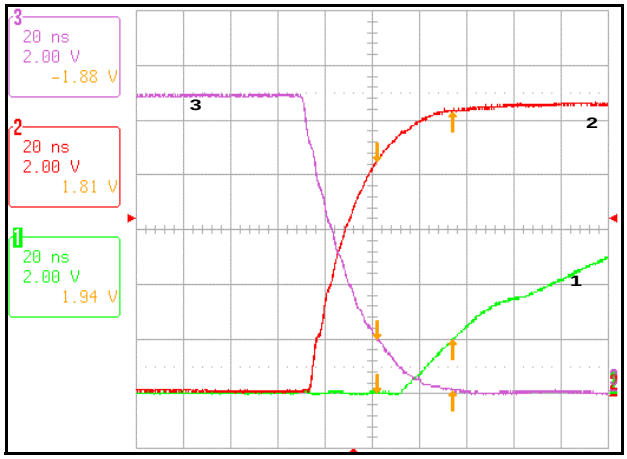


FIGURE 20. RESONANT DELAY AT LOWER FET. CHANNEL 1: LOWER DRIVE SIGNAL; CHANNEL 2 & 3: UPPER DRIVE SIGNALS

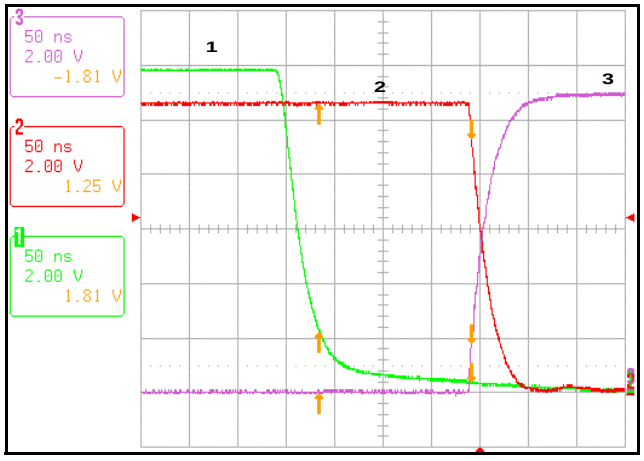


FIGURE 21. DEAD TIME AT LOWER FET. CHANNEL 1: LOWER DRIVE SIGNAL; CHANNEL 2 & 3: UPPER DRIVE SIGNALS

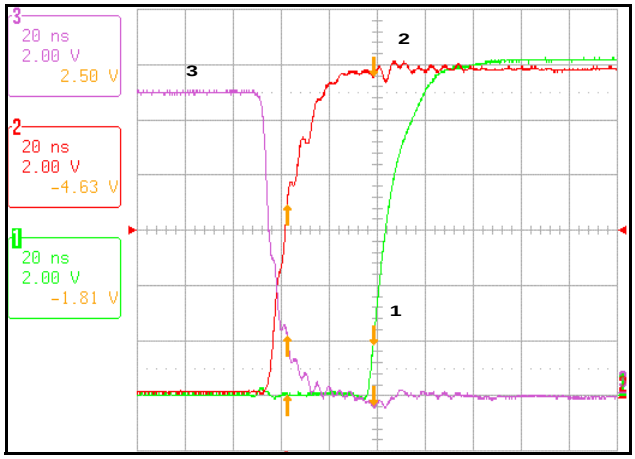


FIGURE 22. RESONANT DELAY AT ISL6551. CHANNEL 1: LOWER DRIVE SIGNAL; CHANNEL 2 & 3: UPPER DRIVE SIGNALS

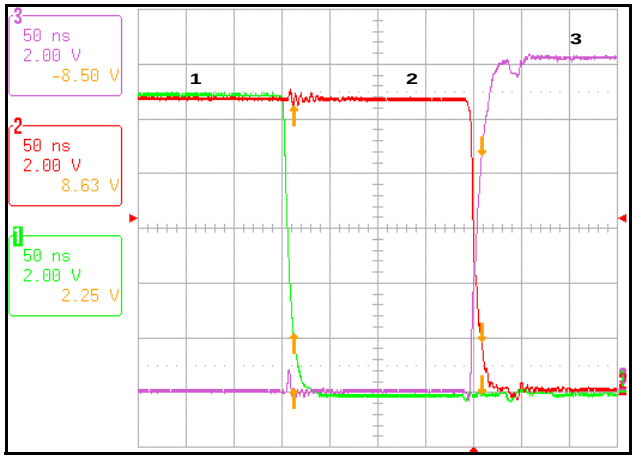


FIGURE 23. DEAD TIME AT ISL6551. CHANNEL 1: LOWER DRIVE SIGNAL; CHANNEL 2 & 3: UPPER DRIVE SIGNALS

The synchronous drive signals are the inverting version of both lower drive signals with little propagation delays. The turn-on gate resistors, R23 and R33, soften the rising edge of the lower drive signals, while the diodes, D5 and D19, reduce their falling edge delay. Meanwhile, the diodes, D1 and D4, minimize the turn-off delay of the synchronous drive signals, while the resistors, R3 and R18, increase their turn-on delay. As shown in Figure 24, the synchronous FET is turned off/on (Channel 2) whenever its corresponding lower switch is turned on/off (Channel 3). There is no overlap between these two drive signals. Hence, shoot-through currents between the secondary winding and the synchronous FETs are eliminated.

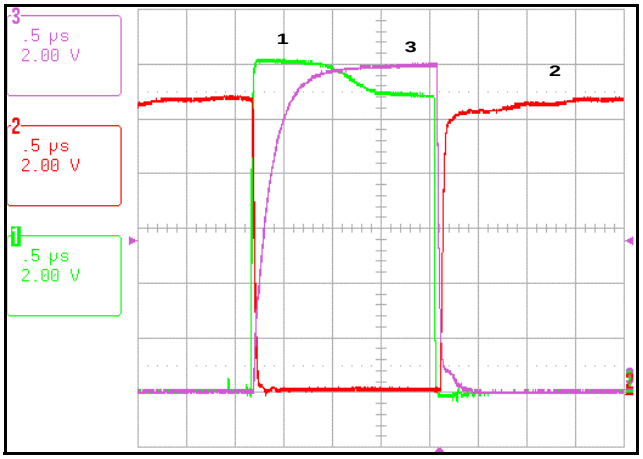


FIGURE 24. SYNCHRONOUS DRIVE SIGNAL. CHANNEL 1: LOWER DRIVE SIGNAL AT ISL6551; CHANNEL 2: SYNCHRONOUS DRIVE SIGNAL; CHANNEL 3: LOWER DRIVE SIGNAL AT THE LOWER FET

Switching Waveforms

WINDING VOLTAGE AND CURRENT

Figures 24 to 29 show the voltage waveforms across the transformer and the primary currents through it. Note that the R22 is replaced with a 5.0” of 14AWG wire so that the primary current can be measured at this loop, which should be shorted when determining the ZVS load range.

The delay between the primary voltage and secondary voltage on the leading edge, as shown in Figures 25 and 26, is caused by the leakage inductance of the transformer. The input voltage is applied first across the leakage inductor resetting its current, and the voltage across the real primary and secondary must stay zero until the current through the leakage inductor changes in direction and reaches the value of the reflected load. A higher load results in larger stored energy in the leakage inductor that needs to be reset before going into the active mode, and the longer the delay is. There is almost no delay for zero load operation, as shown in Figure 27.

As shown in Figure 27, with the synchronous FETs turned on, the converter still runs at continuous mode (CCM) with a large duty cycle even at no-load operation. Figure 28 shows the operation waveforms with synchronous FETs off. In this case, the synchronous FETs block any negative current, which forces the converter to run at discontinuous mode (DCM) cutting down the duty cycle significantly.

Figure 29 shows the operation waveforms for INV_SYNC DRIVE scheme. Since only one synchronous FET is turned on and conducts currents during the freewheeling period, the freewheeling current reflected to the primary is higher than that of the INV_LOW DRIVE scheme. Hence, the INV_LOW DRIVE scheme produces as much as 2% higher efficiency than the INV-SYNC DRIVE scheme.

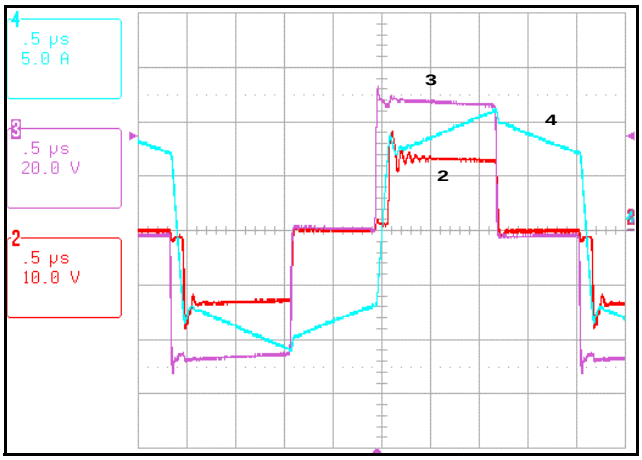


FIGURE 25. TRANSFORMER WAVEFORMS AT V_{IN}=48V, V_{OUT}=3.3V, AND I_{OUT}=60A. CHANNEL 4: PRIMARY CURRENT (I_P); CHANNEL 3: PRIMARY VOLTAGE (VP); CHANNEL 2: SECONDARY VOLTAGE (VS)

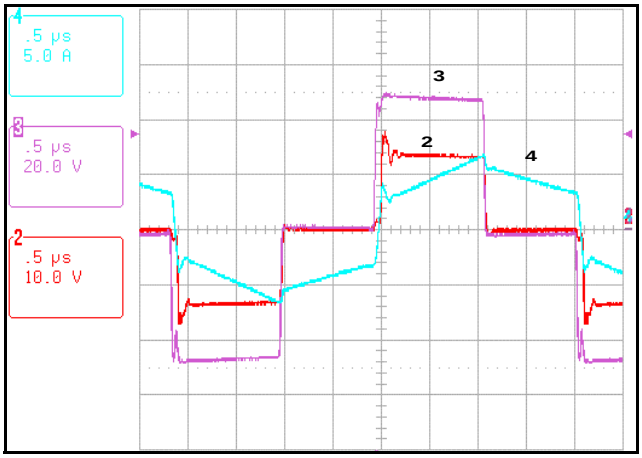


FIGURE 26. TRANSFORMER WAVEFORMS AT V_{IN}=48V, V_{OUT}=3.3V, AND I_{OUT}=30A. CHANNEL 4: PRIMARY CURRENT (I_P); CHANNEL 3: PRIMARY VOLTAGE (VP); CHANNEL 2: SECONDARY VOLTAGE (VS)

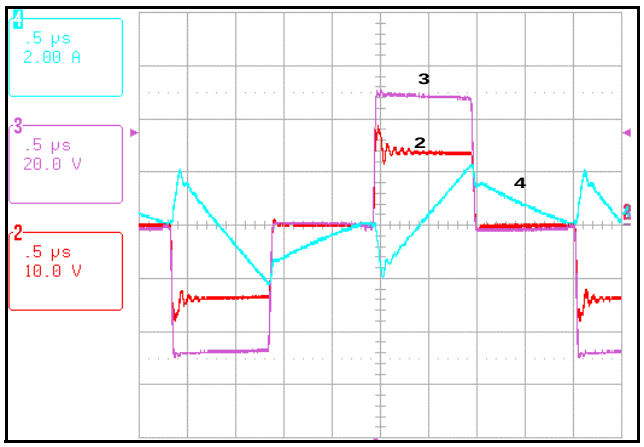


FIGURE 27. TRANSFORMER WAVEFORMS AT V_{IN}=48V, V_{OUT}=3.3V, AND I_{OUT}=0A (SYN ON). CHANNEL 4: PRIMARY CURRENT (I_P); CHANNEL 3: PRIMARY VOLTAGE (VP); CHANNEL 2: SECONDARY VOLTAGE (VS)

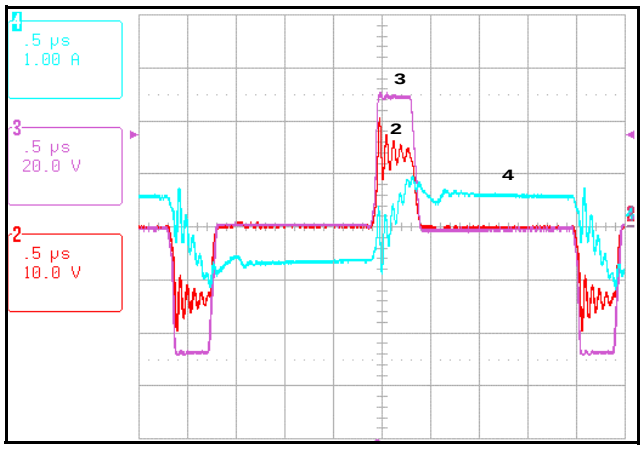


FIGURE 28. TRANSFORMER WAVEFORMS AT V_{IN}=48V, V_{OUT}=3.3V, AND I_{OUT}=0.5A (SYN OFF). CHANNEL 4: PRIMARY CURRENT (I_P); CHANNEL 3: PRIMARY VOLTAGE (VP); CHANNEL 2: SECONDARY VOLTAGE (VS)

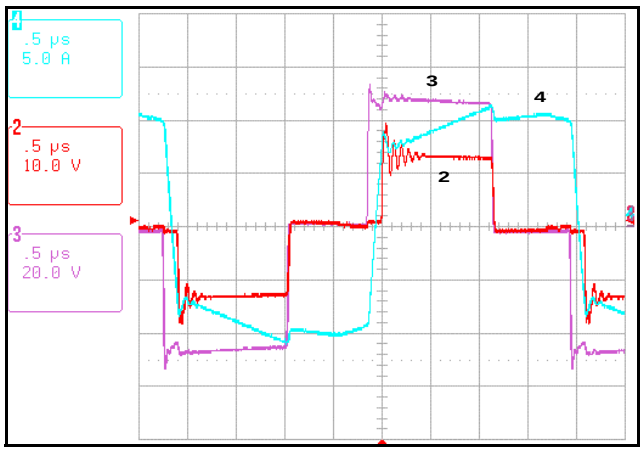


FIGURE 29. TRANSFORMER WAVEFORMS AT V_{IN}=48V, V_{OUT}=3.3V, AND I_{OUT}=60A (INV_SYNC DRIVE SCHEME). CHANNEL 4: PRIMARY CURRENT (I_P); CHANNEL 3: PRIMARY VOLTAGE (VP); CHANNEL 2: SECONDARY VOLTAGE (VS)

ZVS TRANSITIONS

Figures 30 to 34 show resonant transitions for the lower FET in various situations, and they are taken by shortening the loop that is used to measure the primary current. Table 5 summarizes the ZVS conditions of one converter for various input and output voltages (which do not apply to every converter since the ZVS conditions of each converter are heavily dependant upon the leakage inductance and the output capacitance of the primary switches). In the nominal 48V input and 3.3V output condition, the converter loses ZVS transitions below 62% of full load, as shown in Figure 31. At the low line (36V) situation, ZVS transitions extend to 42% of full load, as shown in Figure 33, since the energy stored in the parasitic capacitance is proportional to V_{IN}^2 and reaches its minimum. On the other hand, the high line (75V) completely loses ZVS transitions even at 100% load since the energy stored in the parasitic capacitance reaches its maximum and the energy in the commutating inductance is not enough to resonate the tank to the valley, as shown in Figure 34.

TABLE 5. ZVS LOAD RANGE

V_{IN}\V_{OUT}	2.64V	3.30V	3.63V
36V	<50%	<42%	<33%
48V	<75%	<62%	<58%
75V	>100%	>100%	<92%

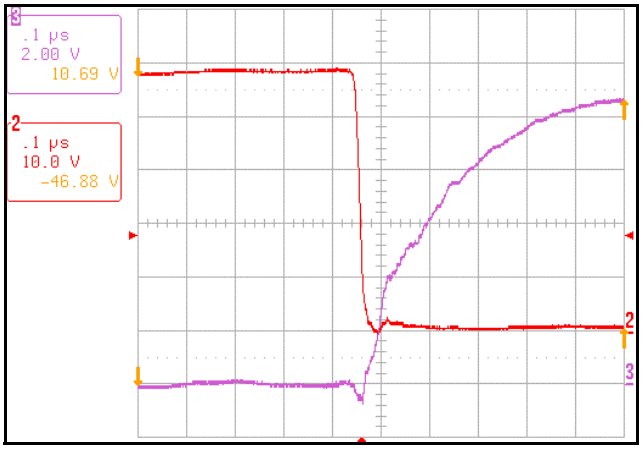


FIGURE 30. RESONANT TRANSITION AT V_{IN}=48V, V_{OUT}=3.3V, AND I_{OUT}=60A. CHANNEL 2: V_{DS} VOLTAGE OF LOWER FET; CHANNEL 3: LOWER GATE DRIVE SIGNAL

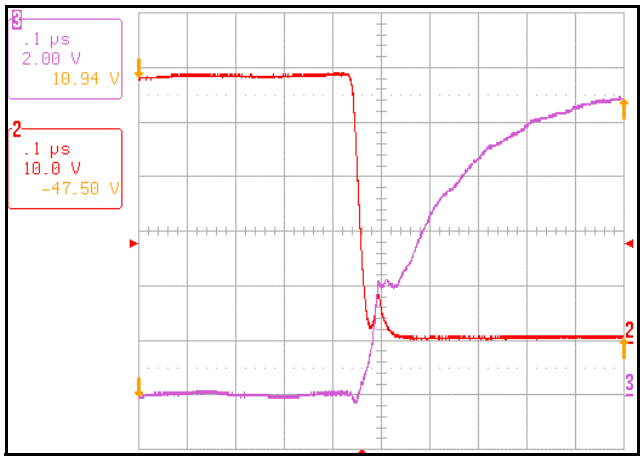


FIGURE 31. RESONANT TRANSITION AT V_{IN}=48V, V_{OUT}=3.3V, AND I_{OUT}=37A. CHANNEL 2: V_{DS} VOLTAGE OF LOWER FET; CHANNEL 3: LOWER GATE DRIVE SIGNAL

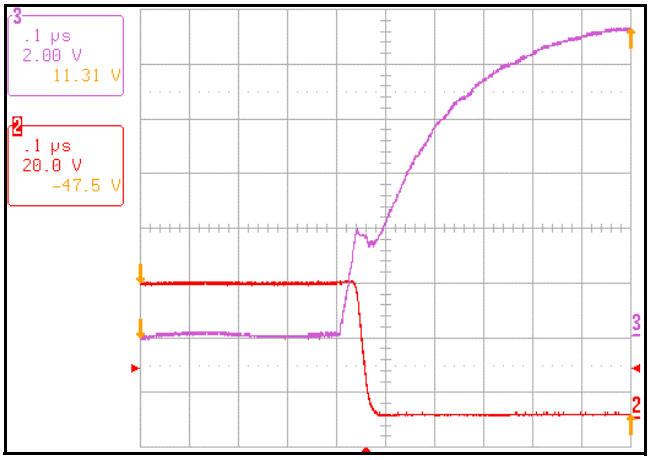


FIGURE 32. RESONANT TRANSITION (LOST) AT V_{IN}=48V, V_{OUT}=3.3V, AND I_{OUT}=0A. CHANNEL 2: V_{DS} VOLTAGE OF LOWER FET; CHANNEL 3: LOWER GATE DRIVE SIGNAL

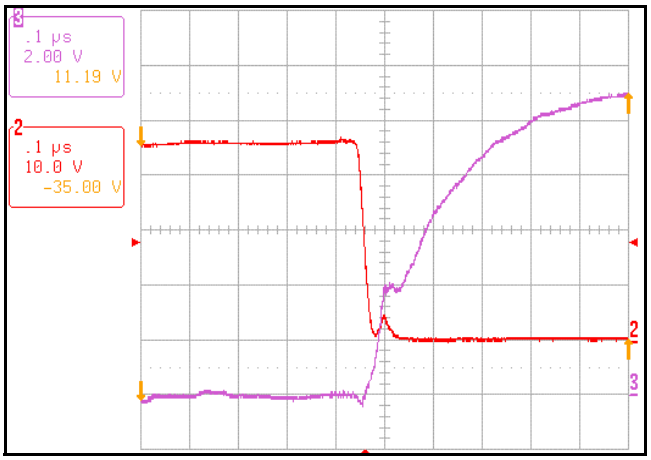


FIGURE 33. RESONANT TRANSITION AT V_{IN}=36V, V_{OUT}=3.3V, AND I_{OUT}=25A. CHANNEL 2: V_{DS} VOLTAGE OF LOWER FET; CHANNEL 3: LOWER GATE DRIVE SIGNAL

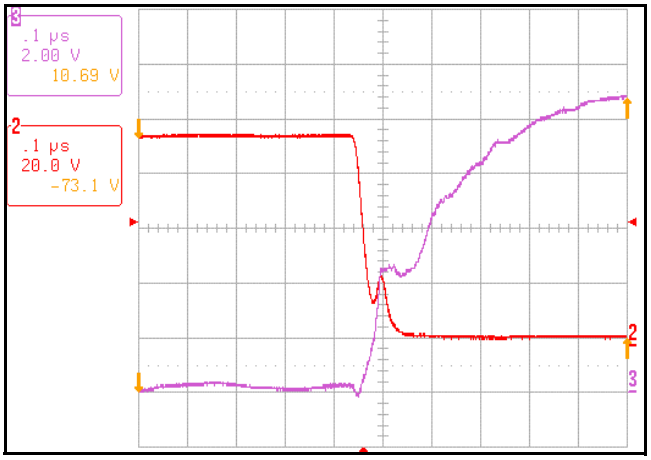


FIGURE 34. RESONANT TRANSITION (LOST) AT V_{IN}=75V, V_{OUT}=3.3V, AND I_{OUT}=60A. CHANNEL 2: V_{DS} VOLTAGE OF LOWER FET; CHANNEL 3: LOWER GATE DRIVE SIGNAL

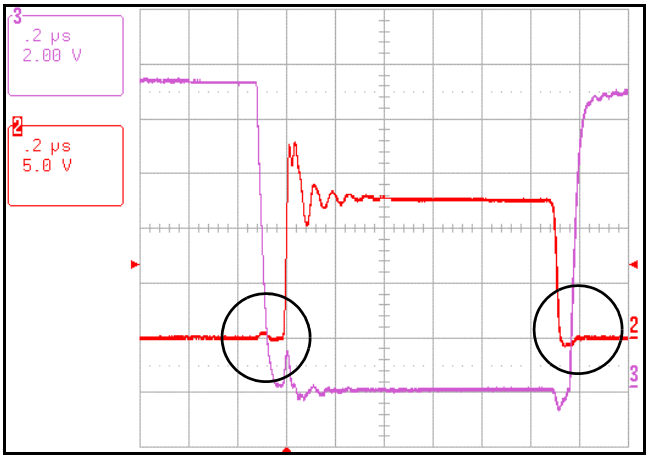


FIGURE 35. V_{IN}=48V, V_{OUT}=3.3V, AND I_{OUT}=60A. CHANNEL 2: V_{DS} VOLTAGE OF SYN FET; CHANNEL 3: SYNCHRONOUS GATE DRIVE SIGNAL

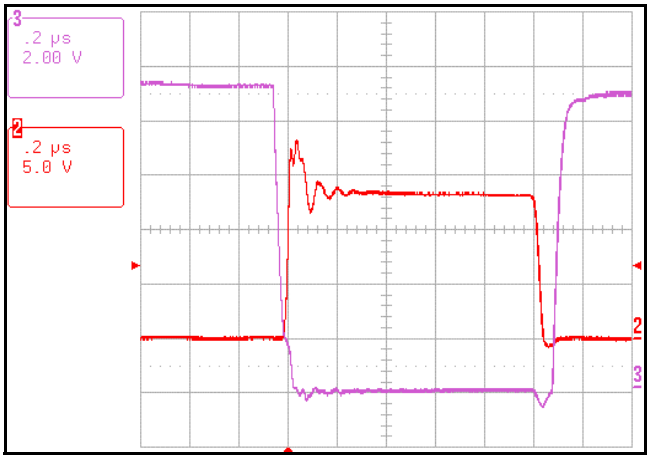


FIGURE 36. V_{IN}=48V, V_{OUT}=3.3V, AND I_{OUT}=0A. CHANNEL 2: V_{DS} VOLTAGE OF SYN FET; CHANNEL 3: SYNCHRONOUS GATE DRIVE SIGNAL

As shown in Figures 35 and 36, the synchronous FETs are zero-voltage switching at turn on, and have negligible switching losses at turn off during the light load. Nevertheless, the two bumps, as shown in Figure 35, are caused by the body diode conduction and/or its reverse recovery at turn on or off, which do induce losses.

Shutdown Timing (Shorted Circuit, UV, OV)

OUTPUT SHORTED CIRCUIT

When the output is shorted, the START (channel 2) is latched after the UVDLY (channel 3) capacitor (C26) is charged above the threshold 5V, as shown in Figure 37. Note that additional delay is induced by the probe at the ISL6550 UVDLY pin. If the short is removed and the output voltage returns to the normal level before the under-voltage delay, around 70ms, is time out, then the START would not be latched.

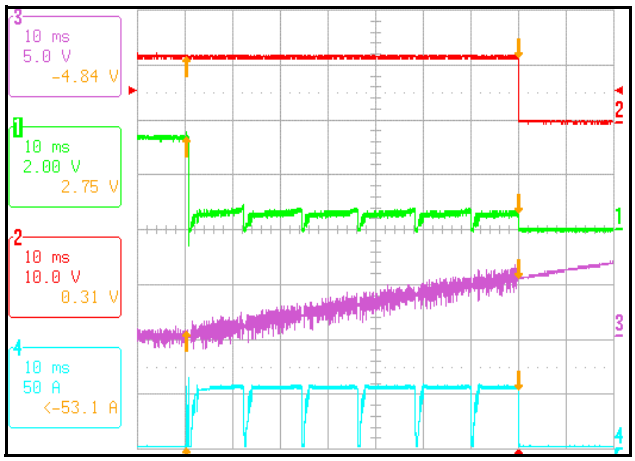


FIGURE 37. OUTPUT SHORTED CIRCUIT. CHANNEL 1: OUTPUT VOLTAGE; CHANNEL 2: START SIGNAL; CHANNEL 3: UVDLY AT ISL6550; CHANNEL 4: OUTPUT CURRENT

OUTPUT UNDER-VOLTAGE DELAY

As shown in Figure 38, the output voltage (Channel 3) has a huge dip, but it returns to normal level before the under-voltage delay is time out, hence, the START (channel 2) is not pulled low. Figure 39 shows that the UVDLY starts to rise when the output voltage is below the under-voltage threshold, and the START is latched when the UVDLY reaches 5V threshold.

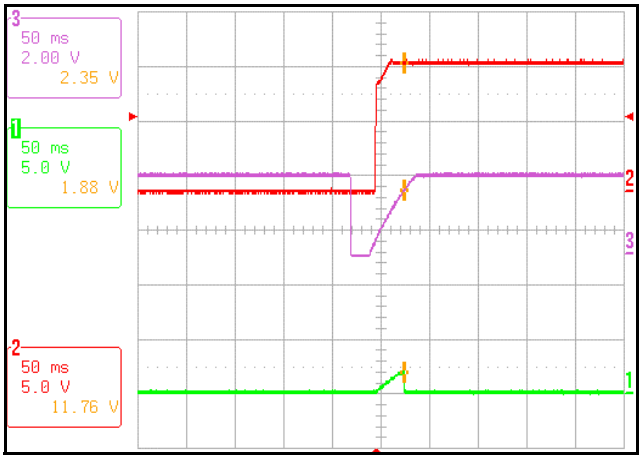


FIGURE 38. OUTPUT UNDER-VOLTAGE DELAY. CHANNEL 1: UVDLY; CHANNEL 2: START SIGNAL; CHANNEL 3: OUTPUT VOLTAGE

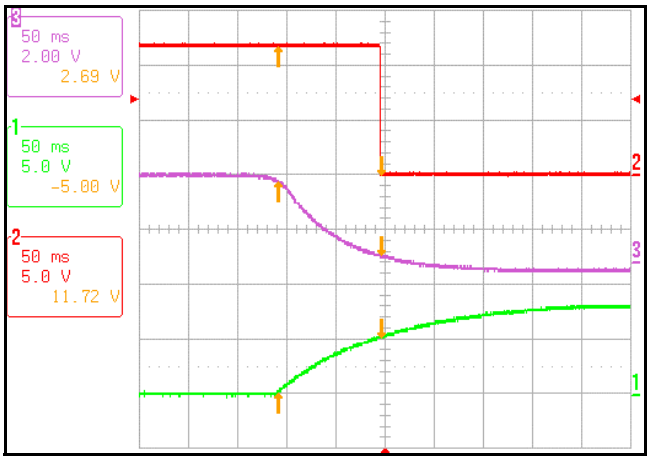


FIGURE 39. OUTPUT UNDER-VOLTAGE DELAY. CHANNEL 1: UVDLY; CHANNEL 2: START SIGNAL; CHANNEL 3: OUTPUT VOLTAGE

OUTPUT OVER-VOLTAGE

When the EAI pin is pulled to ground, the error voltage jumps up and causes an over voltage at the output (channel 1), and the START (Channel 3) is latched, as shown in Figure 40. The LATSD (Channel 2) is not triggered since the output voltage does not exceed the master over-voltage setpoint.

With a quick touch to the output (at zero load) with a 5V voltage source, both local and master over-voltage setpoints are violated. Figure 41 shows that the START is triggered at a lower voltage level than the LATSD. The START is nominally latched at around 108.33% of the output voltage, while the LATSD is latched at a higher fixed voltage, around 4.19V and above the maximum BDAC output voltage. The master over-voltage monitoring circuit is designed with the bandgap reference of the ISL6551, rather than the ISL6550 internal reference that is used for the local over-voltage setpoint, about 108.33% of the BDAC voltage. Thus, the converter can gain additional protection against the failure of the ISL6550 internal reference or mis-configuration of the

ISL6550. For instance, when R40 or R42 is somehow shorted by debris or solder, the output voltage would be programmed up to 5V (the reference of ISL6550) and the local over-voltage setpoint is also moved up relative to the output voltage level. In a such situation, the master over-voltage circuit will over-ride the local over-voltage setpoint whenever it is greater than 4.19V and protect the processor or the load from being over-stressed.

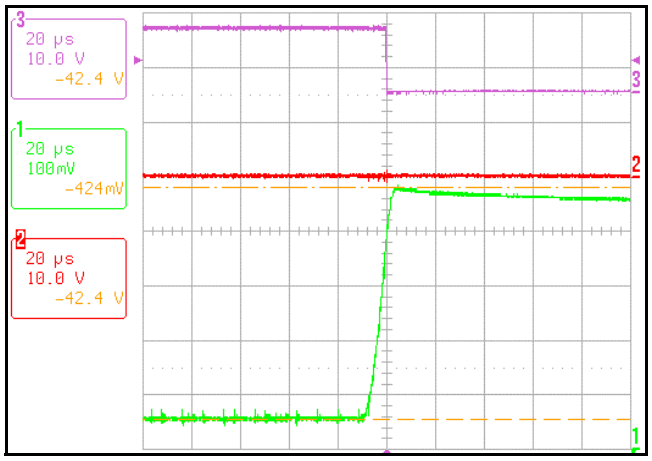


FIGURE 40. OVER VOLTAGE (V_{OUT}=3.6V). CHANNEL 1: OUTPUT VOLTAGE; CHANNEL 2: LATSD SIGNAL; CHANNEL 3: START SIGNAL

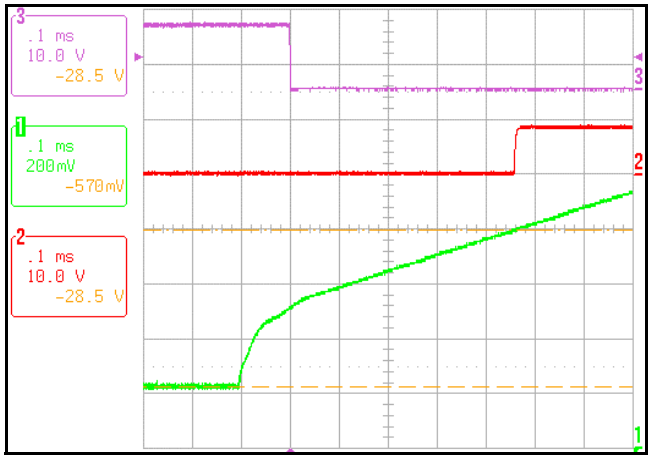


FIGURE 41. OVER VOLTAGE (V_{OUT}=3.63V). CHANNEL 1: OUTPUT VOLTAGE; CHANNEL 2: LATSD SIGNAL; CHANNEL 3: START SIGNAL

Efficiency Curves

Figures 42 to 44 show the efficiency curves for different output voltages, and the data are taken at around 400 LFM airflow with a PAPST-MOTOREN TYP 4600 fan. Each figure illustrates that the lower the input line is, the higher the efficiencies at which the converter operates. This is mainly because the higher the input line is, the lower the duty cycle is, and the higher the conduction and switching losses of the primary switches are. Note that the input and output voltages are measured at TP9 & TP10 and TP4 & TP5, respectively.

Figure 45 shows the full-load efficiencies of the converter for various input lines. Each curve shows that the higher the output voltage is, the higher the efficiency is for the same reasons, as mentioned above.

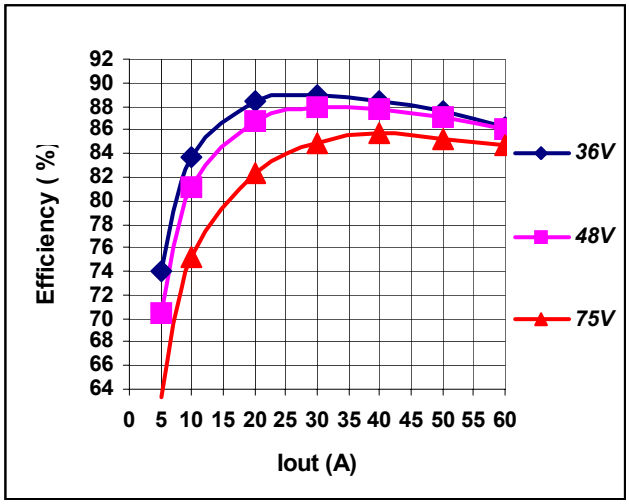


FIGURE 42. EFFICIENCY CURVES FOR V_{OUT}=2.64V@~400 LFM

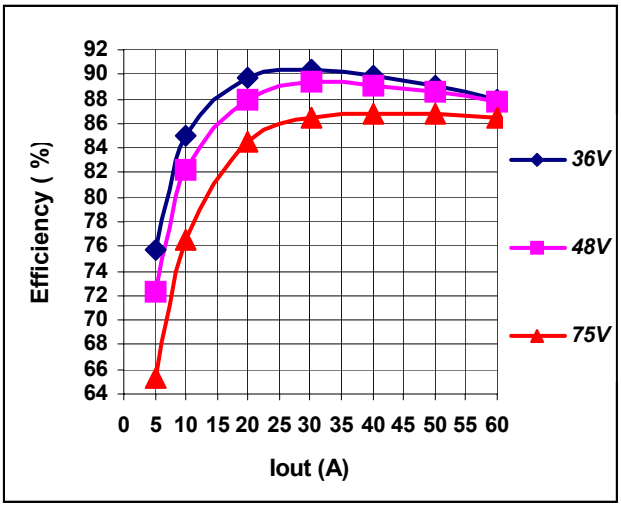


FIGURE 43. EFFICIENCY CURVES FOR V_{OUT}=3.3V @~400 LFM

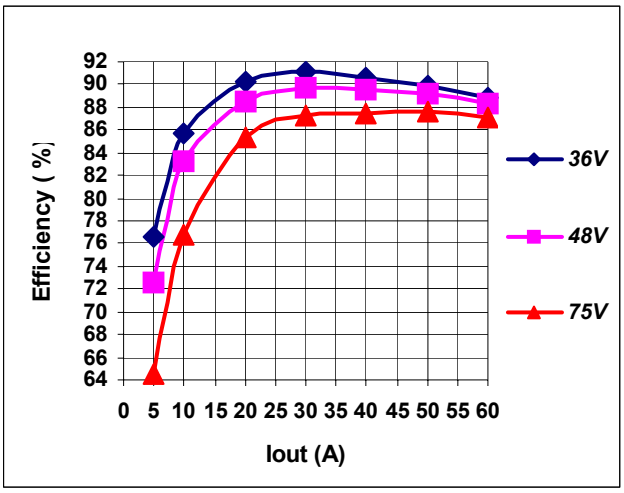


FIGURE 44. EFFICIENCY CURVES FOR V_{OUT}=3.64V @~400 LFM

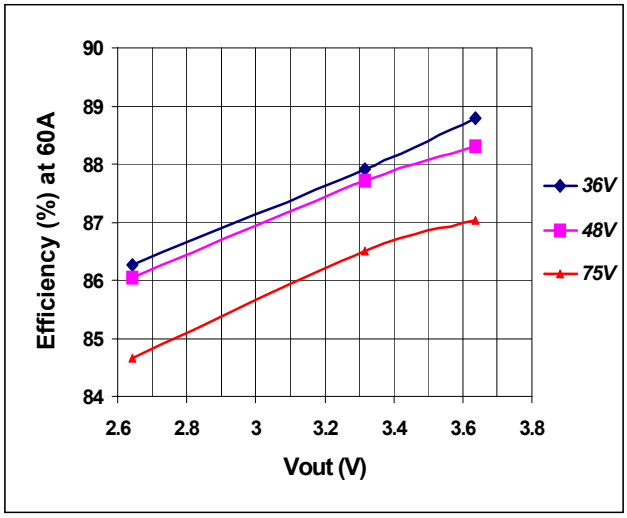


FIGURE 45. EFFICIENCY AT 60A FOR DIFFERENT V_{OUT} @~400 LFM

THERMAL DATA

The thermal data are taken with a Fluke 80T-IR Infrared Temperature Probe at 21^0C ambient temperature while a PAPST-MOTOREN TYP 4600 fan (estimated around 400 LFM or more) is placed vertically 2.0” away from the input end of the converter. The data are used only for a relative comparison purpose, therefore, users should not do any thermal derating based on these thermal curves because the data points are not necessarily presenting the absolute values at the operating condition.

The data points in Figures 46 to 52 are taken at V_{OUT}=3.3V. Figure 46 shows the upper FET (Q14) case temperature. The higher the input voltage is, the longer the freewheeling period is, therefore, the higher the conduction losses of the upper FET is. Thus, the case temperature is higher at the high line.

Figure 47 shows the case temperature of the lower FET (Q17). The higher the input voltage is, the higher the switching losses of the lower FET are. At the high line, the case temperature of the FET rises significantly since ZVS transitions are completely lost and the switching losses dominate the channel conduction losses.

Figure 48 shows the case temperature of the current sense transformer (T4). At low line, the case temperature is much higher since the current ramp through the current sense transformer has a larger duty cycle and produces a higher RMS value and higher resistive losses.

Figures 49 and Figure 50 show the case temperature of the main transformer (T2) and a synchronous FET (Q1), respectively.

Figure 51 shows the synchronous driver (M2) case temperature. The curves in this figure look flatter than those in other figures since the driver losses heavily depend on the gate charge of the synchronous FETs (which remains almost constant), rather than the output load.

Figure 52 shows the case temperature of an output inductor (L2). At the high line, the inductor gets hotter since the ripple current as well as its RMS value is higher.

The data points in Figures 53 to Figure 59 are taken at various output and full load operating conditions with around 400 LFM airflow. As shown in these figures, the worst operating point is at the high line and maximum output voltage for all cases except the current sense transformer (T4), which has its worst operating point at the low line and maximum output voltage.

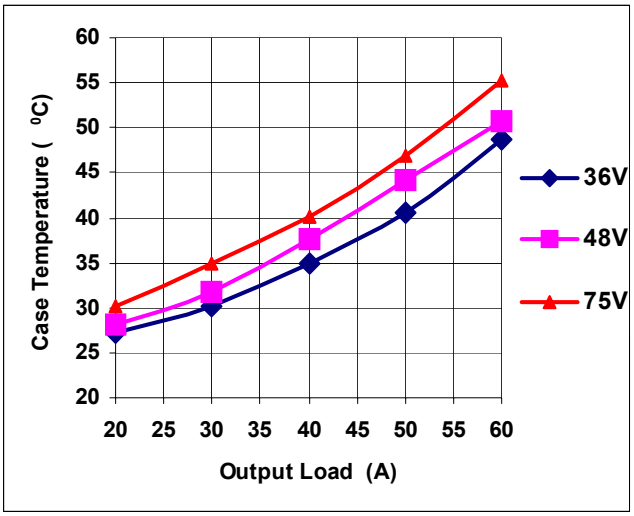


FIGURE 46. UPPER FET (Q14) CASE TEMPERATURE

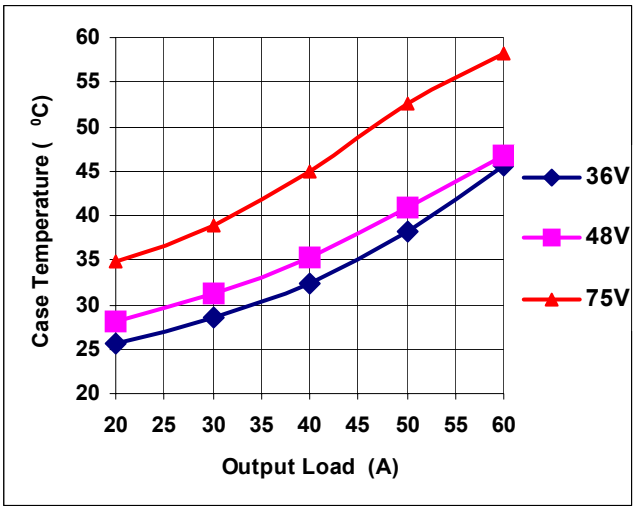


FIGURE 47. LOWER FET (Q17) CASE TEMPERATURE

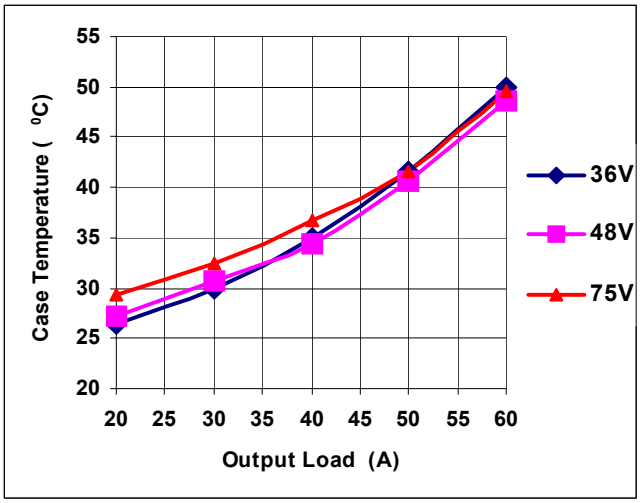


FIGURE 50. SYNCHRONOUS FET (Q1) CASE TEMPERATURE

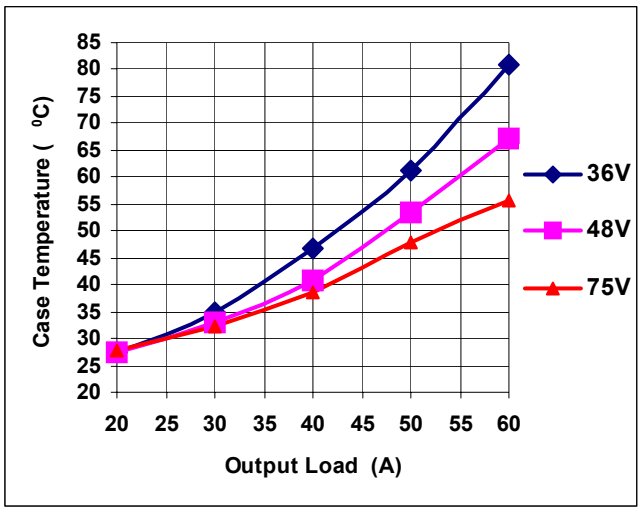


FIGURE 48. CURRENT TRANSFORMER (T4) CASE TEMPERATURE

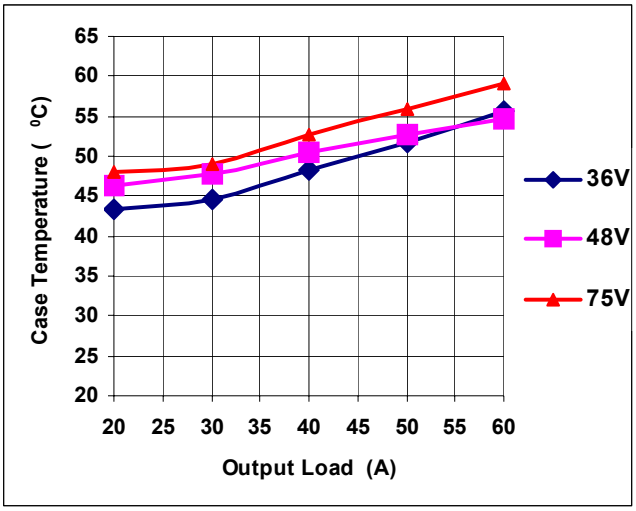


FIGURE 51. SYNCHRONOUS DRIVER (M2) CASE TEMPERATURE

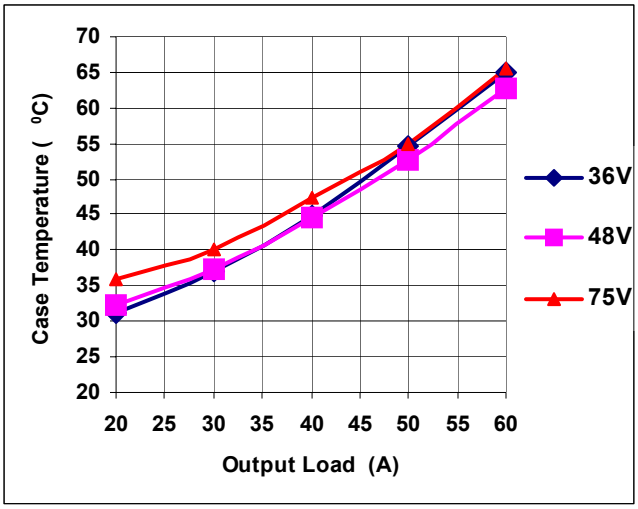


FIGURE 49. MAIN TRANSFORMER (T2) CASE TEMPERATURE

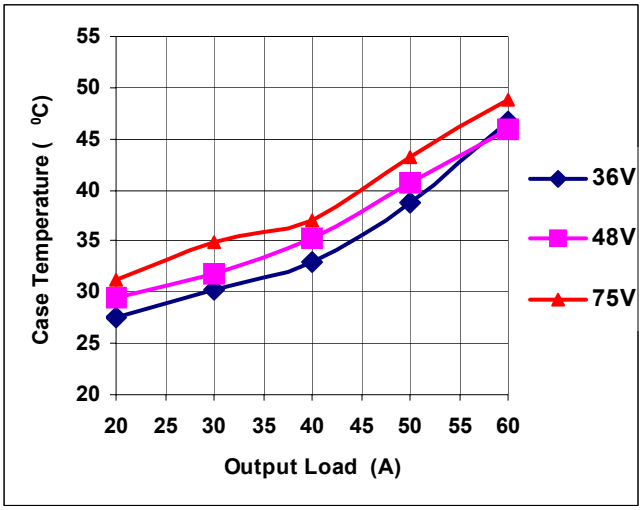


FIGURE 52. OUTPUT INDUCTOR (L2) CASE TEMPERATURE

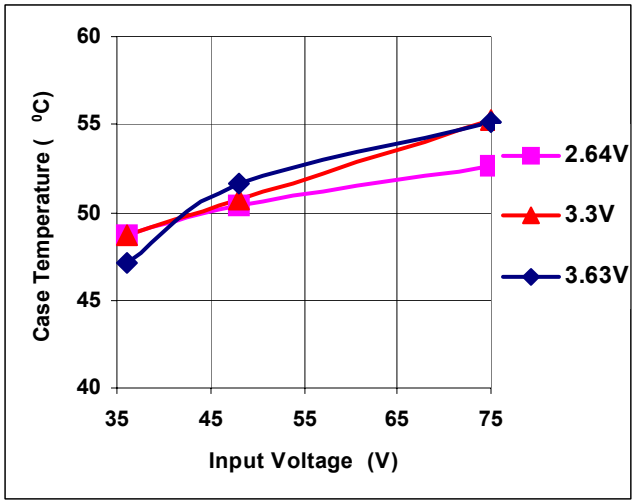


FIGURE 53. UPPER FET (Q14) CASE TEMPERATURE

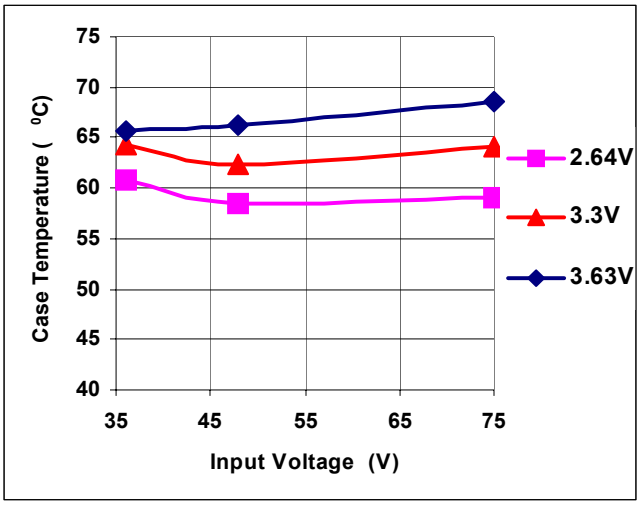


FIGURE 56. MAIN TRANSFORMER (T2) CASE TEMPERATURE

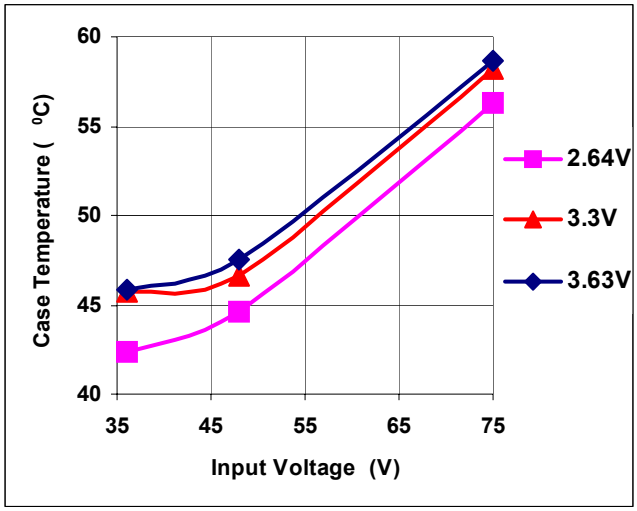


FIGURE 54. LOWER FET (Q17) CASE TEMPERATURE

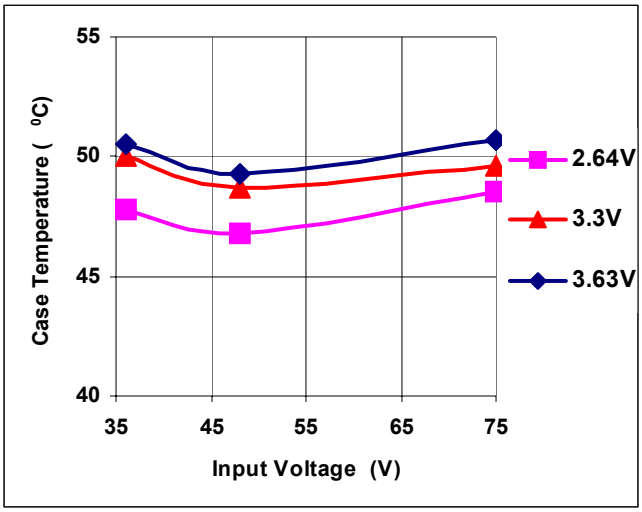


FIGURE 57. SYNCHRONOUS FET (Q1) CASE TEMPERATURE

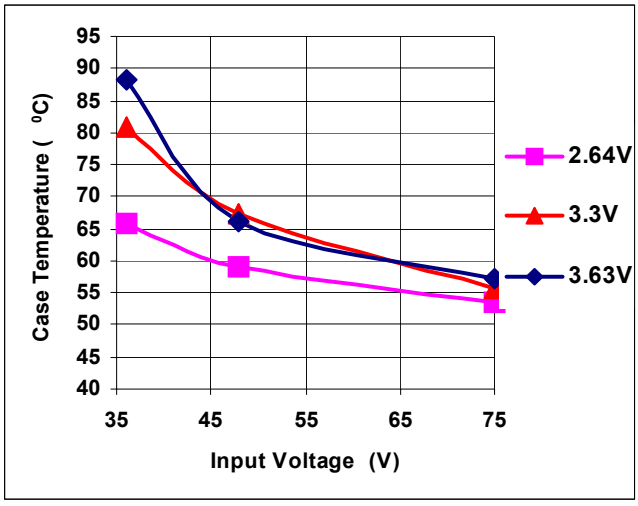


FIGURE 55. CURRENT TRANSFORMER (T4) CASE TEMPERATURE

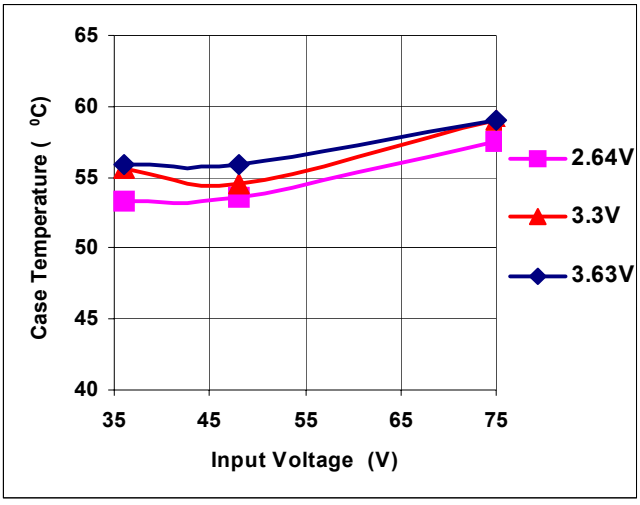


FIGURE 58. SYNCHRONOUS DRIVERS (M2) CASE TEMPERATURE

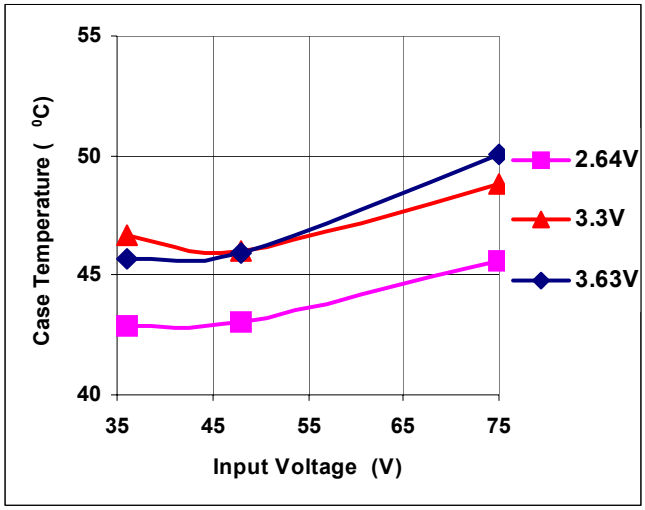


FIGURE 59. OUTPUT INDUCTOR (L2) CASE TEMPERATURE

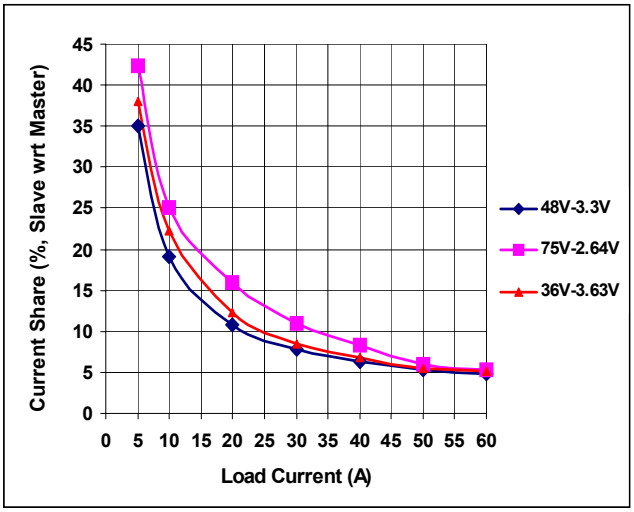


FIGURE 60. CURRENT SHARE CURVES

As shown in the figures above, the current transformer and the main transformer are the hottest components. Without any airflow, their case temperatures would rise significantly and exceed the device ratings at heavy load operations. Users should do a more thorough analysis at the worst case operating condition to evaluate thermal stress of each device. The current transformer is roughly measured to be above 130°C at room ambient temperature, 48V input and 3.3V, 50A output without any airflow due to its heavy glossy pinout, so it is recommended that users redesign the current sense transformer for a better form factor and thermal performance.

Current Share

Two equal length (3 inch) and size (10 AWG) wires split the load into each individual converter, thus, the impedance mismatching of current-carrying traces from the converters to the load is minimized. The current delivered by each converter is measured with only one current probe to reduce measurement error. With this kind of setup and measurement method, impedance difference and measurement error are still greater than that of building both converters in a board with a symmetric layout and measuring the current with precise current sense resistors. The measurement error increases with decreasing load.

Figure 60 shows current share curves at various input lines and output voltages. The current sharing is inversely proportional to the load, and the slave unit can share the load within 5% of the master unit at full load operation. Since the offset of the error amplifier and the difference of the output reference as well as the difference of power train components between both units remains constant, the difference of the load currents delivered by the master and the slave units almost remains constant, as shown in Figure 61. In addition, at no-load operation, the master unit will source current into the slave units because the higher voltage (master) back drives the lower voltage (slave).

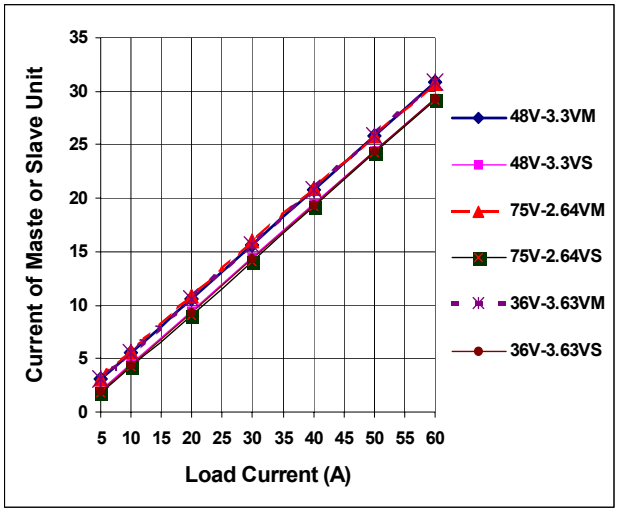


FIGURE 61. CURRENT OF MASTER AND SLAVE UNIT

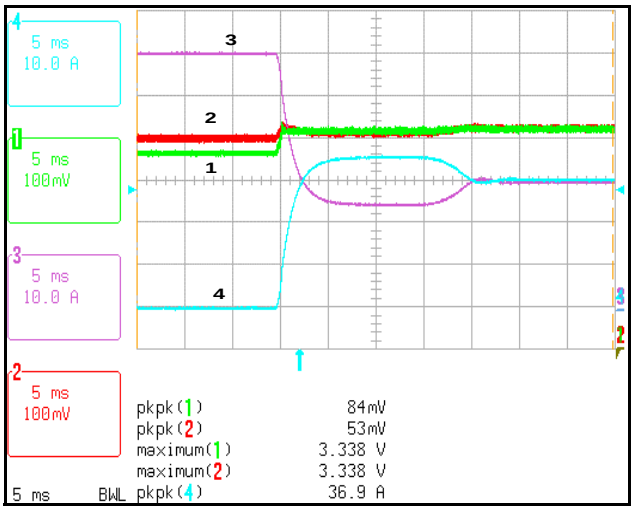


FIGURE 62. TURN ON SLAVE (CHANNEL 3 AND CHANNEL 2) FIRST. MASTER: CHANNEL 4 AND CHANNEL 1

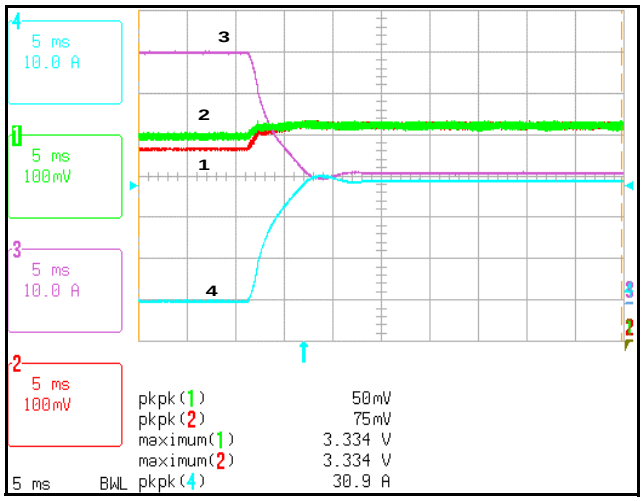


FIGURE 63. TURN ON MASTER (CHANNEL 3 AND CHANNEL 1) FIRST. SLAVE: CHANNEL 4 AND CHANNEL 2

Figures 62 and Figure 63 show the interaction between master and slave units in two different turn-on sequences. When the slave unit is turned on first, it acts as a “master” during the start up of the master unit. It takes a longer time for both converters to switch back to their proper roles settling down than that of the master unit is turned on first.

Step Responses

This section summarizes step responses of the converter at various input lines and output voltages (Figures 64 to 69). In all the figures of this section, Channel 4 represents the load step, and channel 1 represents the output voltage. For transients from 45A to 60A, channel 4 shows only 1/4 of the load. Table 6 summarizes the transient voltage spikes at different operating conditions. Note that the measurement is including the ripple voltage. The actual transient voltages excluding the ripple voltage should be smaller and not very different in all cases since the cut-off frequency and the corresponding phase of the loop for all cases are very close, as illustrated in the *Loop Response* section.

TABLE 6. TRANSIENT RESPONSE

INPUT	OUTPUT	LOAD STEP	TRANSIENT Vp-p	1/2 Vp-p
75V	2.64V	0-15A, 1A/us	353mV	177mV
75V	2.64V	45-60A, 1A/us	350mV	175mV
48V	3.30V	0-15A, 1A/us	328mV	164mV
48V	3.30V	45-60A, 1A/us	319mV	160mV
36V	3.63V	0-15A, 1A/us	316mV	158mV
36V	3.63V	45-60, 1A/us	306mV	153mV

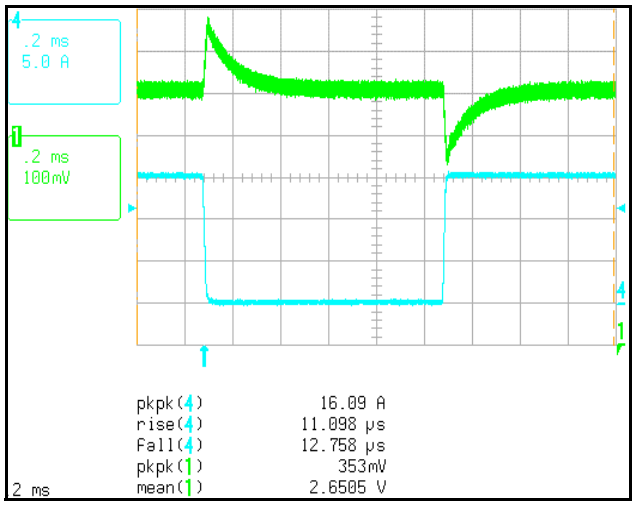


FIGURE 64. TRANSIENT RESPONSE FOR V_{IN}=75V AND V_{OUT} = 2.64V AT 0A-15A STEP, 1A/us

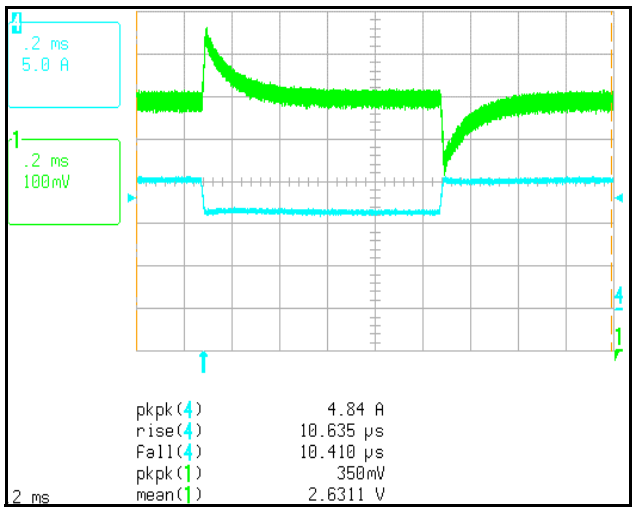


FIGURE 65. TRANSIENT RESPONSE FOR V_{IN}=75V AND V_{OUT} = 2.64V AT 45A-60A STEP, 1A/us

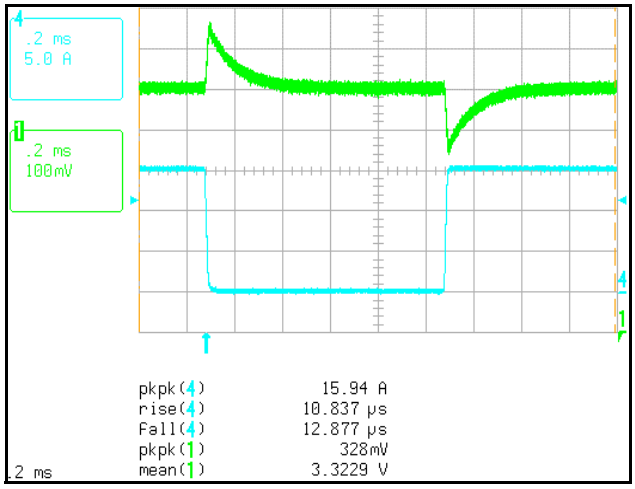


FIGURE 66. TRANSIENT RESPONSE FOR V_{IN}=48V AND V_{OUT} = 3.3V AT 0A-15A STEP, 1A/us

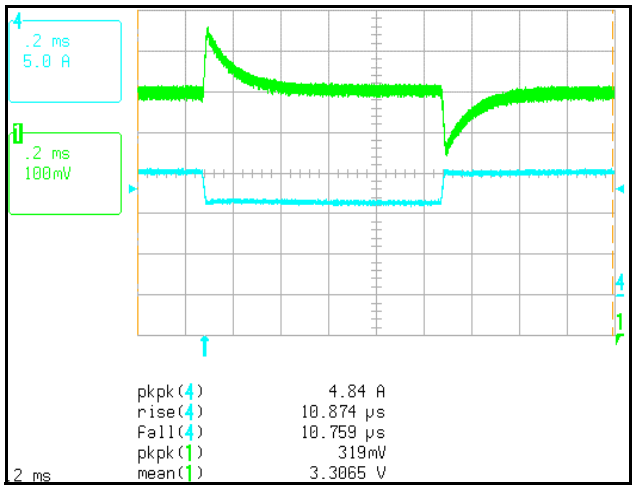


FIGURE 67. TRANSIENT RESPONSE FOR V_{IN}=48V and V_{OUT} = 3.3V AT 45A-60A STEP, 1A/us

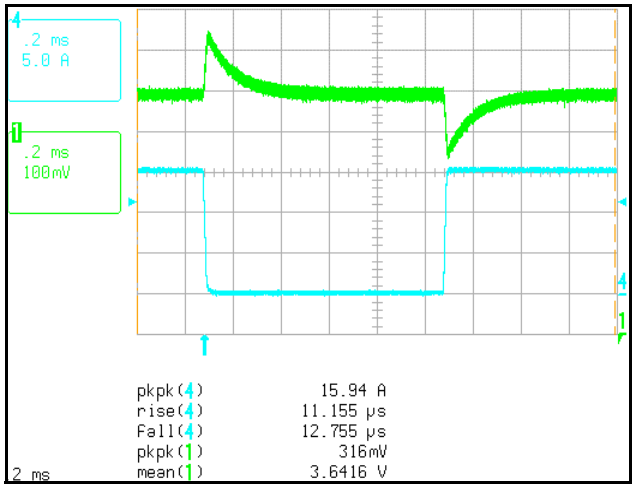


FIGURE 68. TRANSIENT RESPONSE FOR V_{IN}=36V AND V_{OUT} = 3.63V AT 0A-15A STEP, 1A/us

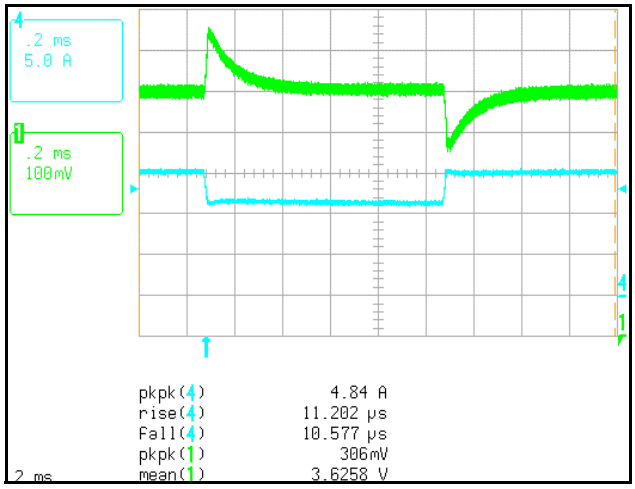


FIGURE 69. TRANSIENT RESPONSE FOR V_{IN}=36V AND V_{OUT} = 3.63V AT 45A-60A STEP, 1A/us

Loop Response

The experimental results presented in this section are measured with a 350 Venable system. The injection point is at R131 instead of R76 since R76 is located at noise sensitivity nodes.

Since it is a current mode control system, the transfer function of the plant is mainly determined by the characteristic of the load including the output resistive, capacitive, and inductive impedance, all of which varies with different applications.

We had only five 25W 0.1Ω “pure” resistive loads available for testing in our lab. A 38A load was constructed with these five resistors for 3.3V output. As shown in Figure 70, the load can be characterized as a 0.086Ω resistor in series with 260 nH inductance induced by the two 5.0” 10AWG wires that connect to the load. The open loop response slightly varies with the input voltage, as shown in Figure 71.

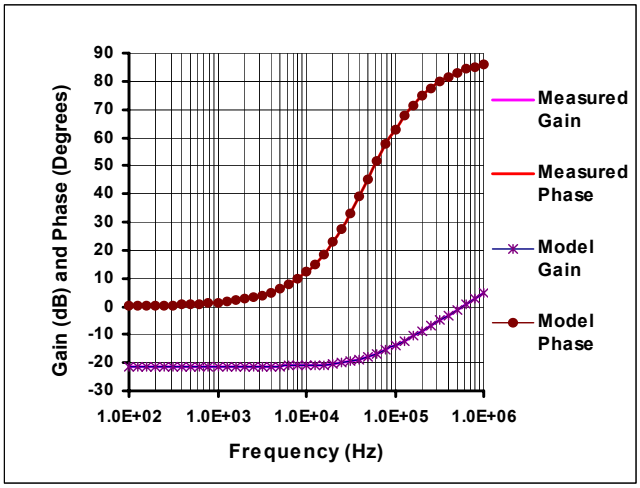


FIGURE 70. RESISTIVE LOAD CHARACTERISTIC

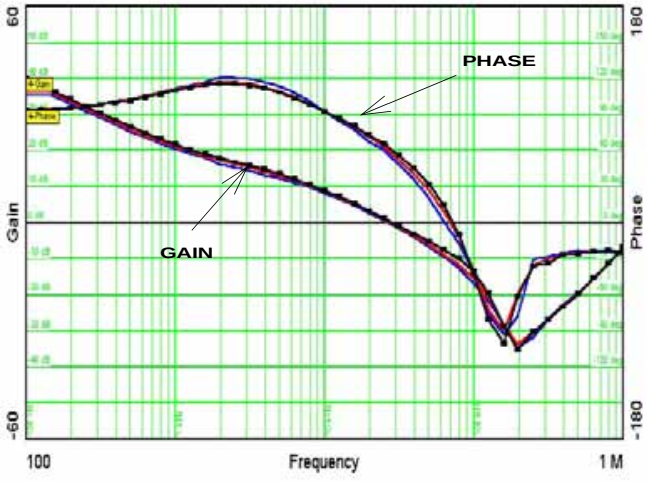


FIGURE 71. OPEN LOOP RESPONSE FOR 3.3V@38A RESISTIVE LOAD. RED-48V, BLUE-75V, AND BLACK-36V

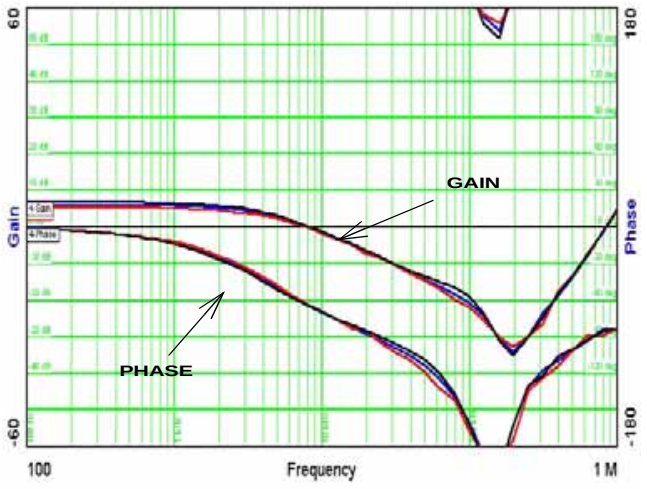


FIGURE 72. PLANT FREQUENCY RESPONSE FOR 3.3V@38A RESISTIVE LOAD. RED-48V, BLUE-75V, AND BLACK-36V

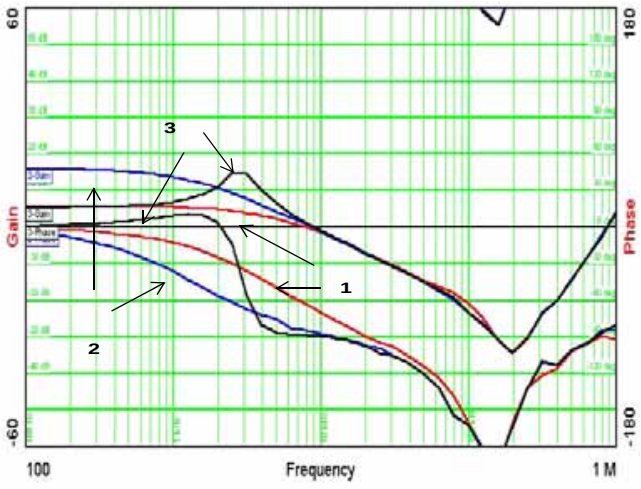


FIGURE 74. PLANT RESPONSE FOR THREE KINDS OF LOADS AT 48V, 3.3V@38A. RED(1)-"PURE" RESISTIVE LOAD, BLUE(2)-ELECTRONIC CONSTANT CURRENT LOAD, AND BLACK(3)-ELECTRONIC RESISTIVE LOAD.

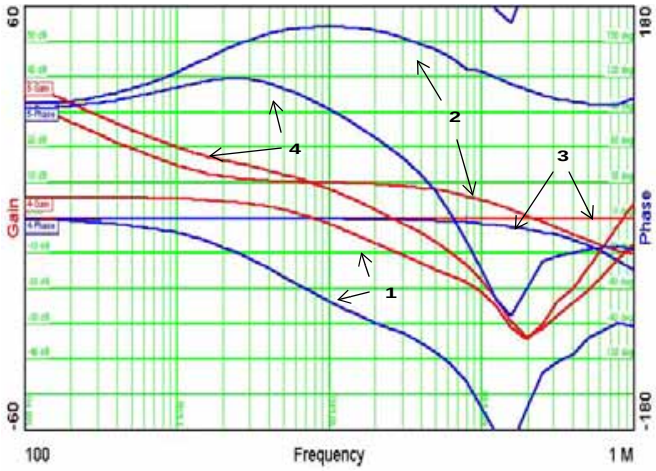


FIGURE 73. FREQUENCY RESPONSE OF 1) PLANT (Vo/Ve), 2) FEEDBACK COMPENSATION,
3) DIFFERENTIAL AMPLIFIER, AND
4) OPEN LOOP FOR V_{IN}=48V, V_{OUT}=3.3V@38A RESISTIVE LOAD. RED-GAIN AND BLUE-PHASE

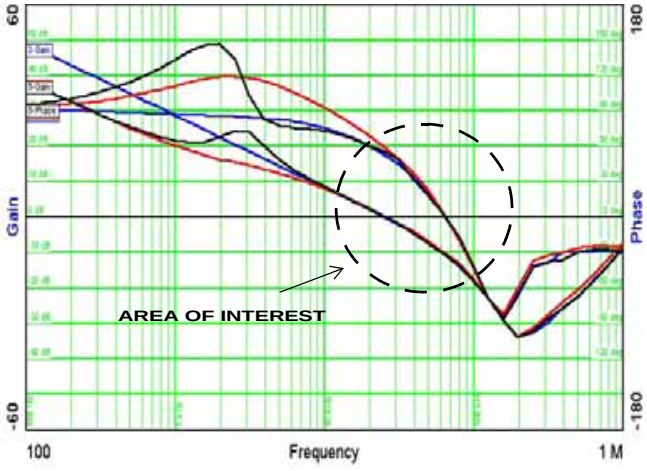


FIGURE 75. OPEN LOOP RESPONSE FOR THREE KINDS OF LOADS AT 48V, 3.3V@38A. RED-"PURE" RESISTIVE LOAD, BLUE-ELECTRONIC CONSTANT CURRENT LOAD, AND BLACK-ELECTRONIC RESISTIVE LOAD

Figure 73 shows three portions of the system loop for 3.3V 38A resistive loaded output: 1) Plant (Vo/Ve), 2) Feedback compensation, and 3) Differential amplifier. The overall loop is the sum of these components, in which the feedback compensation and the differential amplifier are fixed elements and the plant is a variable depending on the load.

Figure 75 shows loop responses for three different types of loads: "pure" resistive load, electronic constant current load, and electronic resistive load. The responses vary significantly at low frequencies, but the frequencies of interest that define the phase margin and gain margin shift little at high frequencies, therefore, the system stability can be studied by just looking at the loop response against the constant current load.

Figures 76 to 81 show loop responses for various input and output conditions including four corners. It can be concluded that the system is stable in under all input and output operating conditions since it has a 20-30kHz loop bandwidth, around 10dB gain margin, and above 45^{o} phase margin. One thing that should be noted is that the tail of the gain, caused by the ESL of output capacitors, at above 200kHz increases with the frequency. If it still exists and causes a problem in a real system, users can lower the pole at the differential amplifier stage to smooth it out (say 100pF for both C27 and C28). The gain of the feedback compensation however should be adjusted, as necessary, to design a favorable gain margin and phase margin system.

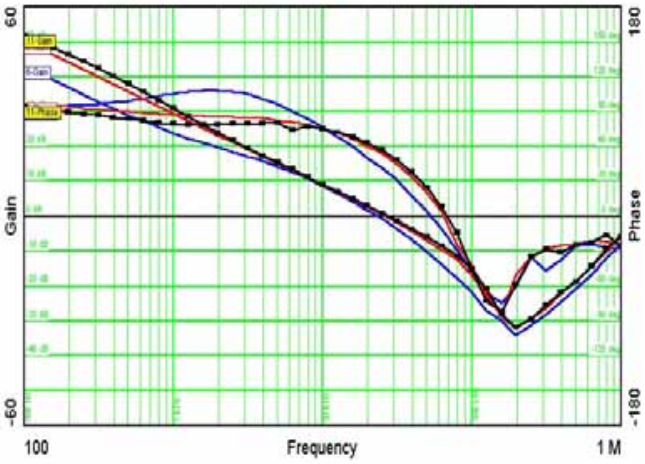


FIGURE 76. OPEN LOOP RESPONSE FOR 2.64V@60A CONSTANT CURRENT LOAD. RED-48V, BLUE-75V, AND BLACK-36V

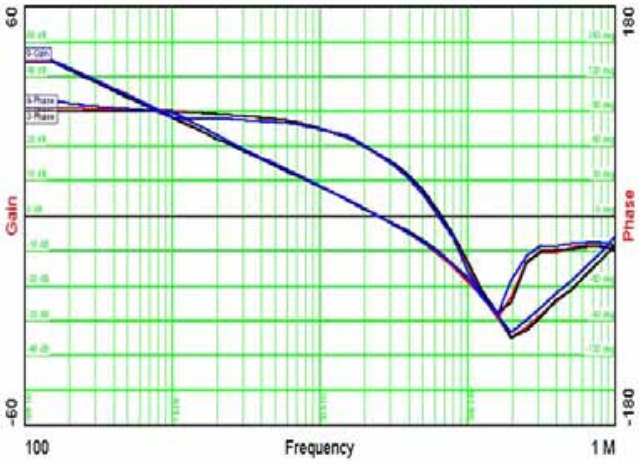


FIGURE 79. OPEN LOOP RESPONSE FOR 2.64V @6A CONSTANT CURRENT LOAD. RED-48V, BLUE-75V, AND BLACK-36V

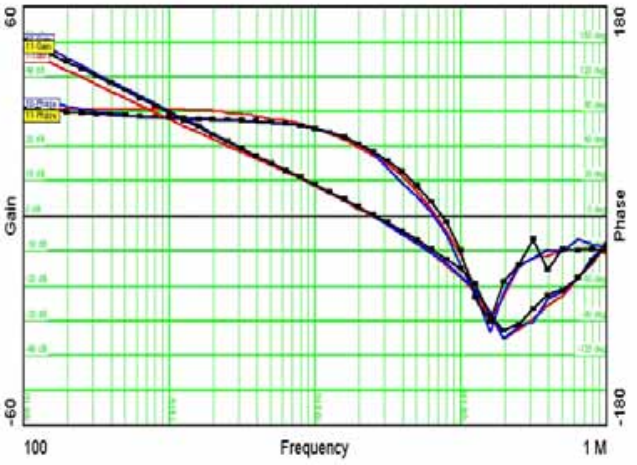


FIGURE 77. OPEN LOOP RESPONSE FOR 3.3V@60A CONSTANT CURRENT LOAD. RED-48V, BLUE-75V, AND BLACK-36V

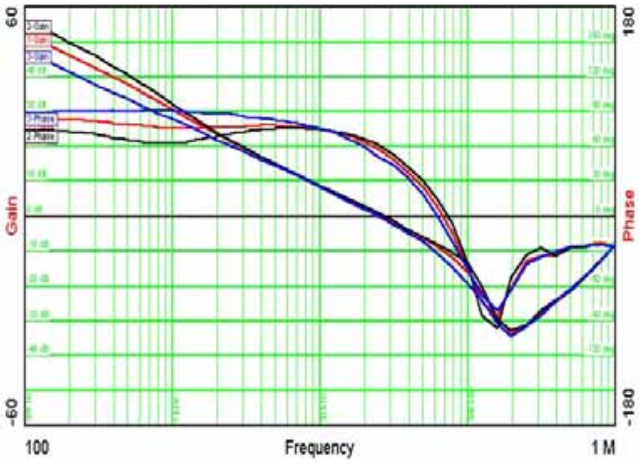


FIGURE 80. OPEN LOOP RESPONSE FOR 3.3V@6A CONSTANT CURRENT LOAD. RED-48V, BLUE-75V, AND BLACK-36V

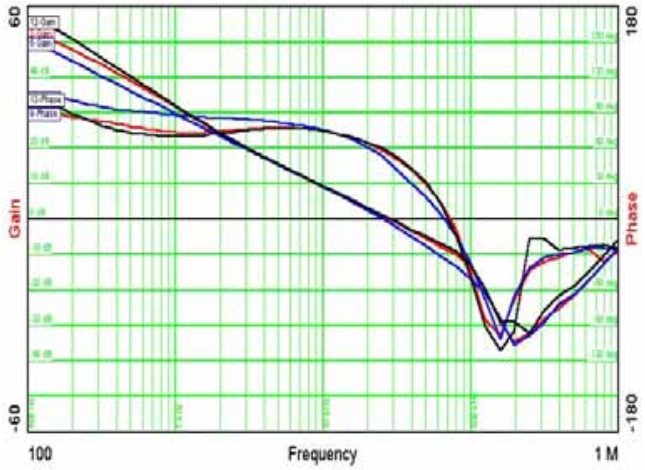


FIGURE 78. OPEN LOOP RESPONSE FOR 3.64V@60A CONSTANT CURRENT LOAD. RED-48V, BLUE-75V, AND BLACK-36V

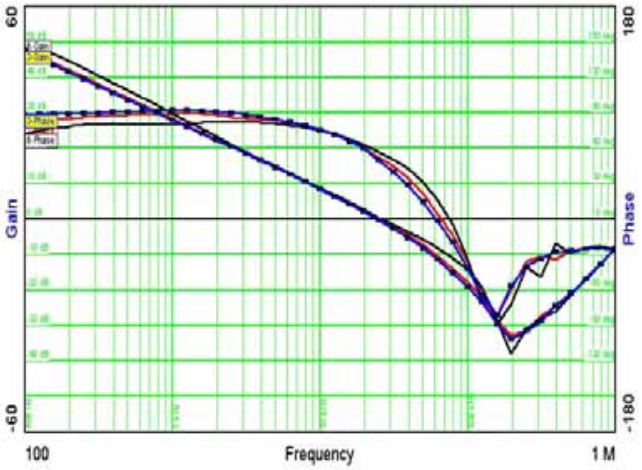


FIGURE 81. OPEN LOOP RESPONSE FOR 3.64V@6A CONSTANT CURRENT LOAD. RED-48V, BLUE-75V, AND BLACK-36V

In addition to the above loop measurement, the following presents some modeling results using the simplified loop system including the high-frequency correlation term as discussed in the *Control Loop Design* section on page 16.

The feedback compensation and the differential amplifier stages are verified with the 350 Venable System, as shown in Figures 82 and 83. They are well matched with the theoretical results except that the phase at the differential amplifier stage is smaller at above 100kHz than is expected. In addition, each TAIYO YUDEN capacitor is characterized with 100uF capacitance in series with 1.8mΩ ESR and 6nH ESL as defined in EQ. 61, which is also verified with the Venable System.

$$Zcap(j\omega) = \frac{1}{j\omega 100x10^{-6}} + 1.8x10^{-3} + j\omega 6x10^{-9} \qquad \text{(EQ. 61)}$$

Thus, the only variable is the plant, i.e., the load and the power train.

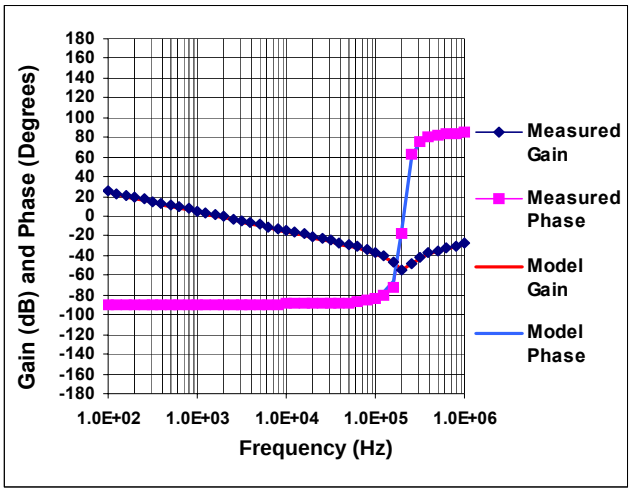


FIGURE 84. OUTPUT CAPACITOR MODELING

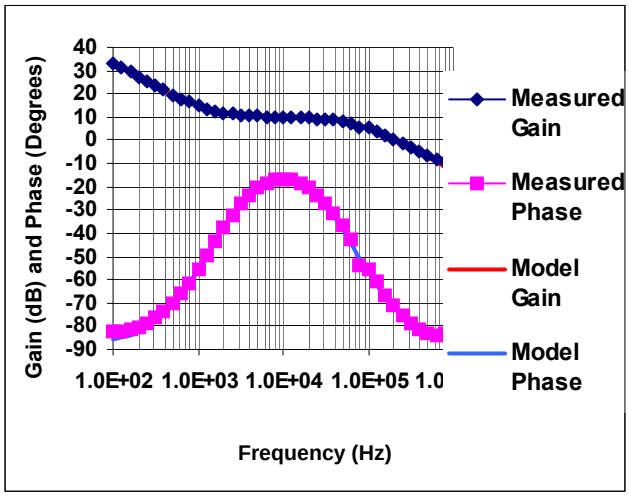


FIGURE 82. COMPENSATION STAGE

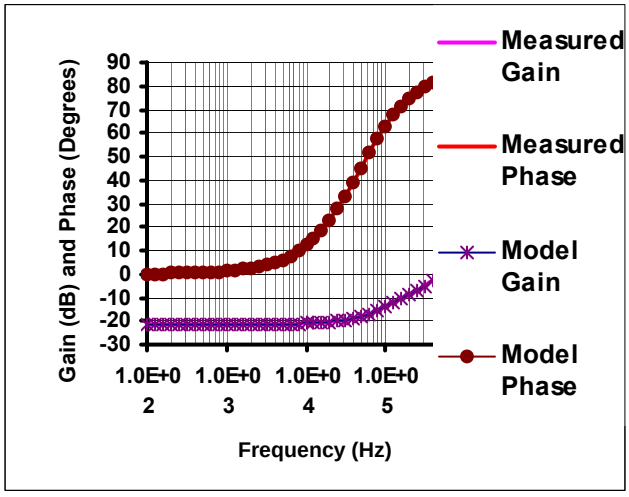


FIGURE 85. OUTPUT LOAD

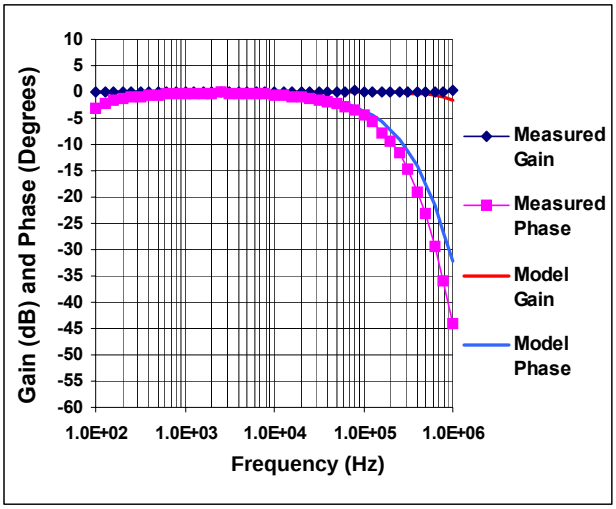


FIGURE 83. DIFFERENTIAL STAGE

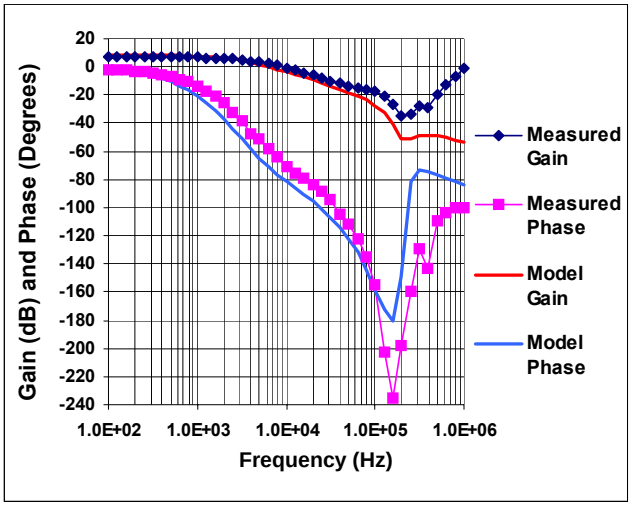


FIGURE 86. PLANT RESPONSE FOR 38A "PURE" RESISTIVE LOAD

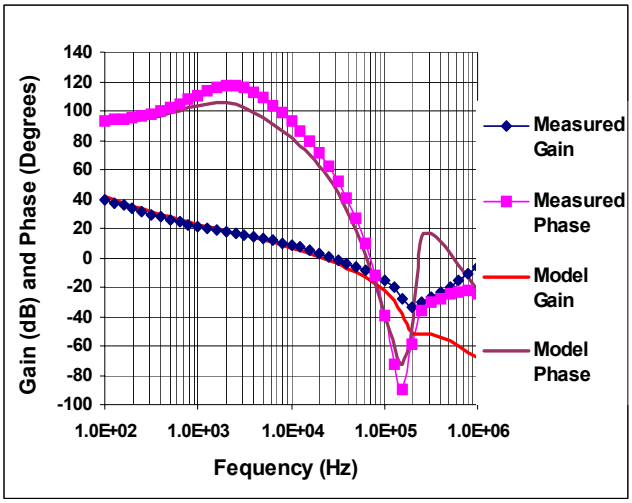


FIGURE 87. LOOP RESPONSE FOR 38A "PURE" RESISTIVE LOAD

The measured loop and plant responses for 48V input and 3.3V output with the resistive load, which is characterized in Figure 85, have a reasonable match with that of the simplified model, as shown in Figure 87.

The loop response in overall "pure" resistive load conditions was not tested. Instead, an electronic constant current load was used. The results are not significantly off from that of the "pure" resistive load within the frequencies of interest, as shown in Figure 75. Figures 88 and Figure 89 show a good prediction of phase margin and gain margin of the system using the simplified model in overall operating conditions.

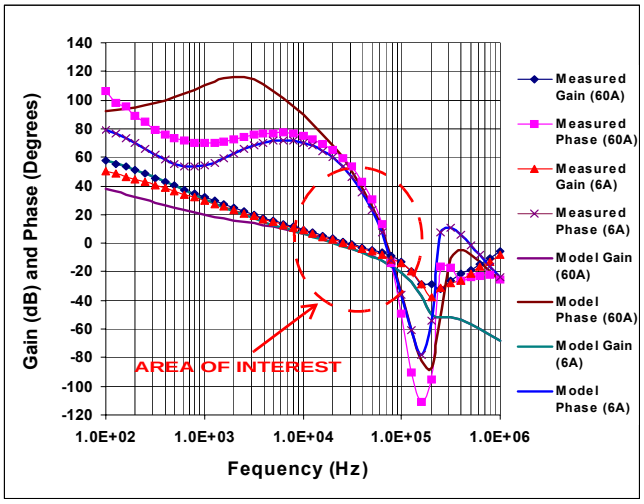


FIGURE 88. LOOP RESPONSE FOR 36V, 3.63V@6A AND 60A

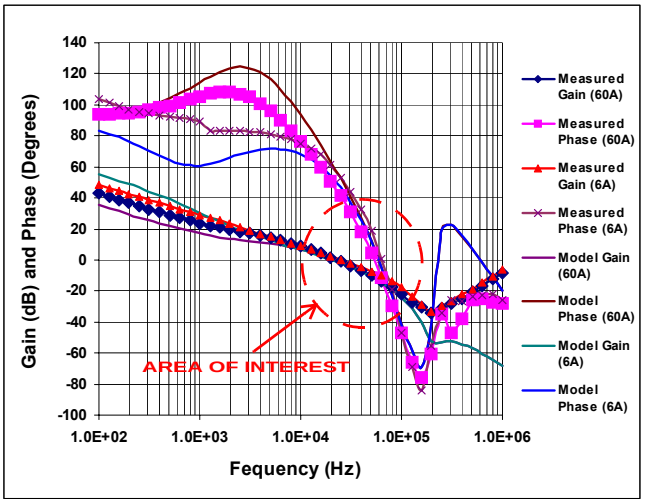


FIGURE 89. LOOP RESPONSE FOR 75V, 2.64V@6A AND 60A

Output Voltage

OUTPUT RIPPLE VOLTAGE

The output ripple voltage in different operating conditions is no greater than 60mV, as summarized in Table 7. The results show that the output has the largest output ripple voltage at the highest input line and the highest output voltage since the highest output ripple current is at this operating point. Note that the ripple current in the table is not for discontinuous mode. Figure 90 shows the converter operating in burst mode at very light load. Figure 93 and 94 show the converter operates at 48V, 3.3V, and 0.5A load with synchronous FETs turned off and on, respectively. The one with synchronous FETs turned on has a larger duty cycle than the one with synchronous FETs turned off, which runs at discontinuous mode since the body diodes of the turned-off FETs block the output inductor current from flowing negatively. Note that the channel 1 represents the output ripple voltage and the channel 3 represents the voltage across the secondary winding.

TABLE 7. OUTPUT VOLTAGE RIPPLE

V_{IN}	V_{OUT}	0.5A SYN OFF	0.5A SYN ON	60A LOAD	RIPPLE CURRENT
36V	3.63V	21.9mV	25.0mV	32.8mv	5.4A
48V	3.31V	25.0mV	28.1mV	34.4mV	9.0A
75V	2.64V	56.2mV	37.5mV	48.4mV	10.8A
75V	3.63V	59.4mV	46.9mV	59.4mV	12.9A

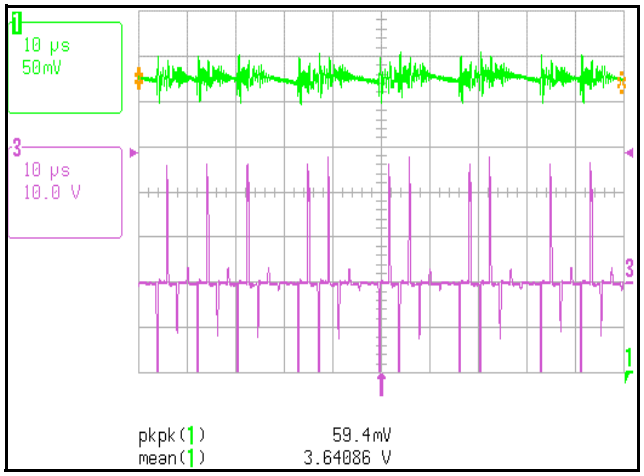


FIGURE 90. OUTPUT VOLTAGE RIPPLE (CHANNEL 1) AT V_{IN}=75V, V_{OUT}=3.63V, AND I_{OUT}=0.5A. SYN OFF

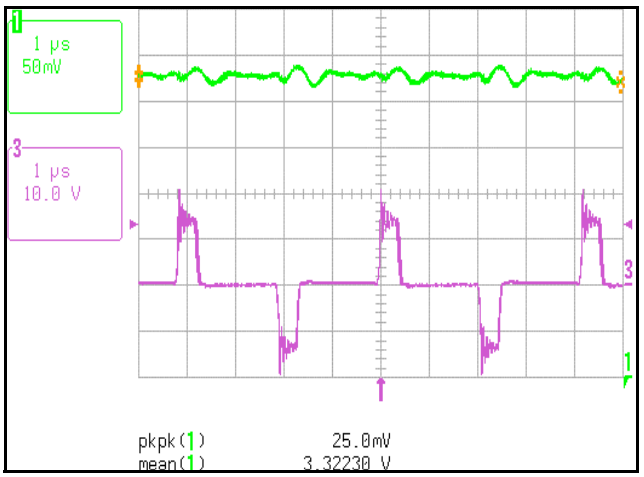


FIGURE 93. OUTPUT VOLTAGE RIPPLE (CHANNEL 1) AT V_{IN}=48V, V_{OUT}=3.3V, AND I_{OUT}=0.5A. SYN OFF

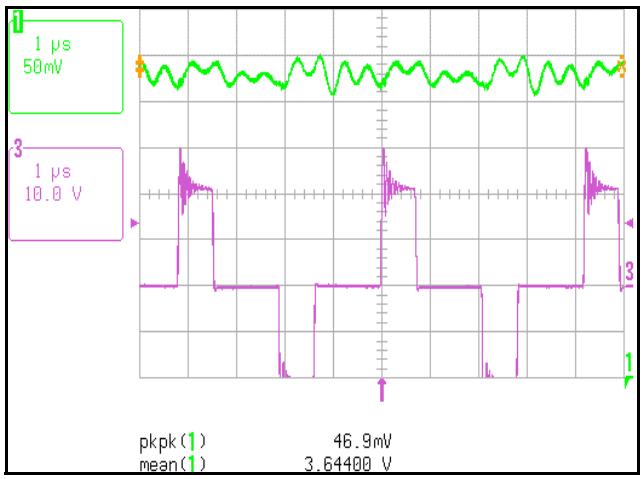


FIGURE 91. OUTPUT VOLTAGE RIPPLE (CHANNEL 1) AT V_{IN}=75V, V_{OUT}=3.63V, AND I_{OUT}=0.5A. SYN ON

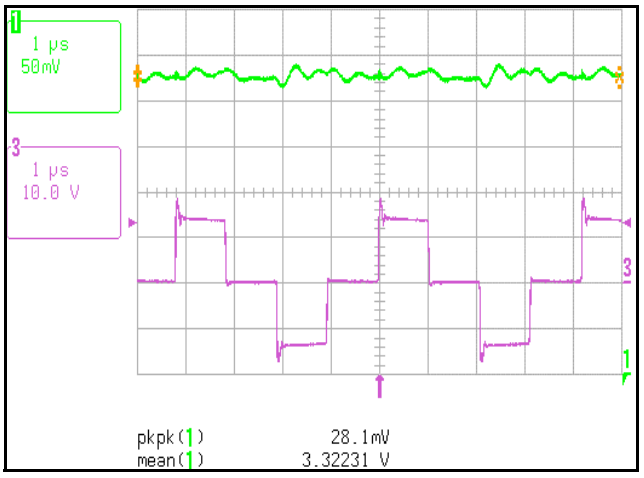


FIGURE 94. OUTPUT VOLTAGE RIPPLE (CHANNEL 1) AT V_{IN}=48V, V_{OUT}=3.3V, AND I_{OUT}=0.5A. SYN ON

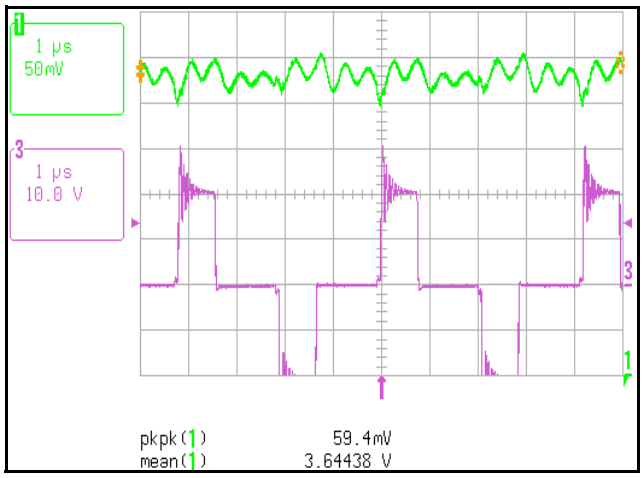


FIGURE 92. OUTPUT VOLTAGE RIPPLE (CHANNEL 1) AT V_{IN}=75V, V_{OUT}=3.63V, AND I_{OUT}=60A

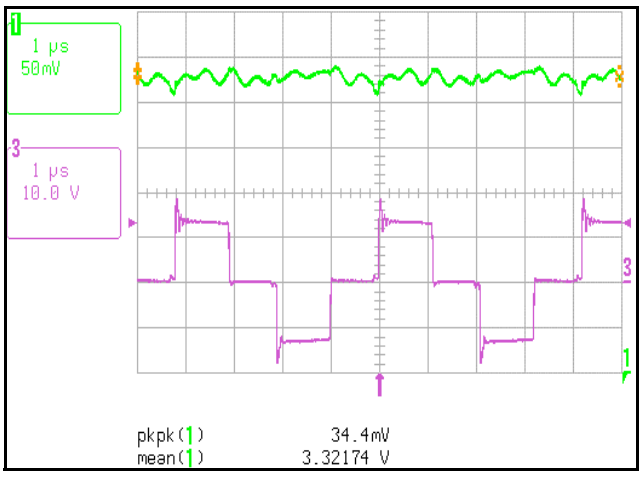


FIGURE 95. OUTPUT VOLTAGE RIPPLE (CHANNEL 1) AT V_{IN}=48V, V_{OUT}=3.3V, AND I_{OUT}=60A

Output Start Up

The start up characteristic of the output voltage heavily depends on the load. For a “pure” resistive load or an electronic load with low slew rate (0.01A/us), the output voltage comes up smoothly, as shown in Figures 96 and 97. In the case of high slew rate electronic load, the monotonicity of the output voltage is lost, as shown in Figures 98 and 99. During the startup, the load demands more current than what the converter can deliver, which causes the output dipping. The higher the load is, the higher the current ramp is needed, and the higher the error voltage is required to push the duty cycle up further. The error voltage is limited by the soft start voltage (Vclamp) that comes up with a slower speed, therefore, the duty cycle is limited causing repetitive up/downs at the output voltage, as shown in Figure 100. For applications with similar behavior of the electronic load, this problem can be resolved by speeding up the startup of the soft start with two possible options: 1) increase the soft start speed above the start-up speed of the error voltage by reducing the capacitive load at the CSS pin of ISL6551; or 2) set the soft start at the output reference pin (EANI) and completely remove all capacitive load at the CSS pin. In general, the second option is the practical one. Note that the delay at the electronic load is caused by its turn-on threshold.

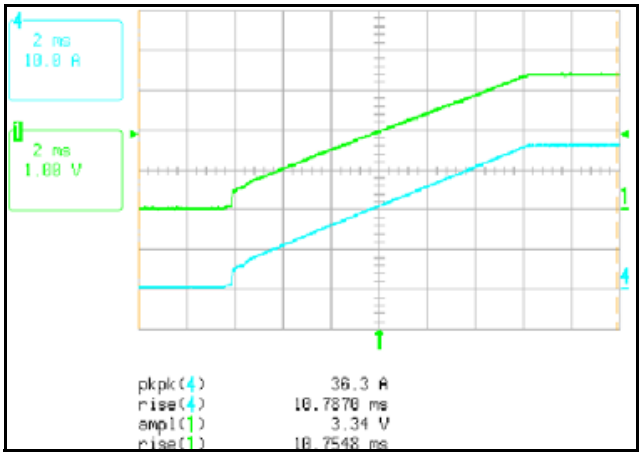


FIGURE 96. OUTPUT VOLTAGE (CHANNEL 1) AT V_{IN}=48V, V_{OUT}=3.3V, AND 0.083Ω RESISTIVE LOAD

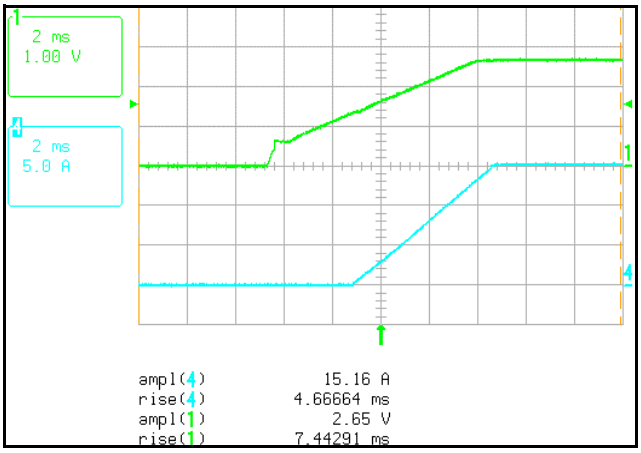


FIGURE 97. OUTPUT VOLTAGE (CHANNEL 1) AT V_{IN}=75V, V_{OUT}=2.64V, AND I_{OUT}=60A, 0.01A/US ELECTRONIC CONSTANT CURRENT MODE (CHANNEL 4, 1/4 OF THE LOAD)

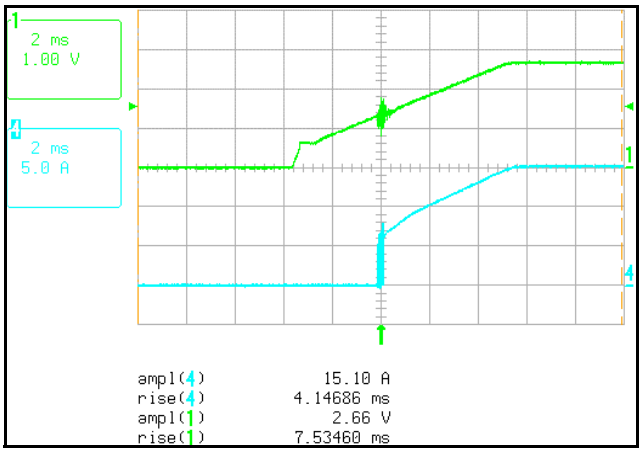


FIGURE 98. OUTPUT VOLTAGE (CHANNEL 1) AT V_{IN}=75V, V_{OUT}=2.64V, AND I_{OUT}=60A, 1A/US ELECTRONIC RESISTIVE MODE (CHANNEL 4, 1/4 OF THE LOAD)

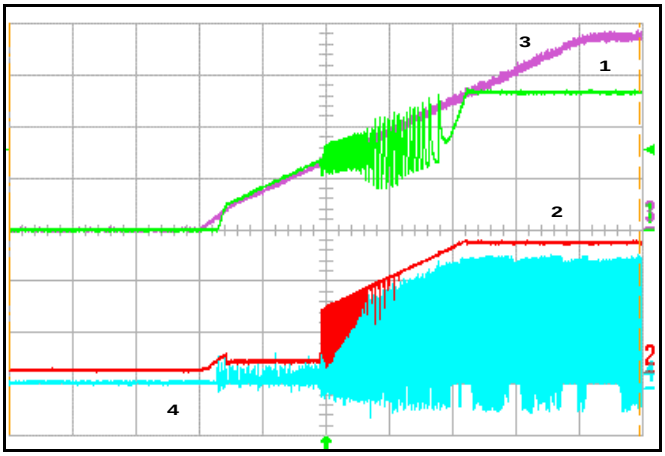


FIGURE 99. OUTPUT VOLTAGE (CHANNEL 1) AT V_{IN}=48V, V_{OUT}=2.64V, AND I_{OUT}=60A, 1A/US ELECTRONIC CONSTANT CURRENT MODE. CHANNEL 2: ERROR VOLTAGE; CHANNEL 3: VCLAMP VOLTAGE; CHANNEL 4: CURRENT RAMP (ISENSE). EACH CHANNEL IS 1V/DIV AND 2MS/DIV.

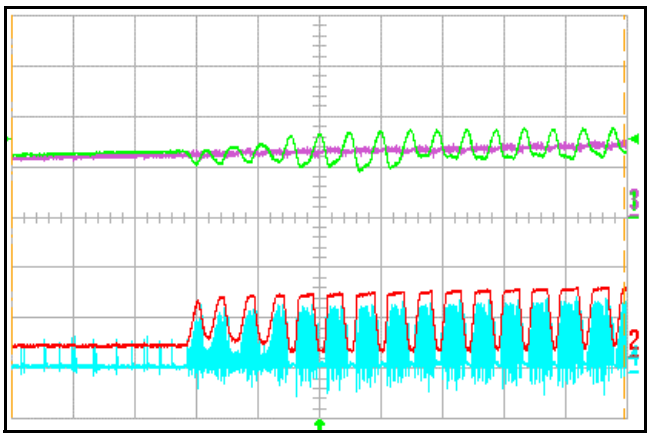


FIGURE 100. OUTPUT VOLTAGE STARTUP EXPANSION (CHANNEL 1) AT V_{IN}=48V, V_{OUT}=2.64V, AND I_{OUT}=60A, 1A/US ELECTRONIC CONSTANT CURRENT MODE. CHANNEL 2: ERROR VOLTAGE; CHANNEL 3: VCLAMP VOLTAGE; CHANNEL 4: CURRENT RAMP (ISENSE). 100US/DIV.

Output Turned Off Characteristic

When the converter is turned off by an operator or a fault, the energy stored in the output inductors and capacitors is dissipated in the parasitic resistance of the output inductors and capacitors, the load, and the synchronous FETs.

In Figure 101, the output current lags by 90° from the output voltage, which means that the output load (electronic load) behaves inductively when the converter is turned off. Note that the electronic load is not activated until its input is above 0.95V. The delay to turn off the synchronous FETs is induced by the C60 and C58 in the peak current detecting circuit on page 6 of the schematics, which allows negative currents through the Channels during this period. Since the electronic load does not behave resistively and the losses due to the Rds(on) of the synchronous FETs are relatively small, the output L-C resonant tank cannot be heavily dampened, which causes the output ringing down to an undesired negative voltage (-2V). With an 1000uF Aluminum capacitor at the output, the resonant frequency decreases but the stored energy increases; however, the negative spike does cut down by a small amount, as shown in Figure 102. With the assistance of additional output capacitance and additional circuits, as shown on page 6 of the schematics (D131...), to turn off the synchronous FETs by a fault or an operator, the negative spike is reduced to an acceptable level (200mV), as shown in Figure 104. Note that the 1000uF Aluminum capacitor at the output is necessary to help reduce the negative spike to a controllable level.

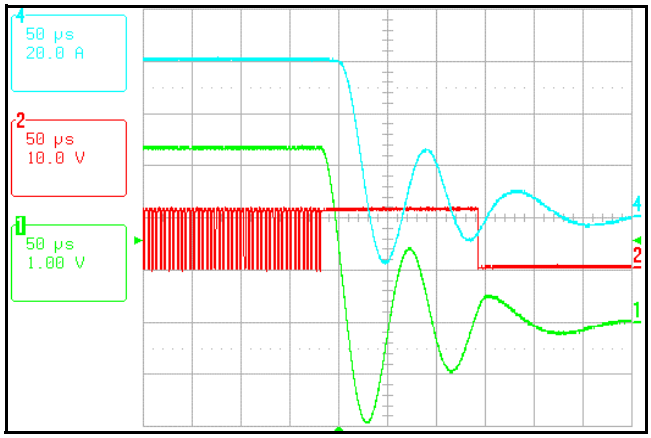


FIGURE 101. V_{IN}=48V, V_{OUT}=3.3V, I_{OUT}=60A ELECTRONIC LOAD WITH NO ADDITIONAL CAP. CHANNEL 1: OUTPUT VOLTAGE; CHANNEL 2: SYNCHRONOUS FET GATE SIGNAL; CHANNEL 4: OUTPUT CURRENT

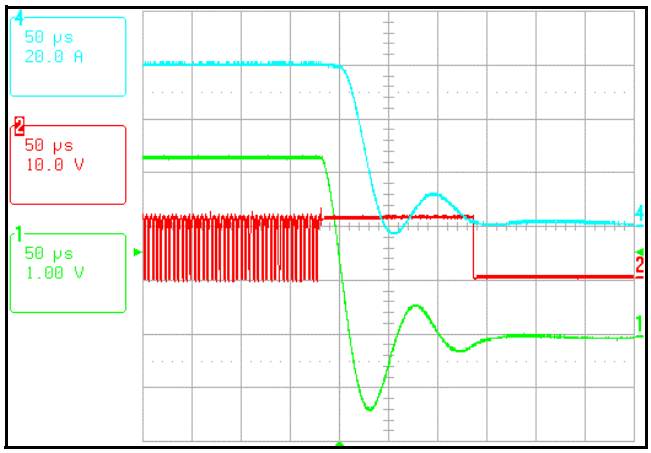


FIGURE 102. V_{IN}=48V, V_{OUT}=3.3V, I_{OUT}=60A ELECTRONIC LOAD WITH 1000uF ALUMINUM CAPACITOR. CHANNEL 1: OUTPUT VOLTAGE; CHANNEL 2: SYNCHRONOUS FET GATE SIGNAL; CHANNEL 4: OUTPUT CURREN

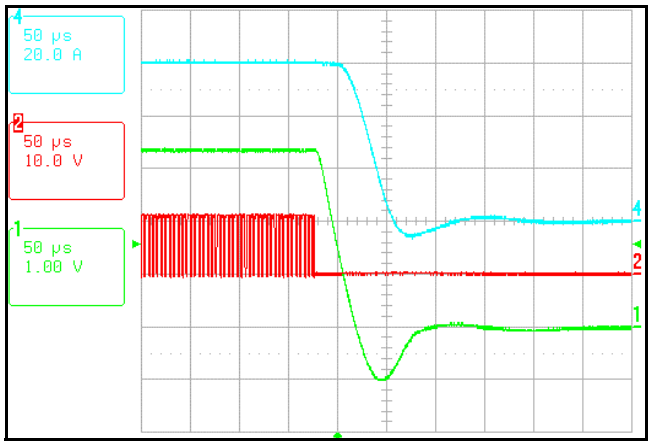


FIGURE 103. V_{IN}=48V, V_{OUT}=3.3V, I_{OUT}=60 ELECTRONIC LOAD WITH NO ADDITIONAL CAP. CHANNEL 1: OUTPUT VOLTAGE; CHANNEL 2: SYNCHRONOUS FET GATE SIGNAL; CHANNEL 4: OUTPUT CURRENT

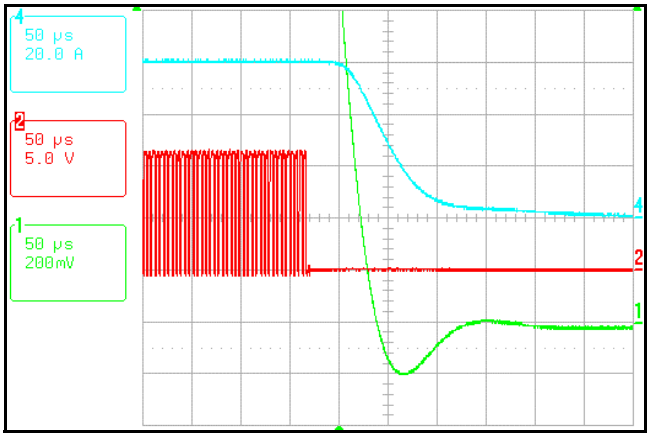


FIGURE 104. V_{IN}=48V, V_{OUT}=3.3V, I_{OUT}=60A ELECTRONIC LOAD WITH 1000UF ALUMINUM CAPACITOR. CHANNEL 1: OUTPUT VOLTAGE; CHANNEL 2: SYNCHRONOUS FET GATE SIGNAL; CHANNEL 4: OUTPUT CURRENT

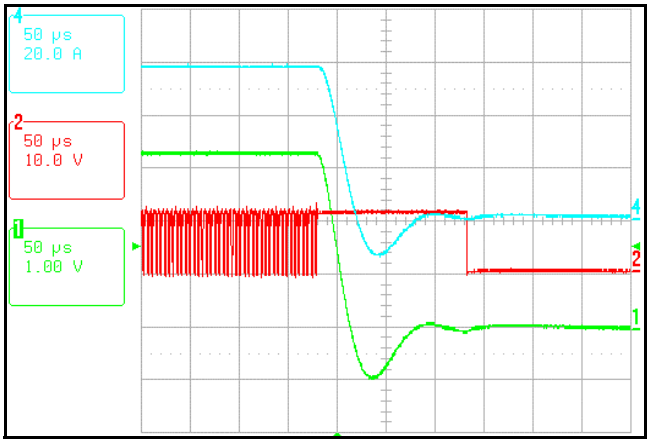


FIGURE 105. V_{IN}=48V, V_{OUT}=3.3V, I_{OUT}=60A PURE RESISTIVE LOAD WITH NO ADDITIONAL CAP. CHANNEL 1: OUTPUT VOLTAGE; CHANNEL 2: SYNCHRONOUS FET GATE SIGNAL; CHANNEL 4: OUTPUT CURRENT

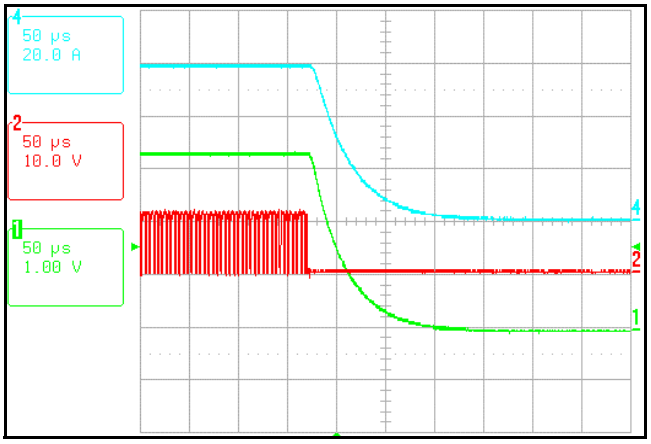


FIGURE 106. V_{IN}=48V, V_{OUT}=3.3V, I_{OUT}=60A PURE RESISTIVE LOAD WITH NO ADDITIONAL CAP. CHANNEL 1: OUTPUT VOLTAGE; CHANNEL 2: SYNCHRONOUS FET GATE SIGNAL; CHANNEL 4: OUTPUT CURRENT

As shown in Figure 105, the output voltage and the output current are in phase since the load is resistive (two DALE NH-25 25W 0.1W in parallel, they operate for only a short period due to their power ratings). The negative spike is much smaller than that of the previous case because the load helps dissipate some of the residual energy. When the synchronous FETs are turned off at the shutdown of the converter, the body diodes of the synchronous FETs help dissipate a large portion of the energy and block any negative current through the output inductors resulting in zero negative spike, as shown in Figure 106. In this case, no extra capacitor is required.

Equipment List

TABLE 8. EQUIPMENT LIST

EQUIPMENT	EQUIPMENT DESCRIPTIONS
Boards Used	ISl6551EVAL1 Rev. B, #1, #2, #3, & #4
Power Supplies	1. HP 6653A S/N: 3621A-03425 2. Lamda LQ521 S/N: J 3570 3. XANTREX 100-10 S/N: 72963 4. XANTREX 100-6 S/N: 66287 5. HP6205C S/N: 2411A-06136
Oscilloscope	LeCroy LT364L S/N: 01106
Differential Probe	Hewlett Packard HP1141A
Multimeters	Fluke 8050A S/N: 2466115 & 3200834
Load	1. Chroma 63103 S/N: 631030002967 2. Chroma 63103 S/N: 631030003051 3. Four DALE NH-25 25W 0.1Ω 1%
Current Probe Amplifier	LeCroy AP015 SN: 970139
Temperature Probe	Fluke 80T-IR Infrared Temperature Probe (93/09)
Fan	POPST-MOOREN TYP 4600X (4098547)

Schematics Description

There are six pages of schematics. On the first page is the secondary side power train including the output filter and the synchronous rectifiers with their drivers. Additional circuits are used to turn off the synchronous FETs during the start up and to clamp the ringings across the FETs on the leading edge. On page 2 is the primary power train. It consists of an input filter, current transformer, main transformer, pulse transformer, and full-bridge power switches with their drivers. On page 3 are the main supervisor circuits ISL6550 with some external resistor components, which can differentially sense the output voltage, set the output under-voltage and over-voltage protection, program the output reference with four VID inputs, and set an appropriate output under-voltage lockout delay. On page 4 are the full-bridge controller and the master over-voltage circuit. On page 5 are the input under-voltage and thermal condition detecting circuits. The circuits on the last page are used to monitor the output load level during the start up. It turns off the synchronous FETs during the start up at low load conditions. Once the FETs are turned

on, they will not be turned off again unless the converter re-start up at low load conditions. In addition to that, some circuits are used to turn off the synchronous FETs at a high speed to eliminate any negative voltage spike when the converter is shut down by an operator or a fault.

Layout

The components of the converter are placed on both top and bottom layers within a particular area. Figures 107 and 108 show where each portion of circuit is placed on both layers. Since it is a high current density design, 10 layers with 4 oz copper have been used in the PCB layout. In addition, a buried vias technique has also been applied. A careful and proper layout helps to lower EMI and reduce bugs and development time. Users should use as much time as needed and is possible to layout the board very carefully following guidance. Some guidance for laying out the reference design is discussed in the Layout Considerations section on page 17. Refer to [5] for additional layout guidelines.

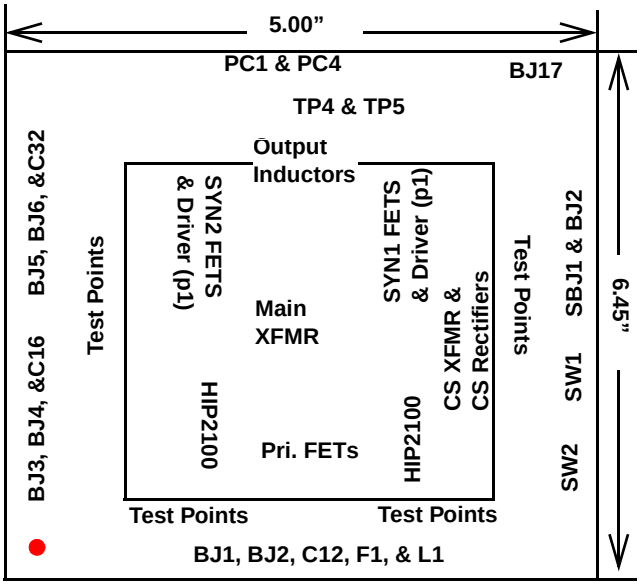


FIGURE 107. COMPONENT PLACEMENT OUTLINE ON TOP LAYER

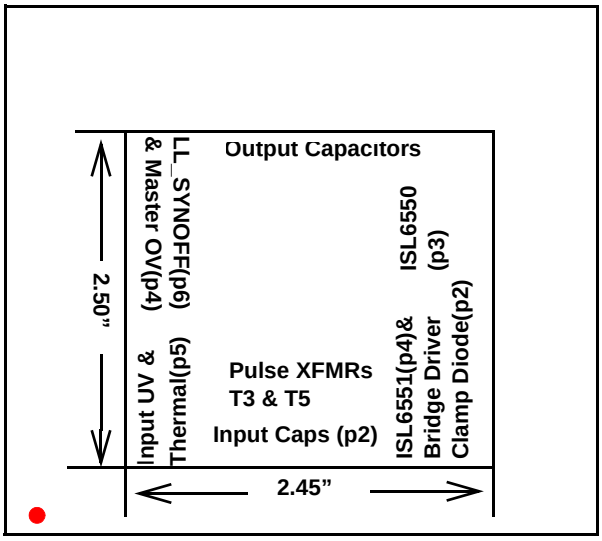


FIGURE 108. COMPONENT PLACEMENT OUTLINE ON BOTTOM LAYER

Conclusion

The ZVS technique of the ISL6551 full-bridge controller is presented. The superior performance of the ISL6551, with its companions Intersil’s HIP2100 half-bridge driver and ISL6550 Supervisor And Monitor, has been demonstrated in the reference design of a 200W, 470kHz telecom power supply incorporating both full-bridge and current doubler topologies.The converter is implemented with secondary-side peak current mode control and includes output overload, input under-voltage, and output over-voltage and under-voltage protection features. A footprint for a thermistor is ready for users to implement thermal protection on the primary side. An ultra high efficiency of 88% at 3.3V output and 60A full load has been achieved.

This application note includes a step-by-step design procedure for the converter, which allows for easier component selection and customization of this reference design for a broader base of applications. Users can use equations, presented in the *CONVERTER DESIGN* section to determine the turns ratio of the main transformer and the switching frequency, to estimate power dissipation of primary switches and synchronous rectifiers, and to calculate I/O filters design parameters. By entering these calculations in a worksheet, users can do numerical iterations and choose appropriate components for their applications in an easier manner. The open loop response of the system can be roughly approximated using the simplified model.

In addition, extensive experimental results give users a better understanding of the operation of the converter, the ISL6551, and the ISL6550.

TERM DEFINITIONS

Cin	Input Capacitance
Co	Output Capacitance
Coss	Output Capacitance of MOSFET
Cp	Primary Capacitance of Transformer
D	Ratio of On-Time Interval of Lower FET to One Clock Period (1/Fclock), Duty Cycle
dI	Ripple Current thru Each Output Inductor
dIo	Overall Ripple Current thru Output Capacitors
Dmaxav	Maximum Available Duty Cycle
dV_{Co}	Output Ripple Voltage due to Output Capacitance
dV_{ESL}	Ripple Voltage Contributed by ESL of Output Capacitance
dV_{ESR}	Ripple Voltage Contributed by ESR of Output Capacitors
dVincap	Allowable Input Ripple Voltage Contributed by the Input Capacitors
dVtr	Output Transient at 25% Step Load
ΔV_{CAP}	Transient due to Output Capacitance
ΔV_{ESL}	Initial Transient Spike due to ESL
E_C	Energy Stored in Primary Parasitic Capacitance
E_L	Energy Stored in Commutating Inductance
ESR	Overall ESR of Output Capacitors
ESRin	Overall ESR of Input Capacitors
ESL	Overall ESL of Output Capacitors
f_c	System Closed-Loop Bandwidth
Fclock	Internal Clock Frequency
F_{DIST}	Current Distribution Factor thru Synchronous FETs
Fsw	Switching Frequency
He	Transfer Function of Error Amplifier
Hd	Transfer Function of Differential Amplifier
Hopen	Open Loop Transfer Function for Simplified Model
Hopen2	Open Loop Transfer Function with Subharmonic and Ramp Components Added
Hs	High-frequency Correction Term for Subharmonic Phenomenon
Idr	Driver Current
Iindpeak	Peak Current thru Each Output Inductor
Iindrms	RMS Current thru Each Output Inductor
Iinrms	RMS Current thru Input Capacitors
I_{LO}	Overall Ripple Current thru Output Inductors
I_{LO1}	Ripple Current thru Inductor Lo1
I_{LO2}	Ripple Current thru Inductor Lo2
Imag	Magnetizing Current

TERM DEFINITIONS (Continued)

Io	Output Load Current
Ion	Current at Turn-on
Iorms	RMS Current thru Output Capacitors
Ip	Current thru Primary Winding
Ipriavgfr	Average Current thru Body Diode of Upper FET in Freewheeling Period
Ipriavgres	Average Current thru Body Diode of Lower FET for a Td turn-on delay longer than Required Resonant Delay
Ipripeak	Peak Current thru Primary Winding /Power Switches
Iprirmsfr	RMS Current thru the Channel of Upper FET in Freewheeling Period
Iprirmstr	RSM Current thru Primary Switches in Power Transfer Period
Iprirms	Overall RMS Current thru Upper FET
Iprms	Overall RMS Current thru Primary Winding
IQ1	Current thru One Synchronous Leg, Q1
IQ2	Current thru Another Synchronous Leg, Q2
Is	Current thru Secondary Winding
Isrmstr	RMS Current thru Secondary Winding in Transfer Period
Isrmsfr	RMS Current thru Secondary Winding in Freewheeling Period
Isrms	Overall RMS Current thru Secondary Winding
Istep	Transient Load Step
Isyndeadavg	Average Current thru Body Diode of Synchronous FETs/External Schottky in SYNC DRIVE Scheme in Dead Time
Isynpeak	Peak Current thru Synchronous FET
Isynrms	Overall RMS Current thru Synchronous FETs
Isynrmstr	RMS Current thru Synchronous FETs in Power Transfer Period
Isynrmsfr	RMS Current thru Synchronous FETs in Clamped Freewheeling Period
Lext	External Commutating Inductance
Lk	Leakage Inductance
Lmag	Magnetizing Inductance
Lo	Inductance of Each Output Inductor
N	Main Transformer Turns Ratio (Np/Ns)
Ncs	Current Sense Transformer Turns Ratio
Nmax	Maximum Allowable Turns Ratio of Main Transformer
Pdr	Driver Switching Losses
Plowfet	Power Dissipation of Lower FET
Ppriswon	Switching Losses of Primary Switches at Turn-on

TERM DEFINITIONS (Continued)

Po	Output Power
Psynfet	Power Dissipation of Synchronous FET
Psynfetfr	Losses of Syn FET in Freewheeling Period
Pupfet	Power Dissipation of Upper FET
Qg	Gate Charge of MOSFET at V_{GS}
Rcs	Current Sense Resistor
Rdsonpri	Rds(on) of Primary Switches
Ro	Output Load Impendence
Rdsonsyn	Rds(on) of Synchronous FETs
Se	External Slope Added to Sn
Sn	Positive Slope of One Output Inductor Current
T	Clock Period
t_{DEAD}	Clock Dead Time
t_{on}	Primary MOSFET Switching Time at Turn On
t_{RESDLY}	Resonant Delay
Vcc	Bias Voltage of Drivers
Vdsyn	Body Diode Drop of Synchronous FETs
Vin	Input Voltage
Vinmax	Maximum Input Line
Vinmin	Minimum Input Line
Vinripple	Input Ripple Voltage
Vo	Output Voltage
Vmisc	Miscellaneous Voltage Drops Including Contact Resistance, Winding Resistance, PCB Copper Resistance
Vomax	Maximum Output Voltage
Von	Primary MOSFET V_{DS} at Turn-on
Voripple	Output Ripple Voltage
Vp	Voltage across Primary Winding
Vs	Voltage across Secondary Winding
Vsynfet	Voltage Drop of Synchronous FET due to Its Rds(on) at Half of the Load
Vsynmax	Maximum Voltage across V_{DS} of Syn FET
Zo	Impedance of Output Capacitors and Load

Acknowledgement

The author acknowledges the support of DT Magnetics for designing and providing magnetics samples.

References

[1] Laszlo Balogh, “Design Review: 100W, 400kHz, DC/DC Converter With Current Doubler Synchronous Ratification Achieve 92% Efficiency.” Unitrode Integrated Circuit Corporation.

[2] Laszlo Balogh, “The Current doubler Rectifiers: An Alternative Rectification Technique For Push-Pull and Bridge Converters,” Design Note-63, Unitrode Integrated Circuit Corporation.

[3] Vatché Vorpérian, “Simplified Analysis of PWM Converters Using the Model of the PWM Switch Part I: Continuous Conduction Mode.” IEEE Transactions on Aerospace and Electronics Systems Vol 26, No. 3 May 1990 p. 490-496.

[4] “Designers’s Series - Part V Current-Mode Control Modeling.” Switching Power Magazine. July 2001, Volume 2, Issue 3.

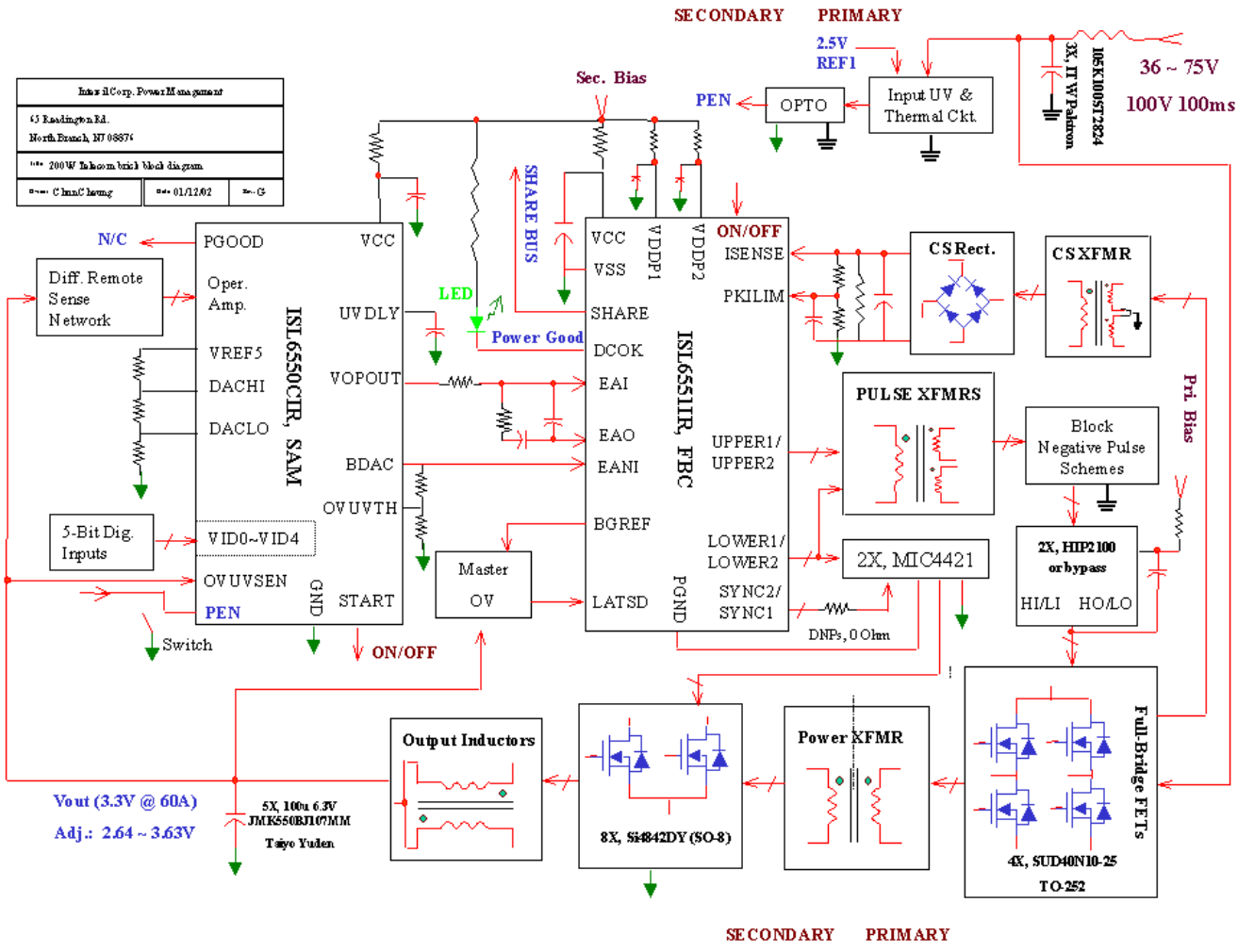
[5] “PCB Design Guidelines For Reduced EMI.” Texas Instrument: SZZA009, November 1999.

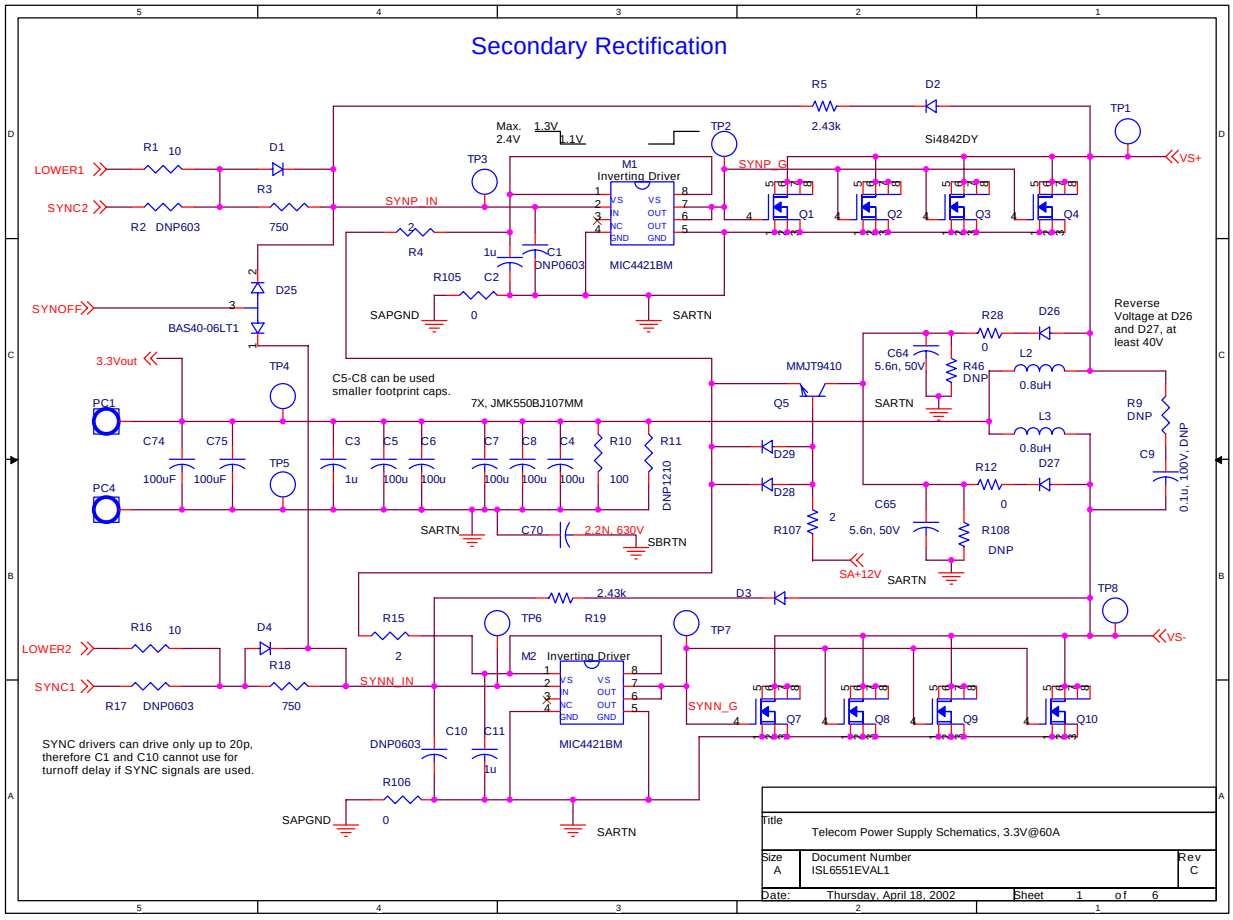
[6] Rais Miftakhutdinov. “An Analytical Comparison of Alternative Control Technique for Powering Next Generation Microprocessors.” TI-Unitrode Power Supply Design Seminar, 2001 Series.

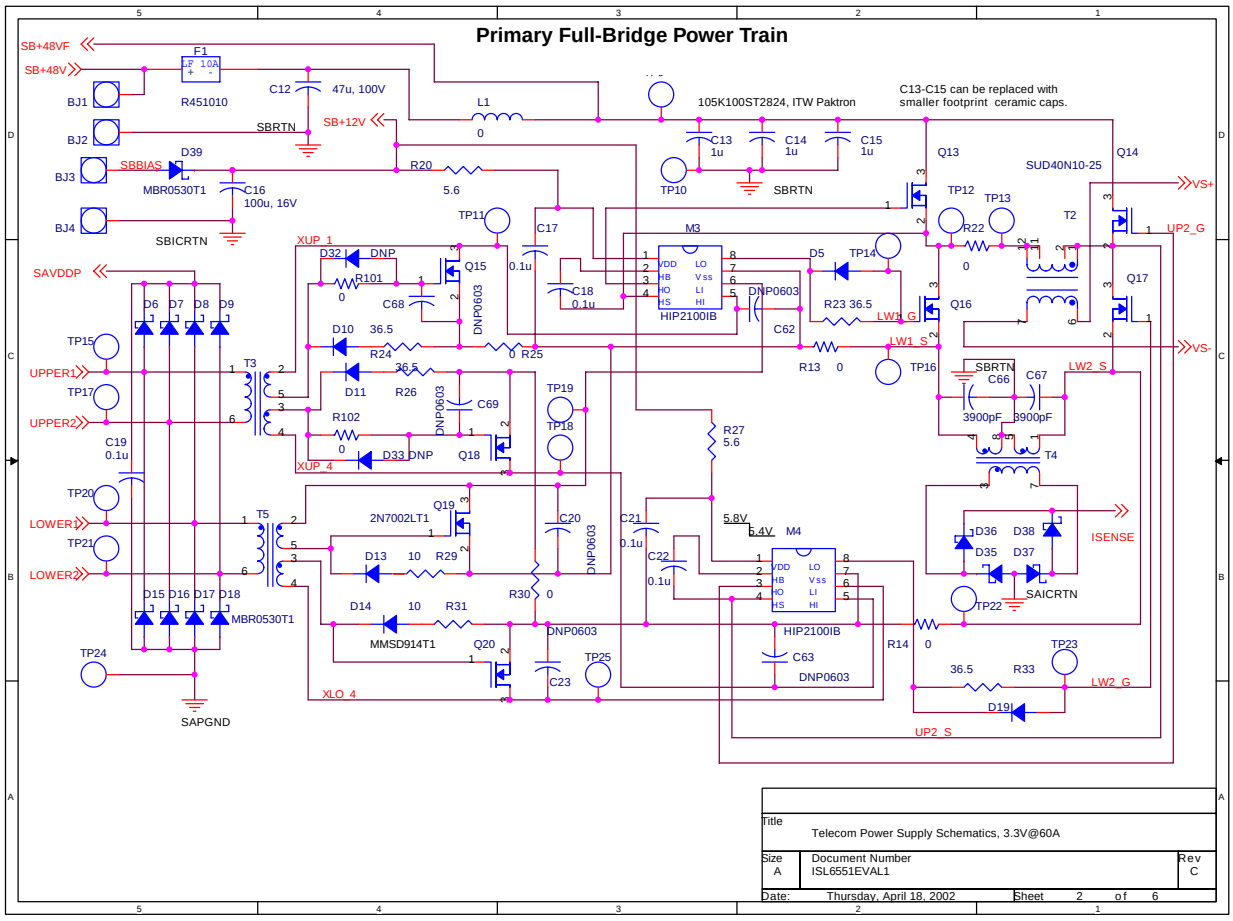
[7] Vatché Vorpérian. Analytical Methods in Power Electronics (Lecture Note). CA: California Institute of Technology.

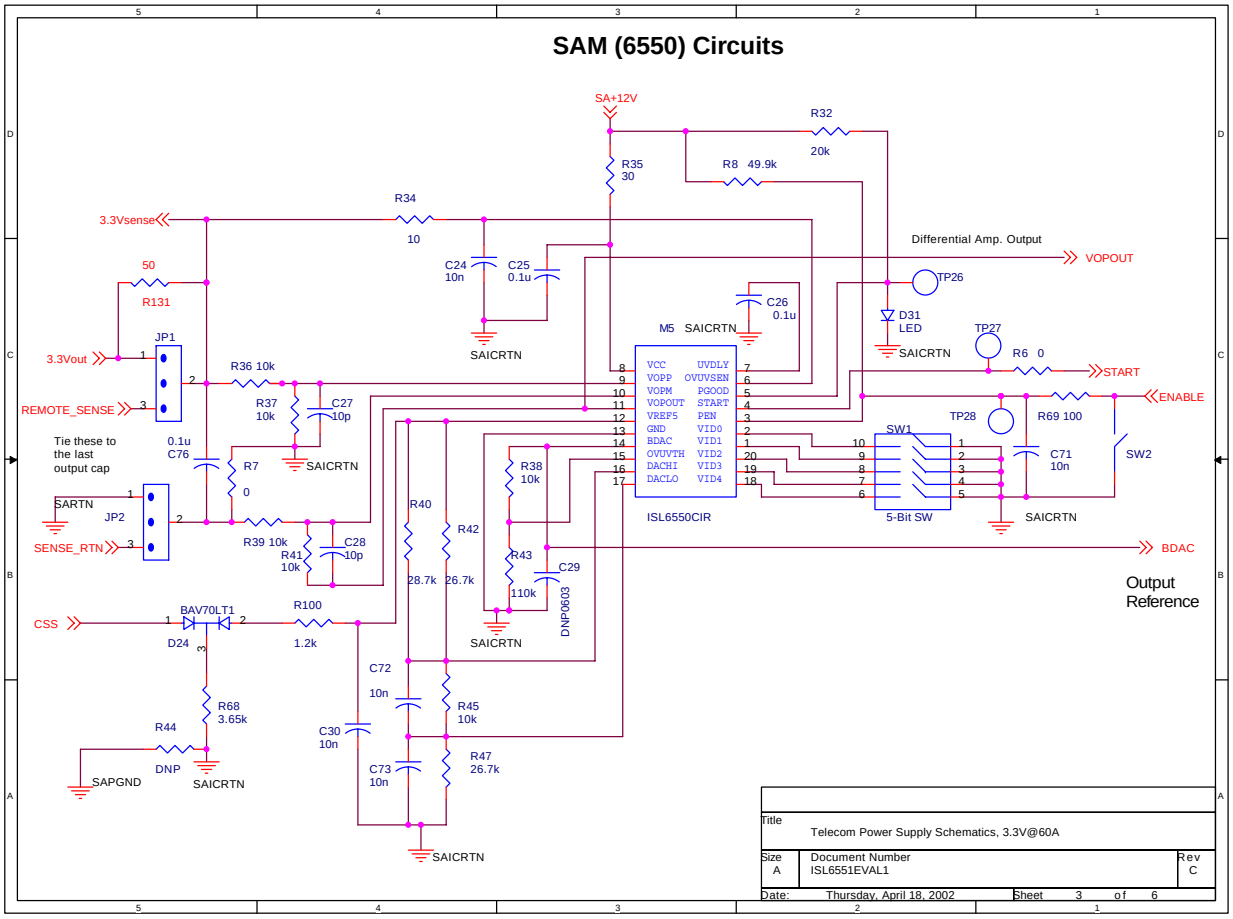
Appendix

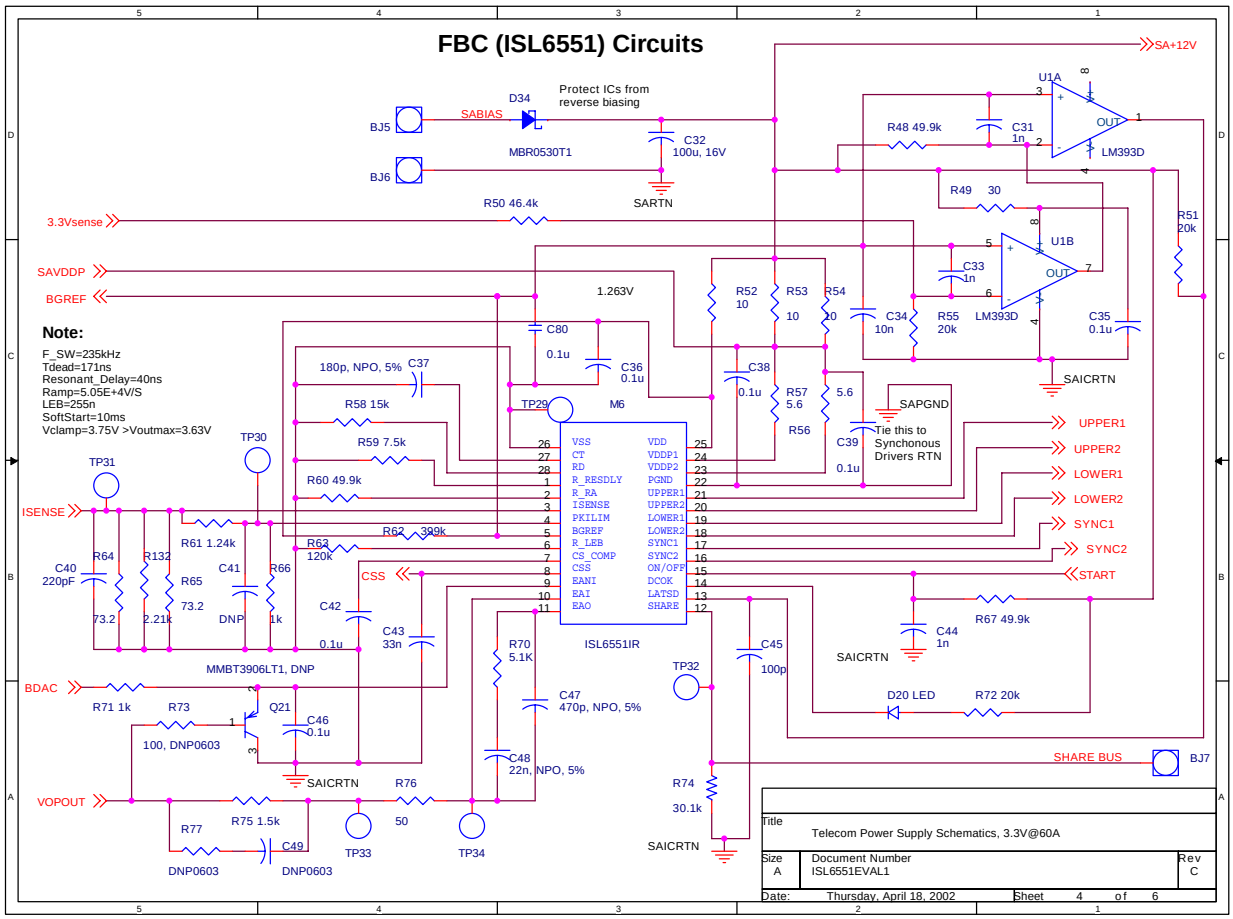
1. Block diagram of the converter in the evaluation board.
2. Evaluation board schematics (6 pages).
3. Evaluation board layout (12 pages).
4. Bill of Materials of the evaluation board (2 pages).
5. Preliminary specifications of the converter.

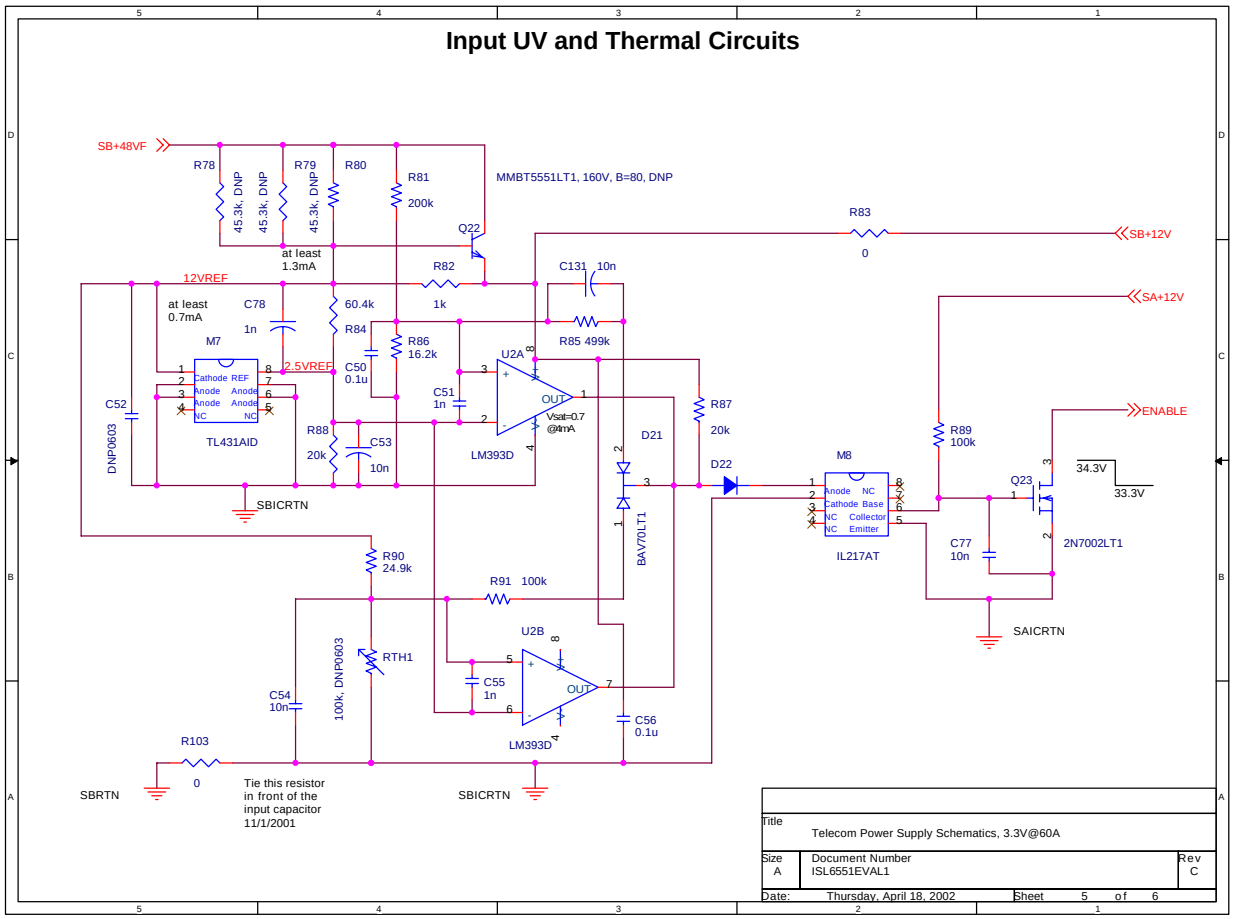


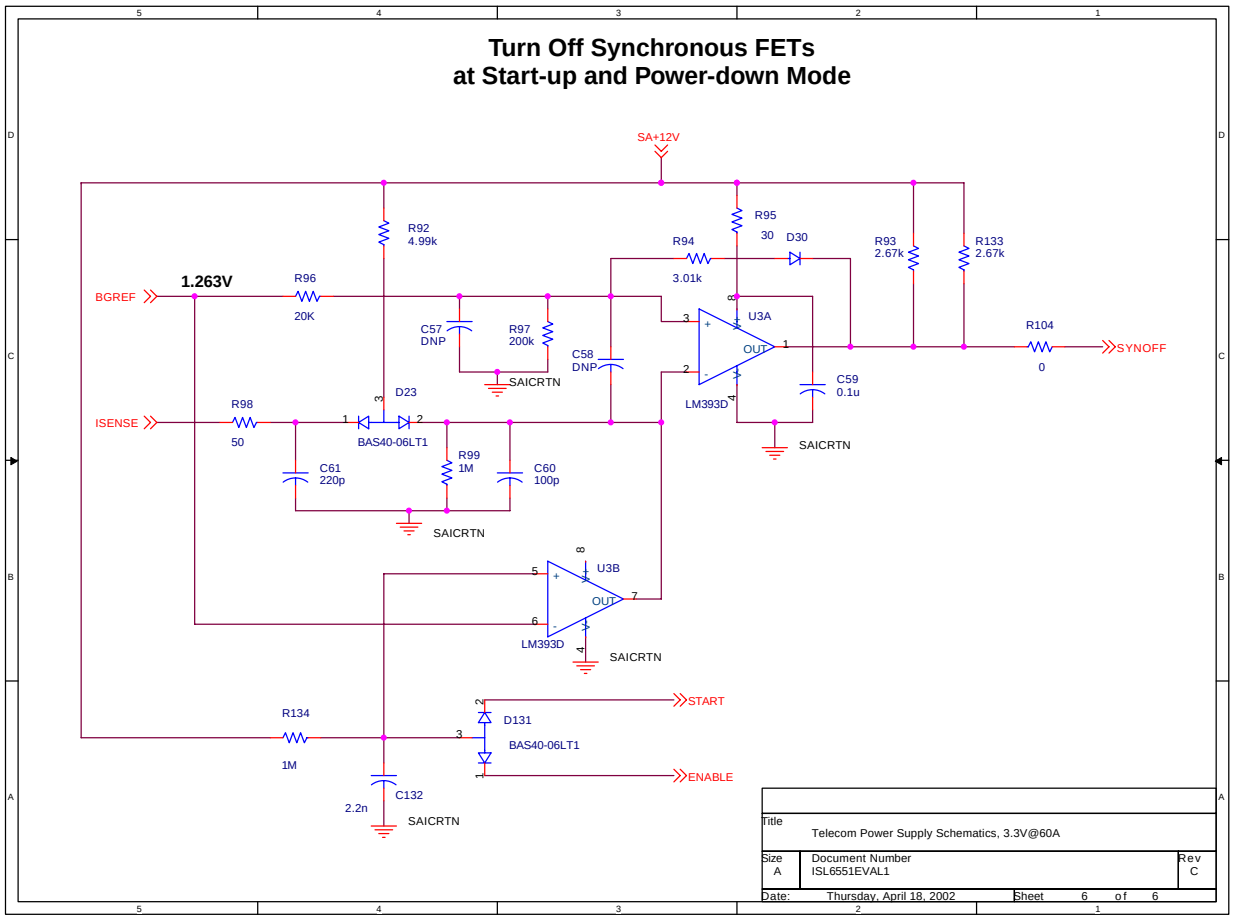




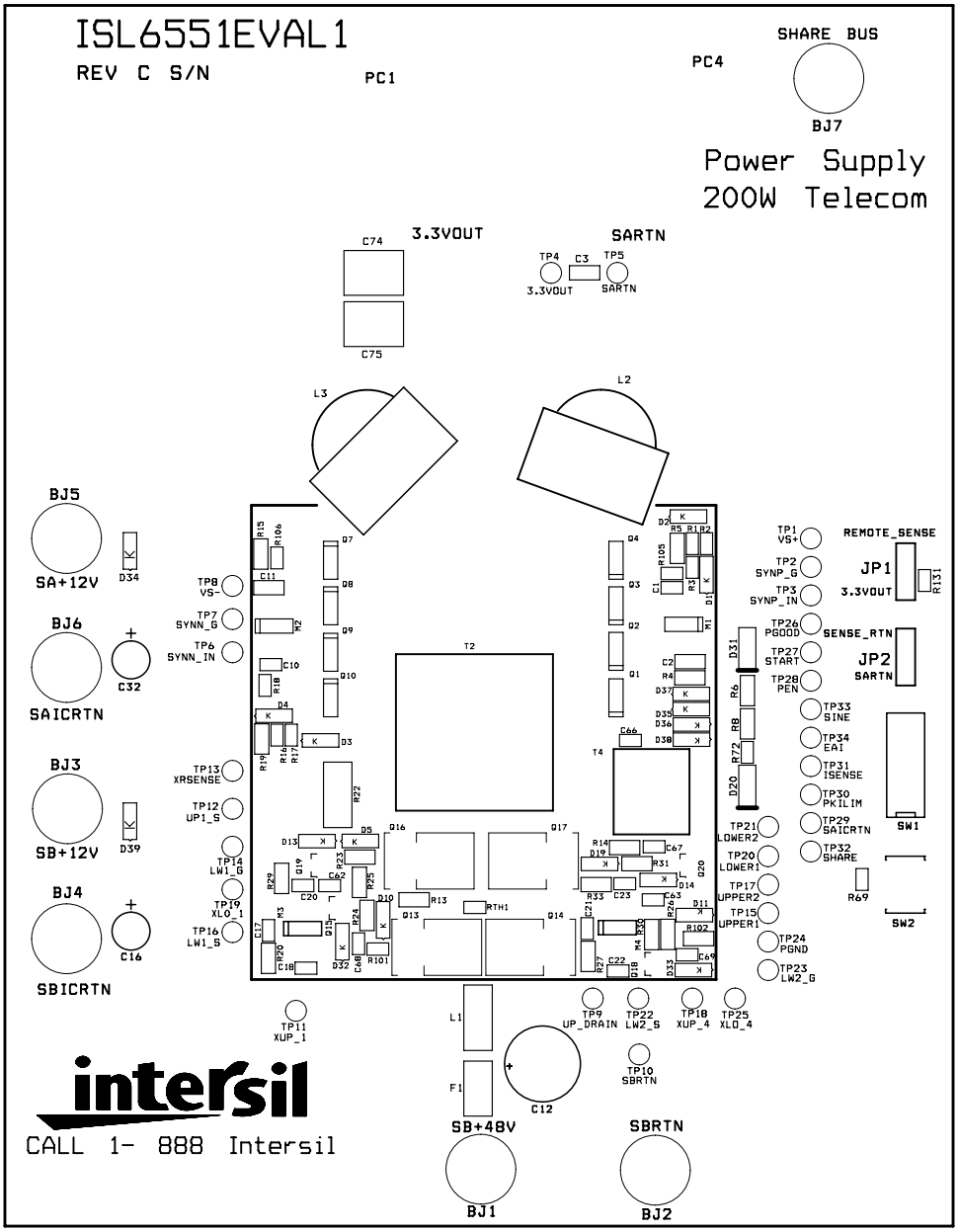




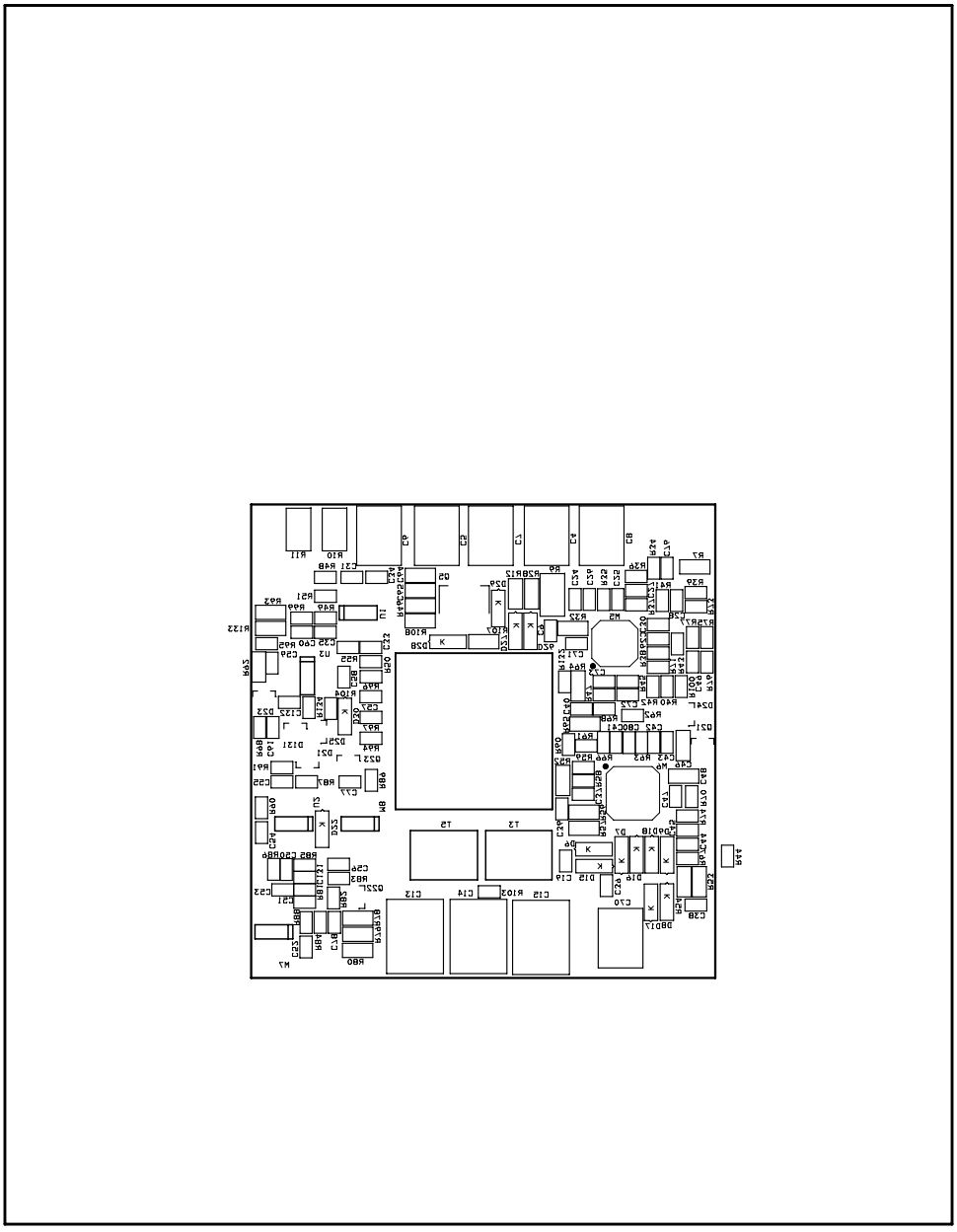




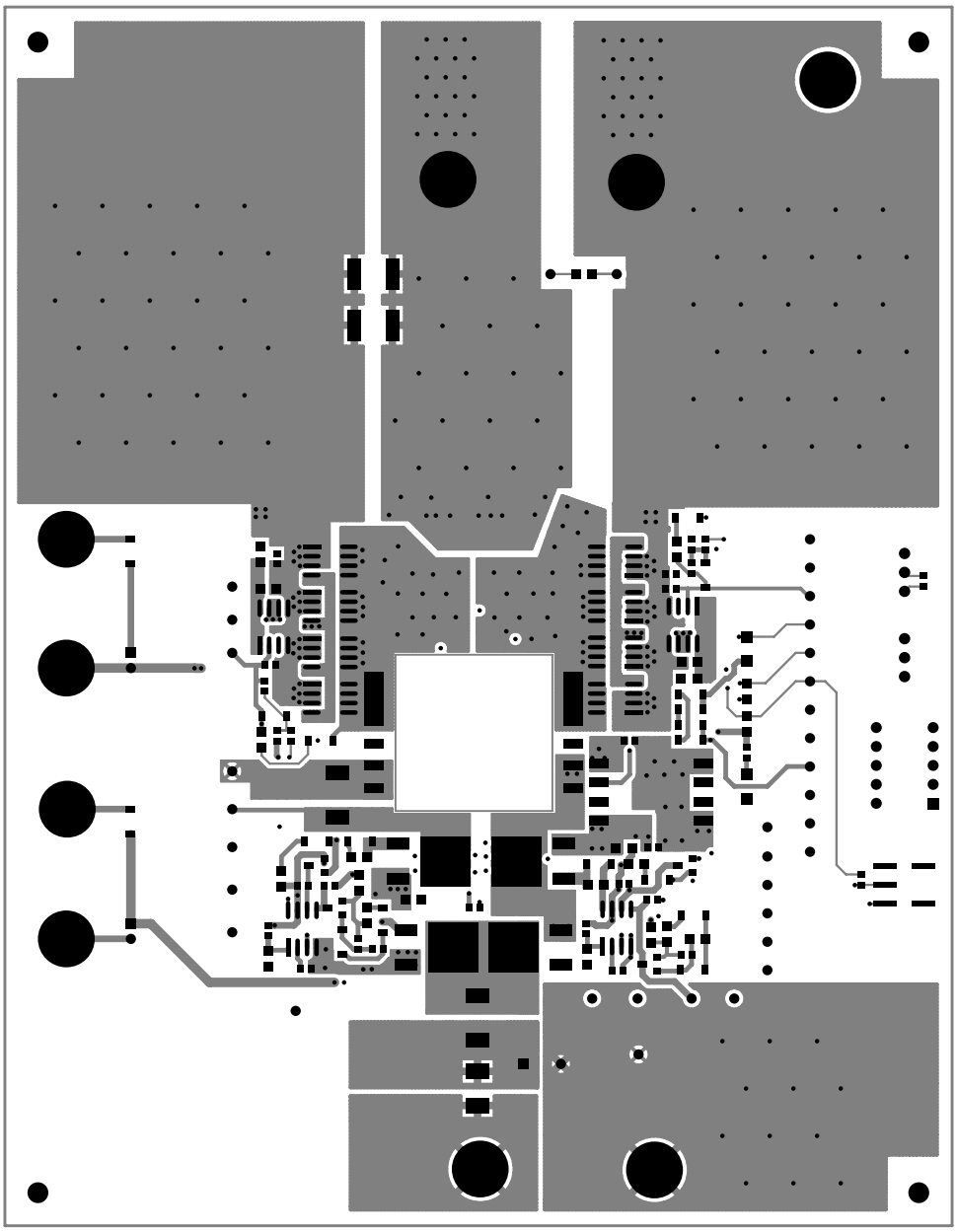
SILKSCREEN TOP



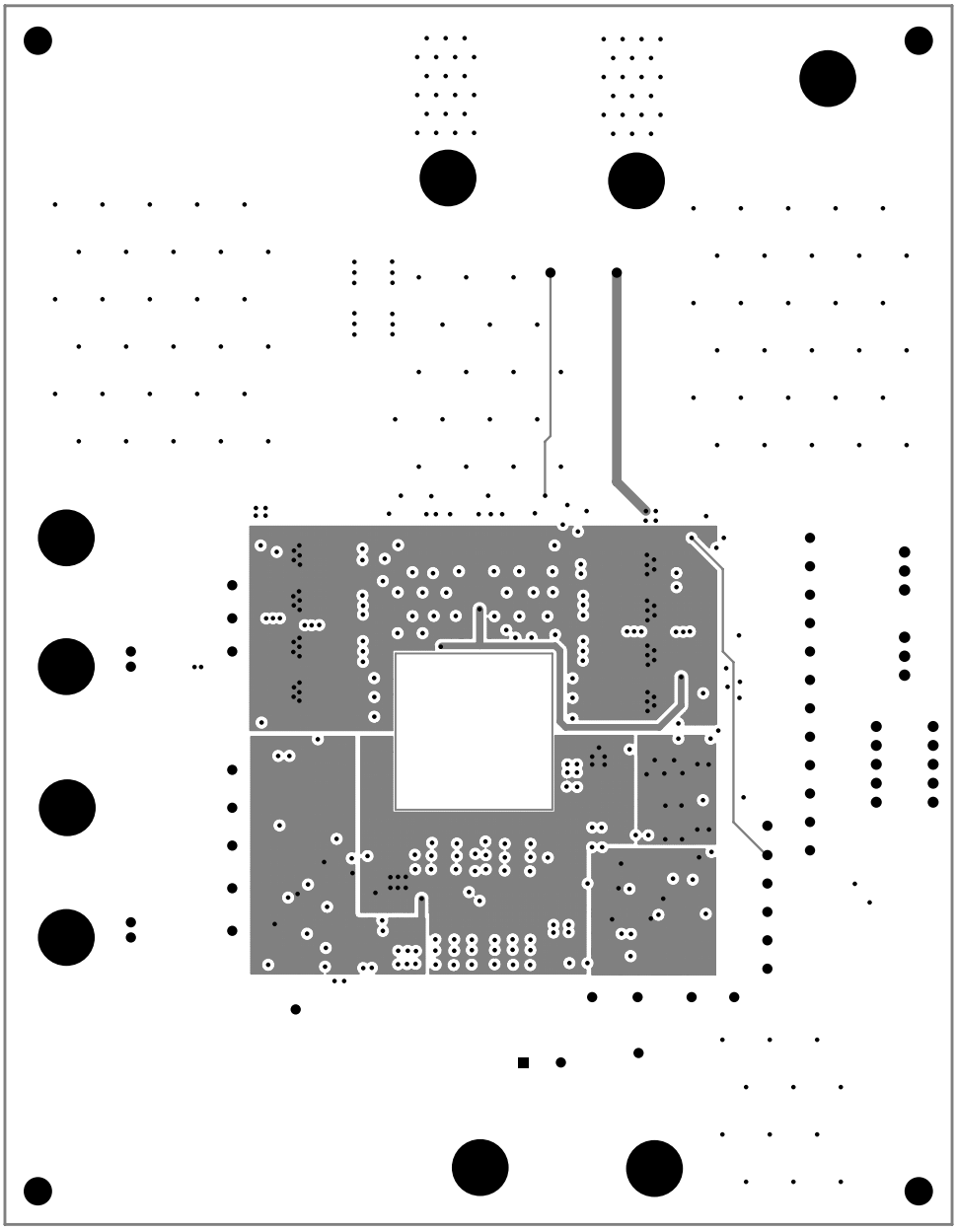
SILKSCREEN BOTTOM



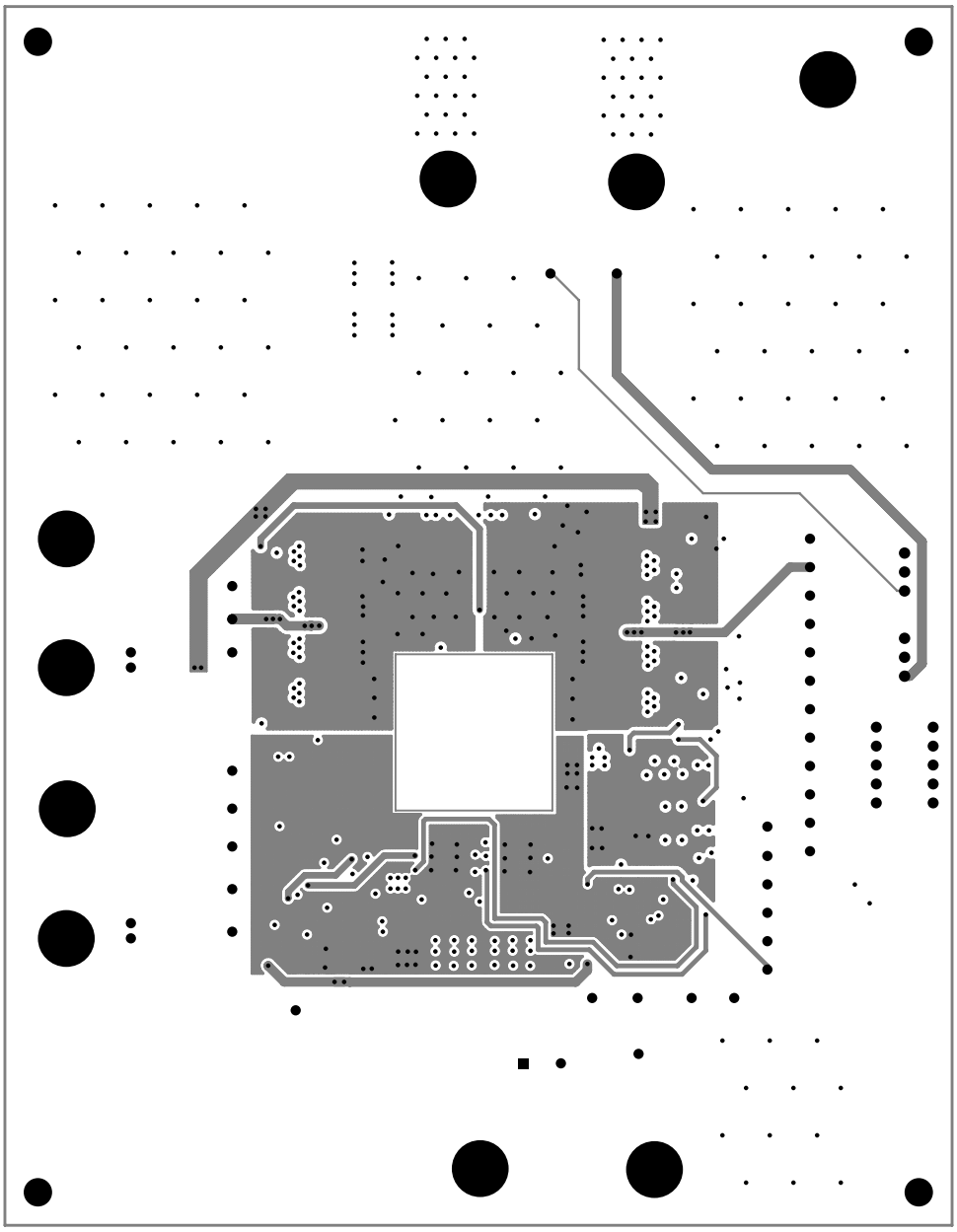
LAYER 1 TOP COPPER



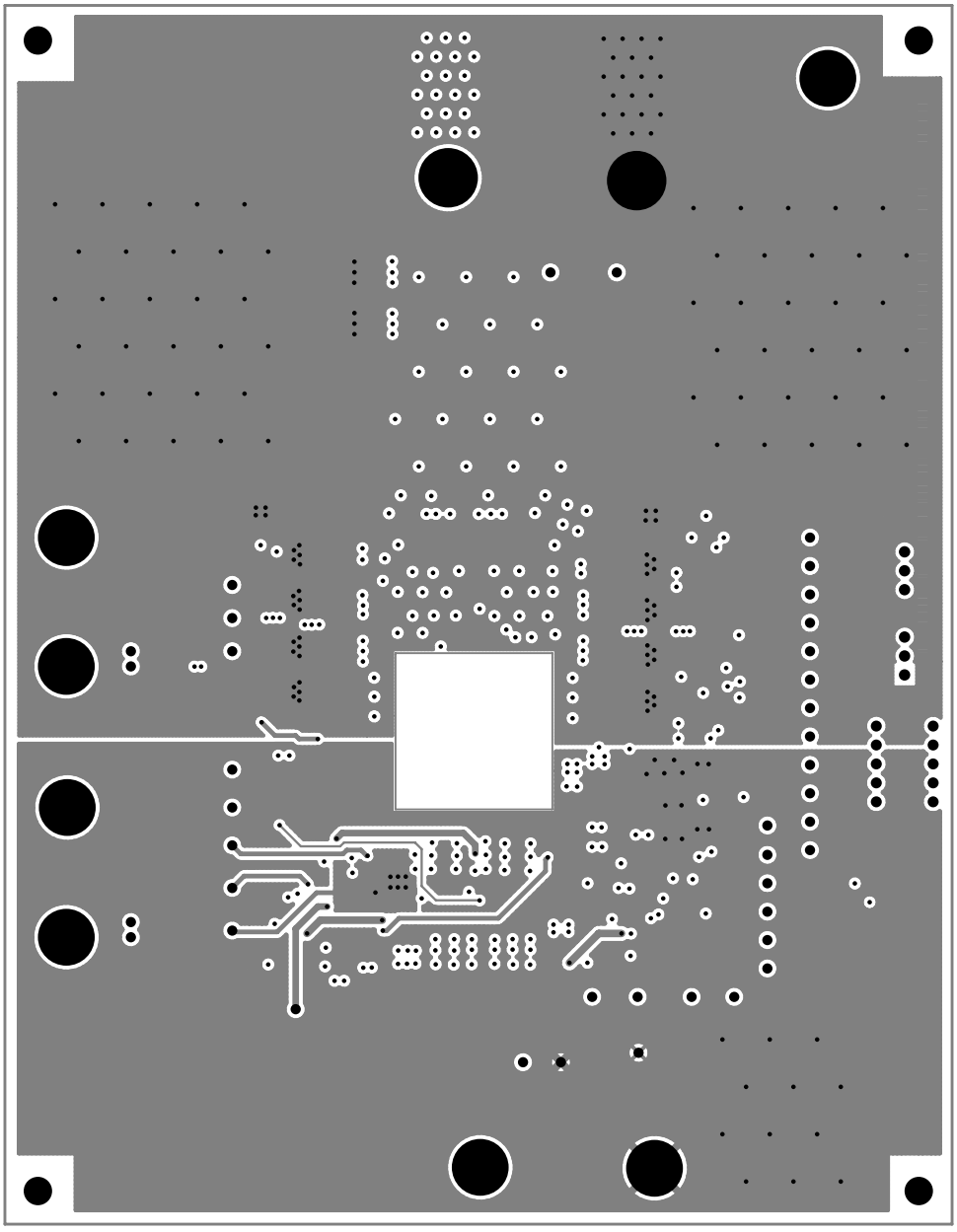
LAYER 2 INNER R1



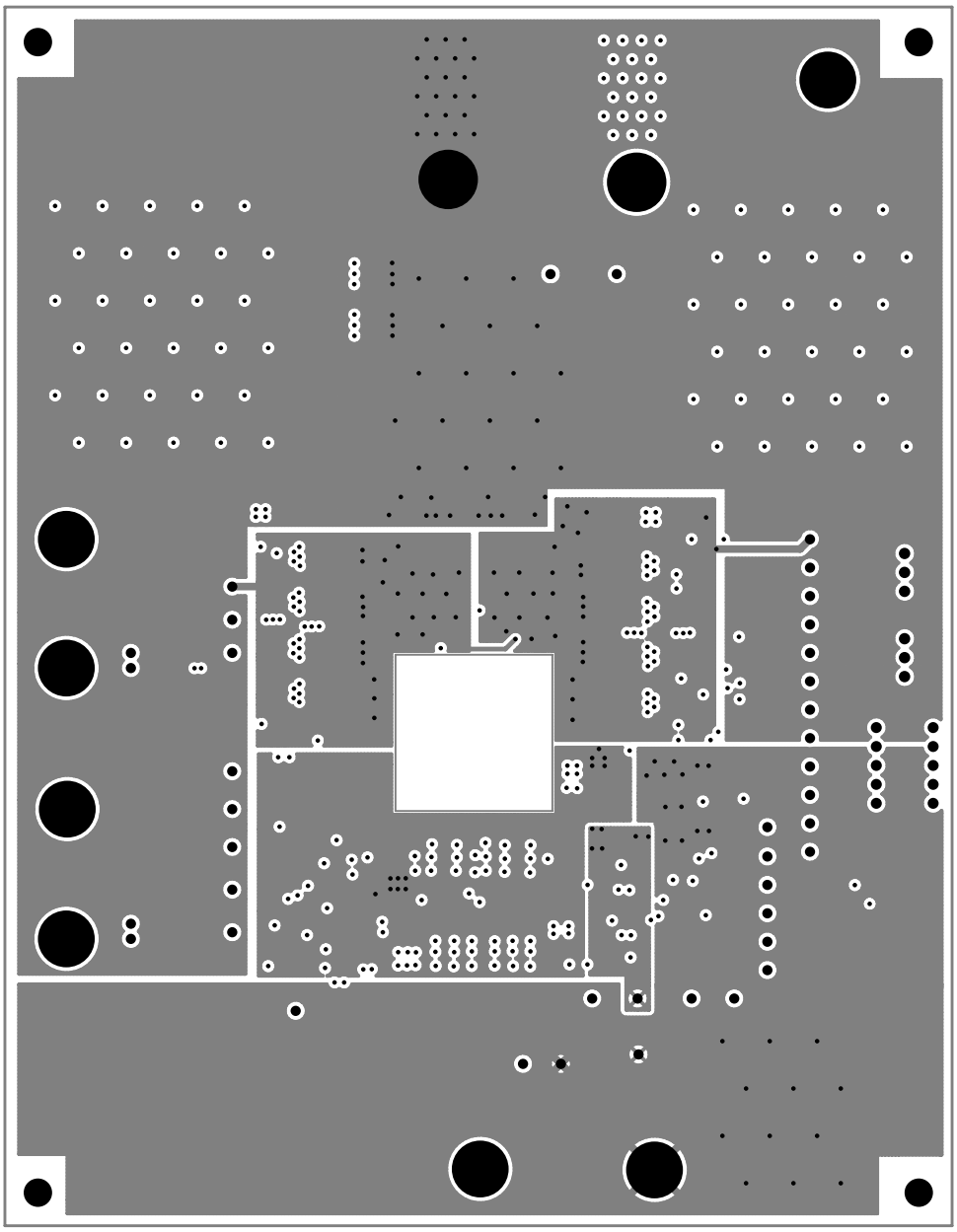
LAYER 3 INNER R2



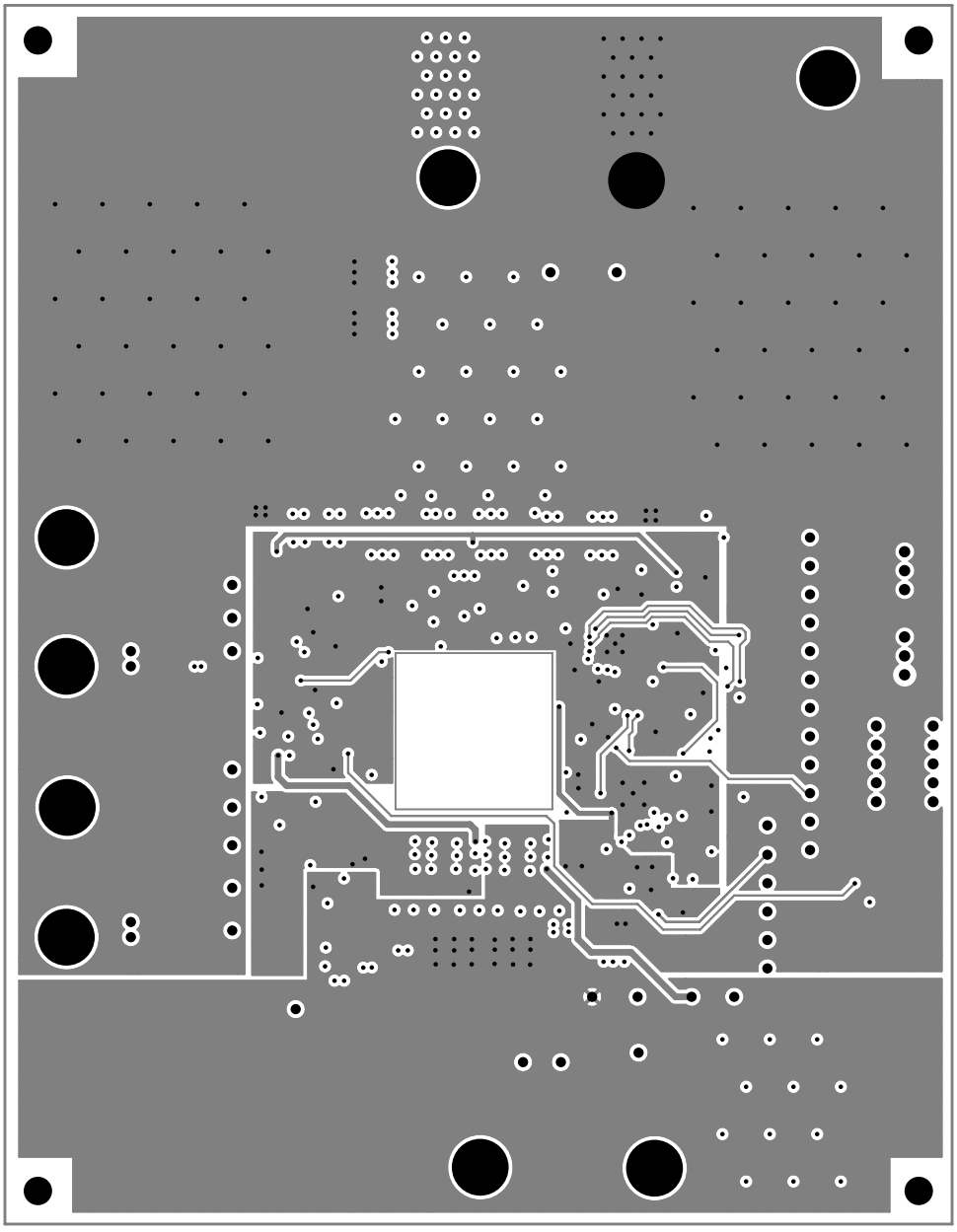
LAYER 4 GROUND PLANE



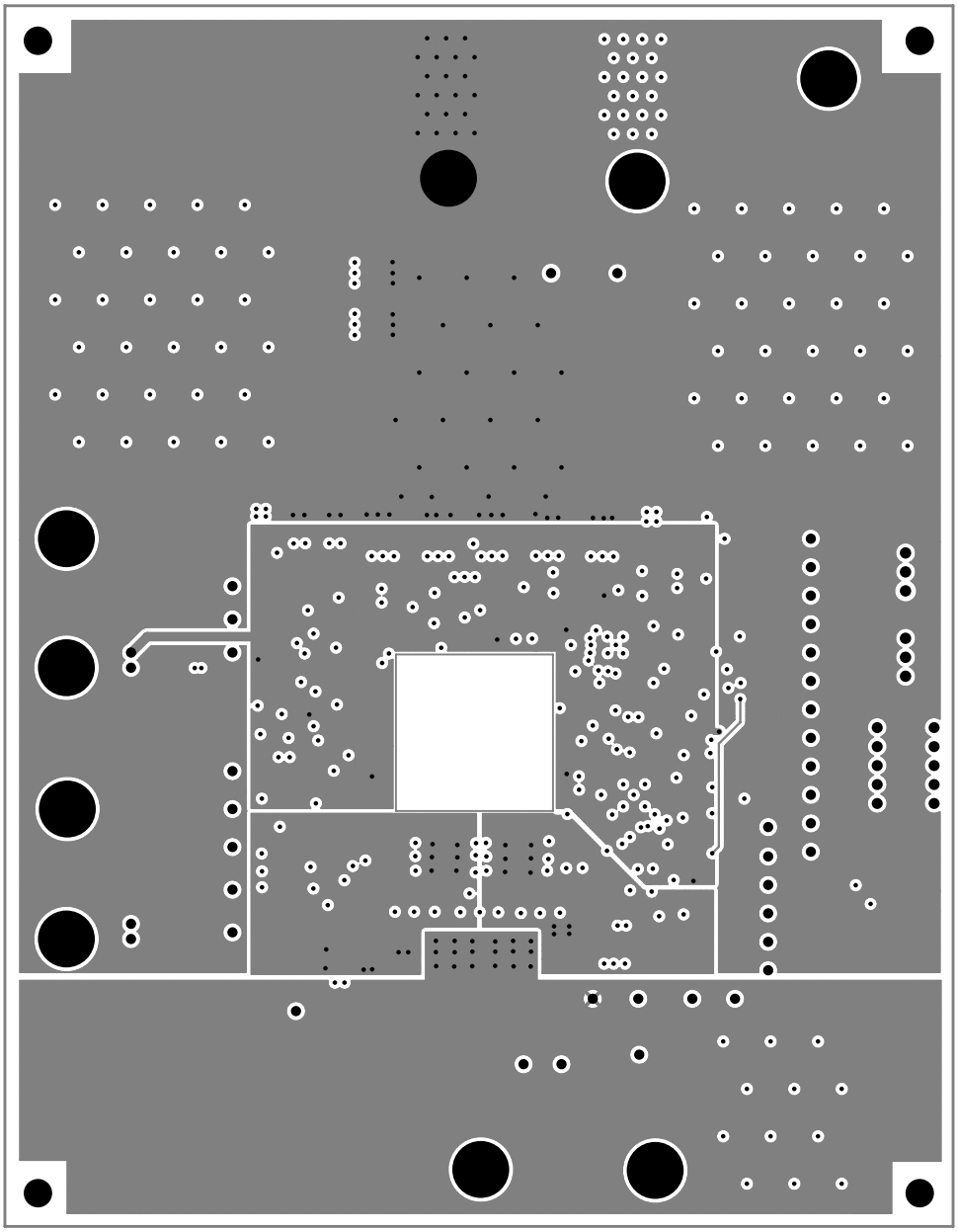
LAYER 5 POWER PLANE



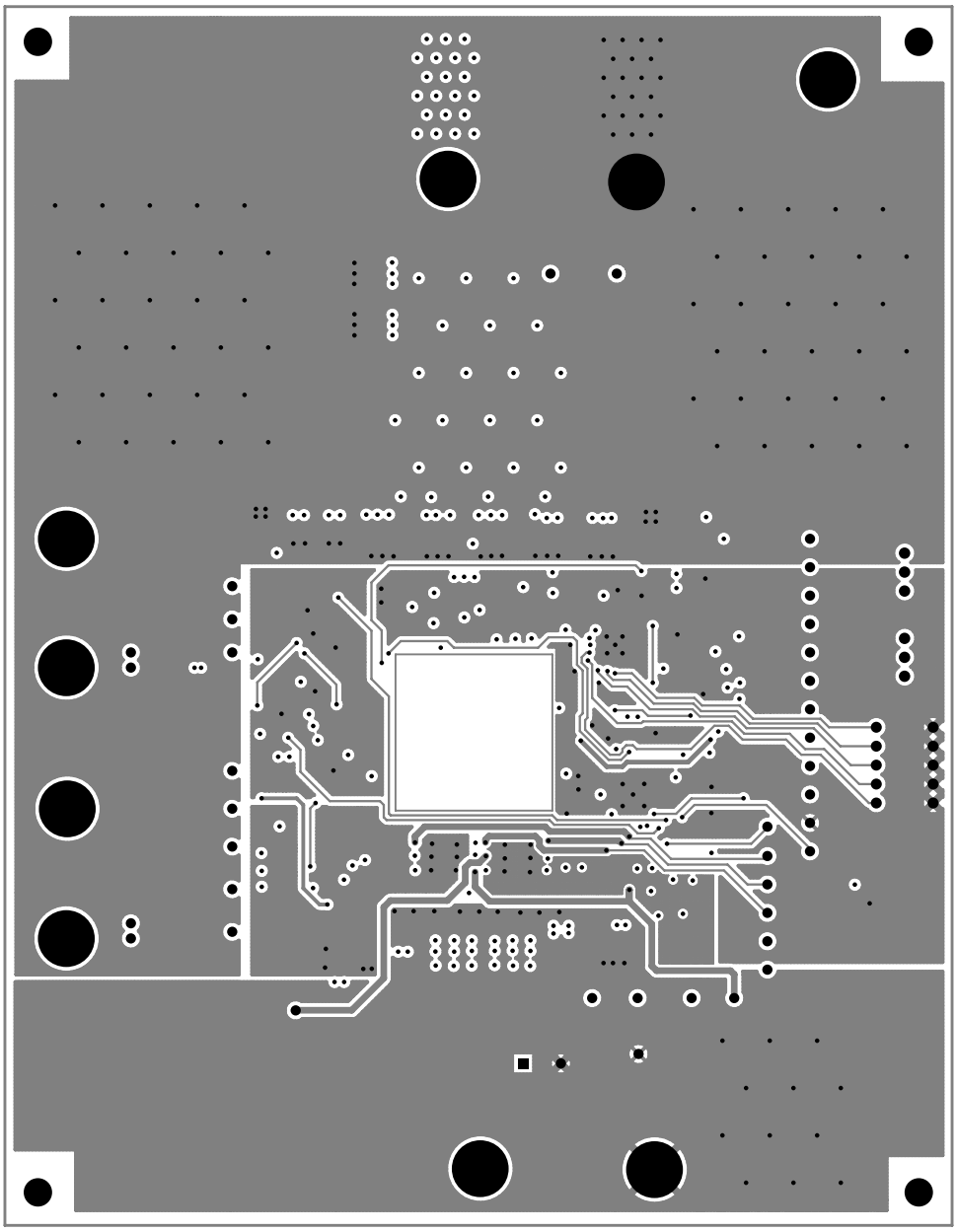
LAYER 6 GROUND PLANE 1



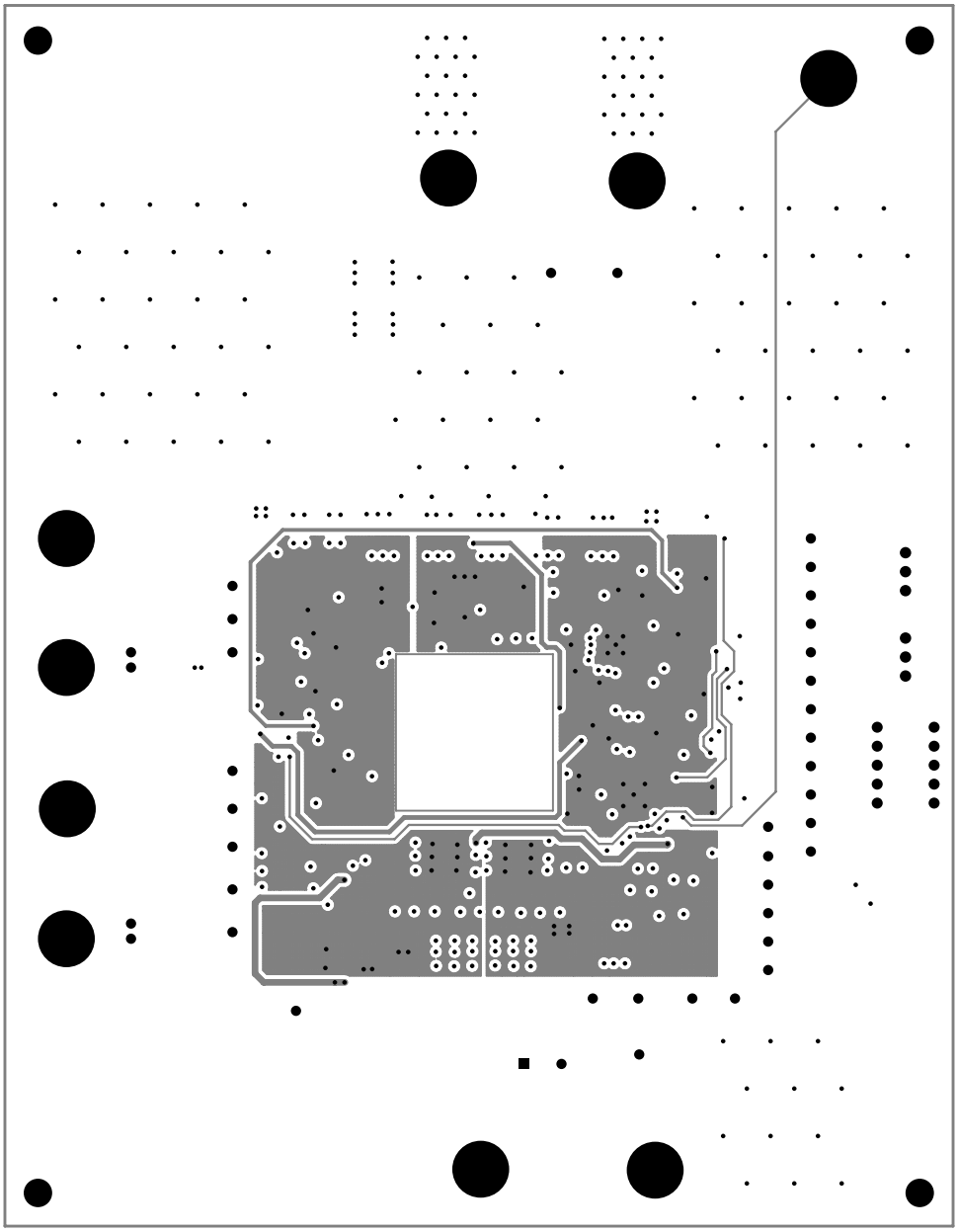
LAYER 7 POWER PLANE 1



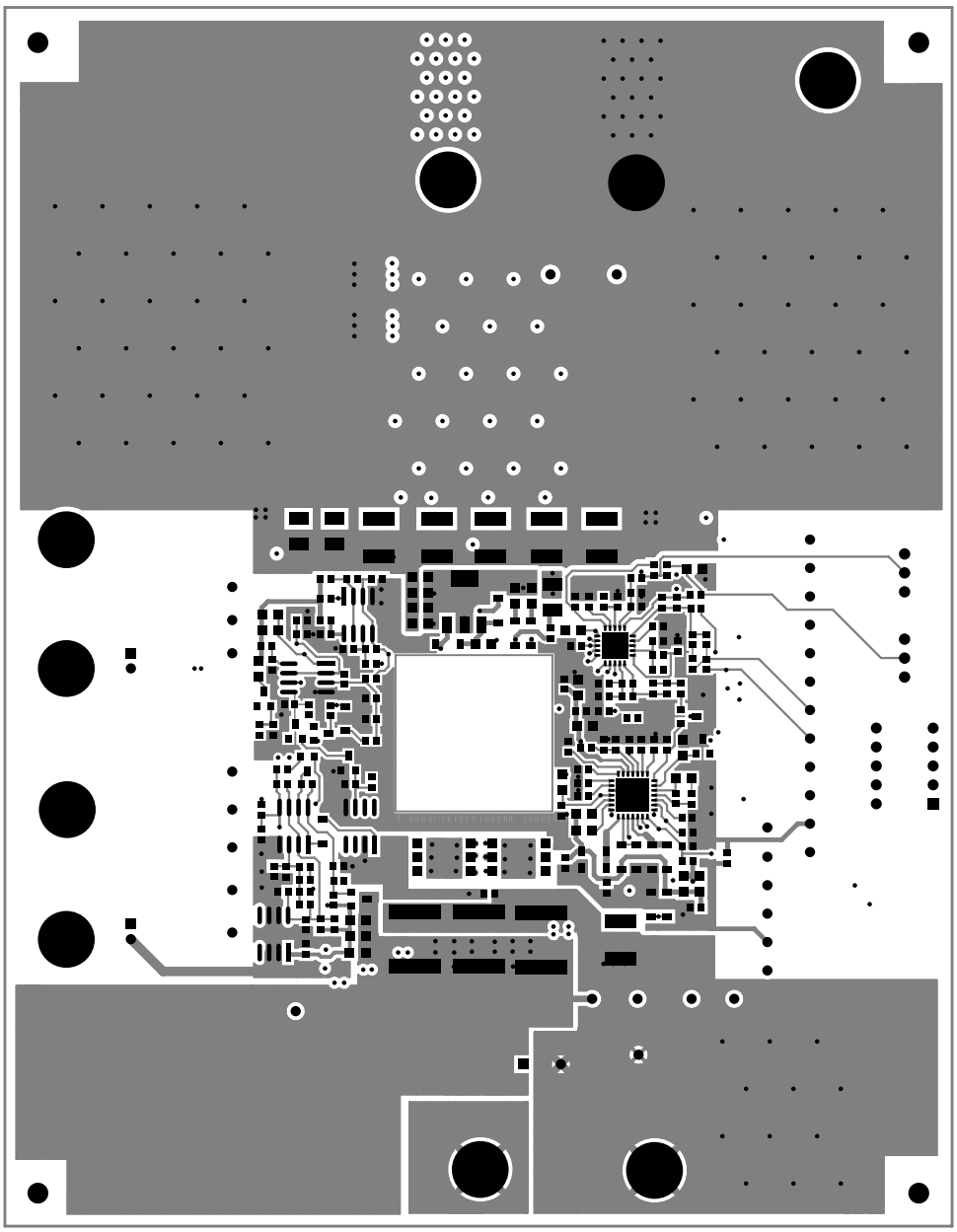
LAYER 8 INNER R3



LAYER 9 INNER R4



LAYER 10 BOTTOM COPPER



BILL OF MATERIALS (1/2)

Item	Quantity	Reference	Part	Footprint	Vendor	Vendor Part Number
1	1	BJ1	Red binding post	BINDING/POST	Johnson Components	111-0702-001
2	2	BJ4,BJ2	White binding post	BINDING/POST	Johnson Components	111-0701-001
3	1	BJ3	Yellow binding post	BINDING/POST	Johnson Components	111-0707-001
4	1	BJ5	Green binding post	BINDING/POST	Johnson Components	111-0704-001
5	1	BJ6	Black binding post	BINDING/POST	Johnson Components	111-0703-001
6	1	BJ7	Blue binding post	BINDING/POST	Johnson Components	111-0710-001
7	11	C1,C10,C20,C23,C29,C49, C52,C62,C63,C68,C69	DNP0603	SM/C_0603	Various	DNP
8	3	C2,C3,C11	1u, X7R, 25V	SM/C_0805	Various	Various
9	7	C4,C5,C6,C7,C8,C74,C75	100u, 6.3V	SM/L_2220	Taiyo Yuden	JMK550BJ107MM
10	1	C9	0.1u, 100V	SM/C_0805	DNP	DNP
11	1	C12	47u, 100V	CPCYL1/D.400/LS.200/.034	Panasonic	ECA-2AHG470
12	3	C13,C14,C15	1u, 100V	SM/ST2824	ITW Paktron	105K100S2824
13	2	C32,C16	100u, 16V	CYL/D.200/LS.079/.034	Panasonic	ECA-1CHG101
14	17	C17,C18,C19,C21,C22,C25, C26,C35,C36,C38,C39,C42, C50,C56,C59,C76,C80	0.1u, X7R, 25V	SM/C_0603	Various	Various
15	10	C24,C30,C34,C53,C54,C71, C72,C73,C77,C131	10n, X7R, 25V	SM/C_0603	Various	Various
16	2	C27,C28	10p, X7R, 25V	SM/C_0603	Various	Various
17	6	C31,C33,C44,C51,C55,C78	1n, X7R, 25V	SM/C_0603	Various	Various
18	1	C37	180p, NPO, 5%, 25V	SM/C_0603	Various	Various
19	1	C40	220p, X7R, 25V	SM/C_0603	Various	Various
20	3	C41,C57,C58	DNP0603	SM/C_0603	Various	Various
21	1	C43	33n, X7R, 25V	SM/C_0603	Various	Various
22	2	C60,C45	100p, X7R, 25V	SM/C_0603	Various	Various
23	1	C46	0.1u, X7R	SM/C_0805	Various	Various
24	1	C47	470p, NPO, 5%, 25V	SM/C_0603	Various	Various
25	1	C48	22n, X7R, 25V	SM/C_0805	Various	Various
26	1	C61	220p, X7R, 25V	SM/C_0603	Various	Various
27	2	C64,C65	5.6n, X7R, 50V	SM/C_0805	Various	5.6n, X7R, 50V
28	2	C67,C66	3900pF, X7R, 25V	SM/C_0603	Various	Various
29	1	C70	2.2N, X7R, 630V, 1206	SM/L_2220	TDK	C3216X7R2J222M
30	1	C132	2.2n, X7R, 25V	SM/C_0603	Various	Various
31	16	D1,D2,D3,D4,D5,D10,D11, D13,D14,D19,D22,D26,D27, D28,D29,D30	MMSD914T1	SOD123	On Semiconductor	MMSD914T1
32	14	D6,D7,D8,D9,D15,D16,D17, D18,D34,D35,D36,D37,D38, D39	MBR0530T1	SOD123	On Semiconductor	MBR0530T1
33	2	D20,D31	LED	DL-35	Digi-Key	160-1173-2-ND
34	2	D21,D24	BAV70LT1	SM/SOT23_123	On Semiconductor	BAV70LT1
35	3	D23,D25,D131	BAS40-06LT1	SM/SOT23_123	On Semiconductor	BAS40-06LT1
36	2	D32,D33	DNP	SOD123	On Semiconductor	MMSD914T1
37	1	F1	R451010	SM/C_1812	LittleFuse	R451010
38	2	JP1,JP2	3-Pin Connector	TP\3P	Digi-Key	S1012-03-ND
39	2	Jumpers	Jumpers for JP1 &JP2		Various	Jumpers for JP1 &JP2
40	1	L1	0	SM/R_2512	Various	Various
41	2	L2,L3	0.8uH	IND/DTPC1000-0002	DT Magnetics	015138 Rev B
42	2	M2,M1	MIC4421BM	SOG.050/8/WG.244/L.200	Micrel Semiconductor	MIC4421BM
43	2	M3,M4	HIP2100IB	SOG.050/8/WG.244/L.200	Intersil	HIP2100IB
44	1	M5	ISL6550CIR	MLFP.65M/20/5X5	Intersil	ISL6550CIR
45	1	M6	ISL6551IR	MLFP.65M/28/6X6	Intersil	ICL6551IR
46	1	M7	TL431AID	SOG.050/8/WG.244/L.200	Texas Instrument	TL431AID
47	1	M8	IL217AT	SOG.050/8/WG.244/L.200	Infineon	IL217AT
48	2	PC1, PC4	KPA8CTP	BINDING/POST_2_REV2	Burndy	KPA8CTP
49	8	Q1,Q2,Q3,Q4,Q7,Q8,Q9,Q10	Si4842DY	SOG.050/8/WG.244/L.200	Vishay Siliconix	Si4842DY
50	1	Q5	MMJT9410	SM/SOT223_BCEC	On Semiconductor	MMJT9410
51	4	Q13,Q14,Q16,Q17	SUD40N10-25	TO252AA-DPAK	Vishay Siliconix	SUD40N10-25
52	5	Q15,Q18,Q19,Q20,Q23	2N7002LT1	SM/SOT23_123	On Semiconductor	2N7002LT1
53	1	Q21	MMBT3906LT1	SM/SOT23_123	On Semiconductor	DNP
54	1	Q22	MMBT5551LT1	SM/SOT23_123	On Semiconductor	DNP
55	1	RTH1	100k, DNP0603	SM/R_0603	Western Electronic Components Corp.	WSTL06104R
56	3	R1,R16,R34	10	SM/R_0603	Various	1%
57	1	R2	DNP603	SM/R_0603	Various	DNP
58	2	R3,R18	750	SM/R_0603	Various	1%
59	3	R4,R15,R107	2	SM/R_0805	Various	1%
60	2	R19,R5	2.43k	SM/R_0805	Various	1%

BILL OF MATERIALS (2/2)

Item	Quantity	Reference	Part	Footprint	Vendor	Vendor Part Number
61	8	R6,R7,R12,R13,R14,R25, R28,R30	0	SM/R_0805	Various	1%
62	4	R8,R48,R60,R67	49.9k	SM/R_0603	Various	1%
63	1	R9	DNP	SM/R_1210	Various	1%
64	1	R10	100	SM/R_1210	Various	1%
65	1	R11	DNP1210	SM/R_1210	Various	DNP
66	2	R77,R17	DNP0603	SM/R_0603	Various	DNP
67	4	R20,R27,R56,R57	5.6	SM/R_0805	Various	1%
68	1	R22	0	SM/R_2512	Various	Various
69	4	R23,R24,R26,R33	36.5	SM/R_0805	Various	1%
70	5	R29,R31,R52,R53,R54	10	SM/R_0805	Various	1%
71	7	R32,R51,R55,R72,R87,R88, R96	20k	SM/R_0603	Various	1%
72	3	R35,R49,R95	30	SM/R_0603	Various	1%
73	6	R36,R37,R38,R39,R41,R45	10k	SM/R_0603	Various	1%
74	1	R40	28.7k	SM/R_0603	Various	1%
75	2	R42,R47	26.7k	SM/R_0603	Various	1%
76	1	R43	110k	SM/R_0603	Various	1%
77	1	R44	DNP0603	SM/R_0603	Various	DNP
78	2	R108,R46	DNP0805	SM/R_0805	Various	DNP
79	1	R50	46.4k	SM/R_0603	Various	1%
80	1	R58	15k	SM/R_0603	Various	1%
81	1	R59	7.5k	SM/R_0603	Various	1%
82	1	R61	1.24k	SM/R_0603	Various	1%
83	1	R62	399k	SM/R_0603	Various	1%
84	1	R63	120k	SM/R_0603	Various	1%
85	2	R65,R64	73.2	SM/R_0805	Various	1%
86	3	R66,R71,R82	1k	SM/R_0603	Various	1%
87	1	R68	3.65k	SM/R_0603	Various	1%
88	1	R69	100	SM/R_0603	Various	1%
89	1	R70	5.1K	SM/R_0603	Various	1%
90	1	R73	100	SM/R_0603	Various	DNP
91	1	R74	30.1k	SM/R_0603	Various	1%
92	1	R75	1.5k	SM/R_0603	Various	1%
93	3	R76,R98,R131	50	SM/R_0603	Various	1%
94	3	R78,R79,R80	45.3k	SM/R_0805	Various	DNP
95	2	R97,R81	200k	SM/R_0603	Various	1%
96	7	R83,R101,R102,R103,R104, R105,R106	0	SM/R_0603	Various	1%
97	1	R84	60.4k	SM/R_0603	Various	1%
98	1	R85	499k	SM/R_0603	Various	1%
99	1	R86	16.2k	SM/R_0603	Various	1%
100	2	R89,R91	100k	SM/R_0603	Various	1%
101	1	R90	24.9k	SM/R_0603	Various	1%
102	1	R92	4.99k	SM/R_0805	Various	1%
103	2	R133,R93	2.67k	SM/R_0805	Various	1%
104	1	R94	3.01k	SM/R_0603	Various	1%
105	2	R99,R134	1M	SM/R_0603	Various	1%
106	1	R100	1.2k	SM/R_0603	Various	1%
107	1	R132	2.21k	SM/R_0603	Various	1%
108	1	SW1	5-Bit DAC Switch	DIPSW.100/10/W.300/L.550	CTS	208-5
109	1	SW2	ON/OFF Switch	SWITCH_DPST	C&K Components	GT11MSCKE
110	34	TP1,TP2,TP3,TP4,TP5,TP6, TP7,TP8,TP9,TP10,TP11, TP12,TP13,TP14,TP15,TP16, TP17,TP18,TP19,TP20,TP21, TP22,TP23,TP24,TP25,TP26, TP27,TP28,TP29,TP30,TP31, TP32,TP33,TP34	Test Point	TP	Keystone	5002
111	1	T2	Main Transformer	IND/DTPC1000-0001	DT Magnetics	010107 Rev C
112	2	T5,T3	Pulse Transformer	DT_X_330X260_REV11	DT Magnetics	UGDT125100
113	1	T4	Current Sense Transformer	DT_XC_640X400_REV3	DT Magnetics	010109 Rev A
114	3	U1,U2,U3	LM393D	SOG.050/8/WG.244/L.200	On Semiconductor	LM393D
115	1	PCB board	10 layers, 4 oz Copper, Buried Vias		Various	10 layers, 4 oz Copper

CONVERTER PRELIMINARY SPECIFICATIONS

Features

- Ultra-high efficiency, 88% at full load
- High power density, 68W/in³ (3.3V@60A)
- Wide input voltage range 36V - 75V
- Fixed frequency switching
- Fast dynamic response, 250us, +/-150mVpeak
- Remote On/Off
- TTL-compatible 5-bit programmable output
- Ouptut under-voltage shutdown with 70mS delay
- Low output ripple, 35mVp-p Typ.
- Low noise ZVS architeture
- Parallel operation with load sharing
- Remote Sense, 0.5V
- Short-Circuit Protection
- Input under-voltage lockout
- Dual output over-voltage protection
- DNP primary thermal protection

Input Specifications (TA=Overall Operating Temperature, unless otherwise specified.)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Voltage		36	48	75	V
Turn-on Input Voltage			34.3	35.7	V
Turn-off Input Voltage		31.9	33.3		V
Operating Bias Voltage			12		V

Output Specifications (TA=Overall Operating Temperature, unless otherwise specified.)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	Overall Operating Range	3.2	3.3	3.4	V
Output Adjust Range		2.64	-	3.63	V
Remote-Sense Compensation	Cannot exceed maximum duty cycle	-	-	0.5	V
Output Current		0.5		60	A
Local Over-Voltage Shutdown			108.33		% Vo
Master Over-Voltage Shutdown		4.07	4.19	4.33	V
Over-Current Trip Point	TA=25°C, ~ 400LFM	60.00	65.00	70.00	A
Efficiency at Full Load	Vin=48V, TA=25°C, ~400LFM		88		%
Line Regulation				0.1	% Vo
Load Regulation				0.2	% Vo
Output Ripple Voltage	< 20 MHz BW, Io=Iomax		35	70	mVp-p
Current Share	60A (Slave relative to Master)	-	5	-	%
Output Rise Time			12	-	mS

Dynamic Response (TA=Overall Operating Temperature, unless otherwise specified.)

Parameter	Conditions	Min.	Typ.	Max.	Unit
25% load step up	dI/dt=1A/us		-150		mV
Recovery Time	Vo < 10% of peak deviation		250		us
25% load step down	dI/dt=1A/us		+150		mV
Recovery Time	Vo < 10% of peak deviation		250		us

Miscellaneous Specifications (TA=Overall Operating Temperature, unless otherwise specified.)

Parameter	Conditions	Min.	Typ.	Max.	Unit
PGOOD Low	Open Collector, Ipgood=5mA	0		0.4	V
PGOOD High		2		12	V
PGOOD sink current				5	mA
Remote On/Off Low				0.8	V
Remote On/Off High		2			V
Ambient Temperature Range	Power derating is required	0		85	°C
Storage Temperature		-40		150	°C
Switching Frequency			235		kHz
Real Estate for Components		Double sides, 2.50" x 2.45" x 2 x 70% = 8.58 in²			