

LM3370 Evaluation Board

National Semiconductor
Application Note 1428
Anne Lu
January 9, 2008



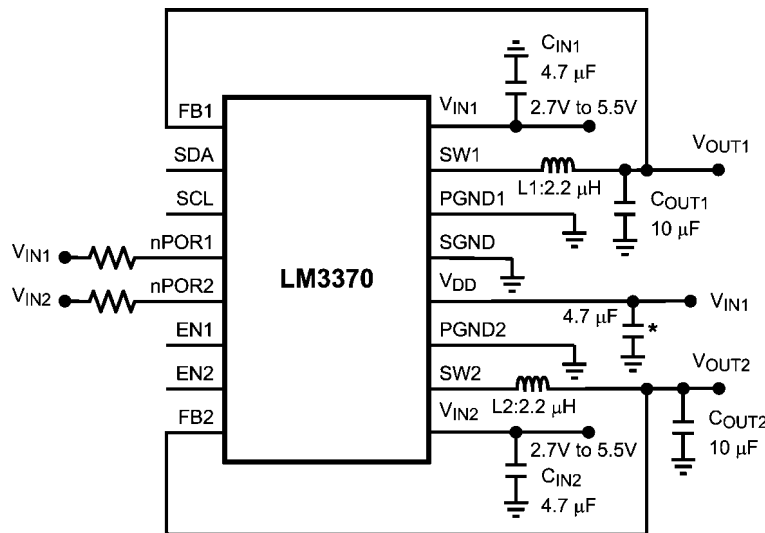
Introduction

The LM3370 evaluation board is a working demonstration of a DUAL step down DC-DC converter. This application note contains information about the evaluation board. For more details and electrical characteristic on the dual buck converter operation, please refer to the LM3370 datasheet.

General Description

The LM3370 is a dual step-down DC-DC converter optimized for powering ultra-low voltage circuits from a single Li-Ion cell or 3 cell NiMH/NiCd batteries. Automatic intelligent switching between PWM low-noise and PFM low current mode offers improved system efficiency. The I²C compatible offers dynamic controls of the output voltages, Auto PFM/PWM mode

Typical Application



* Optional Capacitor

FIGURE 1. Typical Application Circuit

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Operating Information

The LM3370SD evaluation board is pre-programmed to 1.2V at V_{OUT1} and 3.3V at V_{OUT2} for evaluation purpose (no additional interface hardware is needed). If different default output option is desired, the same evaluation board can be used by demount the existing device and replace with new voltage option (voltage option can be order from National's website).

The device comes with the following default setting: Auto PFM and PWM transition mode when the I²C compatible interface is not enabled. For other settings, I²C compatible interface must be used to enable all other functions. Registers information are listed on page 4 for I²C compatible interface.

Powering Up The Evaluation Board

- Apply a voltage at the "Vin_EXT" pin only (not Vin_IO).

selection and other enabling enchantment features such as power-on-reset (nPOR) and spread spectrum.

Operating Conditions

- V_{IN} range: 2.7V ≤ V_{IN} ≤ 5.5V
- Recommended load current: 0 to 600mA

I²C Compatible Interface

- V_{OUT1} (1V to 2V at 50mV step increment)
- V_{OUT2} (1.8V to 3.3V at 100mV steps increment).

Package

- TLA20CWA micro SMD, (3.0mm x 2.0mm x 0.6mm)
- LLP16 non-pullback, (4mm x 5mm x 0.8mm)

- All logic pins are tied to "Vin" on the evaluation board
- Do not power the "Vin_IO" pin unless powering the logic pins via an external source. (Jumper at Vin_IO must be removed.)
- V_{DD} pin is tied to V_{IN1} & V_{IN2} on the evaluation board, no additional connection required. (For any reason if V_{DD} is not directly tied to V_{IN}, V_{DD} needs to be equal or greater than the two inputs (V_{IN1} or V_{IN2}) for proper operation.)

I²C Interface Ready

If interface capability is available via I²C compatible, the SDA & SCL test pins of the evaluation board are brought out for such function. The SDA & SCL pins of the evaluation board are connected to 2 kΩ resistors and pulled up to V_{IN} pin.

Package Marking Information

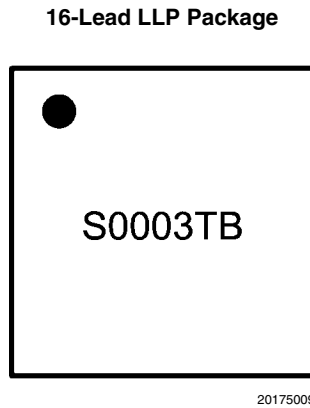


FIGURE 1. Top Marking

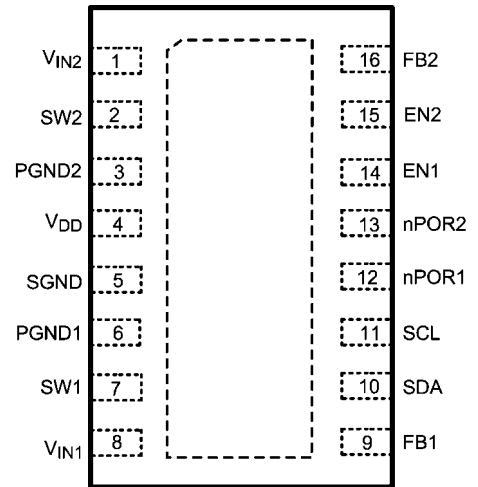
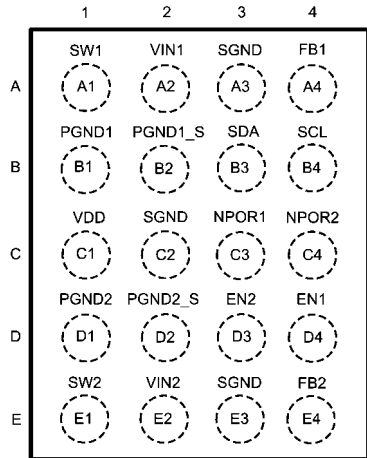


FIGURE 2. Top View

Pin Descriptions (LLP)

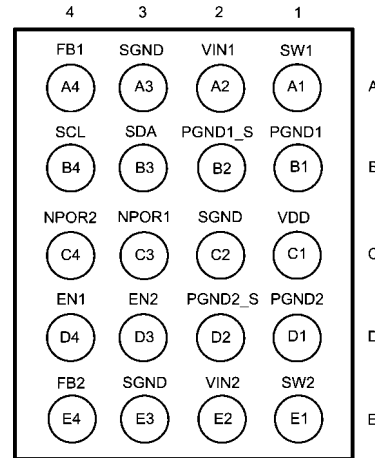
1	V_{IN2}	Power supply voltage input to PFET and NFET switches for Buck2
2	SW2	Buck 2 Switch pin
3	PGND2	Buck 2 Power Ground
4	V_{DD}	Signal supply voltage input, V_{DD} must be equal or greater of the two inputs (V_{IN1} or V_{IN2})
5	SGND	Signal GND
6	PGND1	Buck 1 Power Ground
7	SW1	Buck 1 Switch pin
8	V_{IN1}	Power supply voltage input to PFET and NFET switches for Buck1
9	FB1	Analog feedback input for Buck 1
10	SDA	I ² C Compatible Data, a 2 k Ω pull up resistor is required
11	SCL	I ² C Compatible Data, a 2 k Ω pull up resistor is required
12	nPOR1	Power ON Reset for Buck 1, Open drain output low when Buck 2 output is 92% of target output. A 100 k Ω pull up resistor is required
13	nPOR2	Power ON Reset for Buck 2, Open drain output low when Buck 2 output is 92% of target output. A 100 k Ω pull up resistor is required
14	EN1	Buck 1 Enable
15	EN2	Buck 2 Enable
16	FB2	Analog feedback input for Buck 2

Package Marking Information (micro SMD)



Top View

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Bottom View

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Pin Descriptions (micro SMD)

Pin #	Name	Description
A1	SW1	Buck 1 Switch Pin
A2	V_{IN1}	Power supply voltage input to PFET and NFET switches for Buck 1
A3	SGND	Signal GND
A4	FB1	Analog Feedback Input for Buck 1
B1	PGND1	Buck 1 Power Ground
B2	PGND1_S	Buck 1 Power Ground Sense
B3	SDA	I ² C Compatible Data, a 2 k Ω pull up resistor is required
B4	SCL	I ² C Compatible Clock, a 2 k Ω pull up resistor is required
C1	V_{DD}	Signal supply voltage input, V_{DD} must be equal or greater of the two inputs (V_{IN1} & V_{IN2})
C2	SGND	Signal GND
C3	nPOR1	Power ON Reset for Buck 1, Open drain output Low when Buck 1 output is 92% of target output. A 100 k Ω pull up resistor is required
C4	nPOR2	Power ON Reset for Buck 2, Open drain output Low when Buck 2 output is 92% of target output. A 100 k Ω pull up resistor is required
D1	PGND2	Buck 2 Power Ground
D2	PGND2_S	Buck 2 Power Ground Sense
D3	EN2	Buck 2 Enable
D4	EN1	Buck 1 Enable
E1	SW2	Buck 2 Switch Pin
E2	V_{IN2}	Power supply voltage input to PFET and NFET switches for Buck 2
E3	SGND	Signal GND
E4	FB2	Analog feedback for Buck 2

TABLE 1. Output Selection Table via I²C Programming

Buck Output Voltage Selection Codes		
Data Code	Buck_1 (V)	Buck_2 (V)
00000	NA	NA
00001	NA	1.8
00010	NA	1.85 or 1.9*
00011	NA	2.0
00100	NA	2.1
00101	1.00	2.2
00110	1.05	2.3
00111	1.10	2.4
01000	1.15	2.5
01001	1.20	2.6
01010	1.25	2.7
01011	1.30	2.8
01100	1.35	2.9
01101	1.40	3.0
01110	1.45	3.1
01111	1.50	3.2
10000	1.55	3.3
10001	1.60	NA
10010	1.65	NA
10011	1.70	NA
10100	1.75	NA
10101	1.80	NA
10110	1.85	NA
10111	1.90	NA
11000	1.95	NA
11001	2.00	NA

* Can be trimmed at the factory at 1.85V or 1.9V using the same trim code.

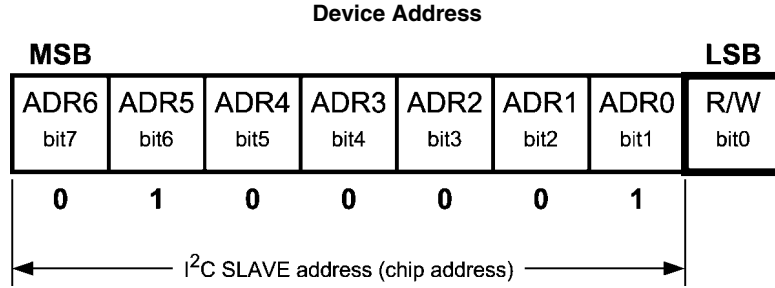
Device Ordering Information (LLP)

Order Number	Voltage Option	Package marking	Supplied As
LM3370SD - 3013	1.2V & 2.5V	S0003UB	1000 units, Tape-and-Reel
LM3370SDX - 3013		S0003UB	4500 units, Tape-and-Reel
LM3370SD - 3021	1.2V & 3.3V	S0003TB	1000 units, Tape-and-Reel
LM3370SDX - 3021		S0003TB	4500 units, Tape-and-Reel
LM3370SD - 3416	1.4V & 2.8V	S0003VB	1000 units, Tape-and-Reel
LM3370SDX - 3416		S0003VB	4500 units, Tape-and-Reel
LM3370SD-3621	1.5V & 3.3V	S0004AB	1000 units, Tape-and-Reel
LM3370SDX-3621		S0004AB	4500 units, Tape-and-Reel
LM3370SD - 3806	1.6V & 1.8V	S0003XB	1000 units, Tape-and-Reel
LM3370SDX - 3806		S0003XB	4500 units, Tape-and-Reel
LM3370SD - 4221	1.8V & 3.3V	S0003YB	1000 units, Tape-and-Reel
LM3370SDX - 4221		S0003YB	4500 units, Tape-and-Reel

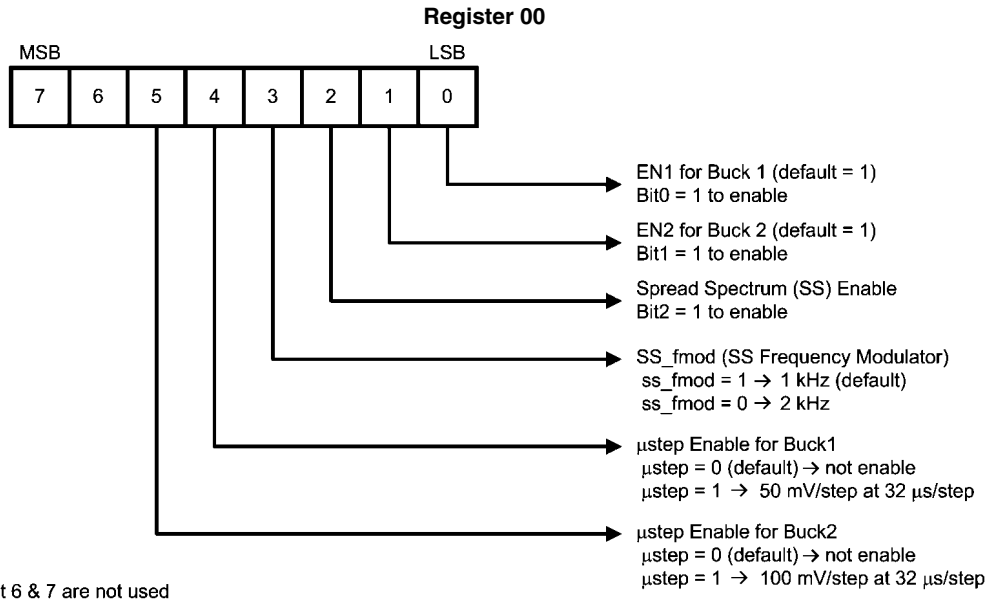
Device Ordering Information (micro SMD)

Order Number	Voltage Option	Package Marking	Supplied As
LM3370TL-3607 NOPB	1.5V & 1.9V	SPSB	1000 units, Tape-and-Reel
LM3370TLX-3607 NOPB		SPSB	3000 units, Tape-and-Reel
LM3370TL-3008 NOPB	1.2V & 2.0V	SPTB	1000 units, Tape-and-Reel
LM3370TLX-3008 NOPB		SPTB	3000 units, Tape-and-Reel
LM3370TL-3006 NOPB	1.2V & 1.8V	SPUB	1000 units, Tape-and-Reel
LM3370TLX-3006 NOPB		SPUB	3000 units, Tape-and-Reel
LM3370TL-3806 NOPB	1.6V & 1.8V	SPVB	1000 units, Tape-and-Reel
LM3370TLX-3806 NOPB		SPVB	3000 units, Tape-and-Reel
LM3370TL-3206 NOPB	1.3V & 1.8V	SPXB	1000 units, Tape-and-Reel
LM3370TLX-3206 NOPB		SPXB	3000 units, Tape-and-Reel
LM3370TL-3022 NOPB	1.2V & 1.85V	STHB	1000 units, Tape-and-Reel
LM3370TLX-3022 NOPB		STHB	3000 units, Tape-and-Reel

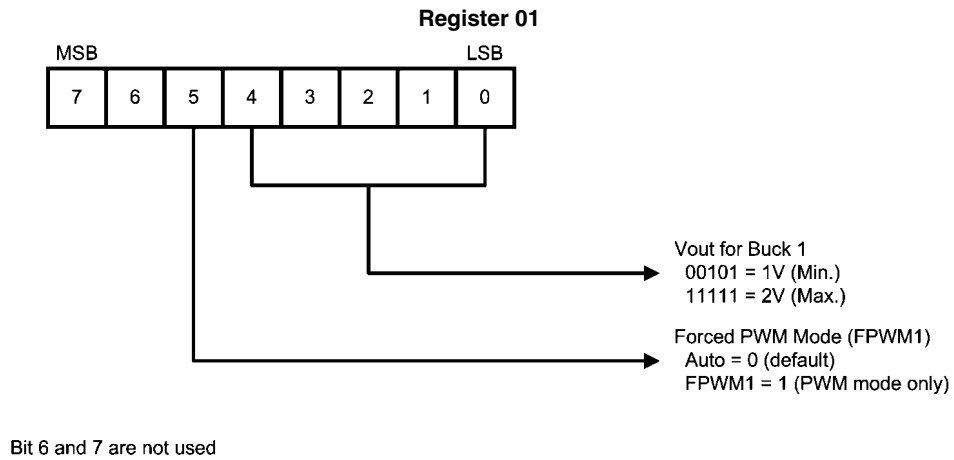
Registers Information



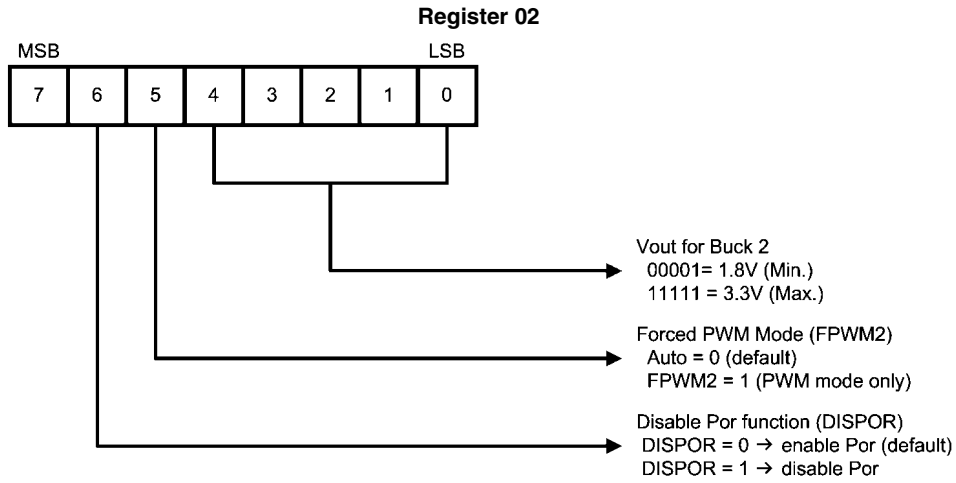
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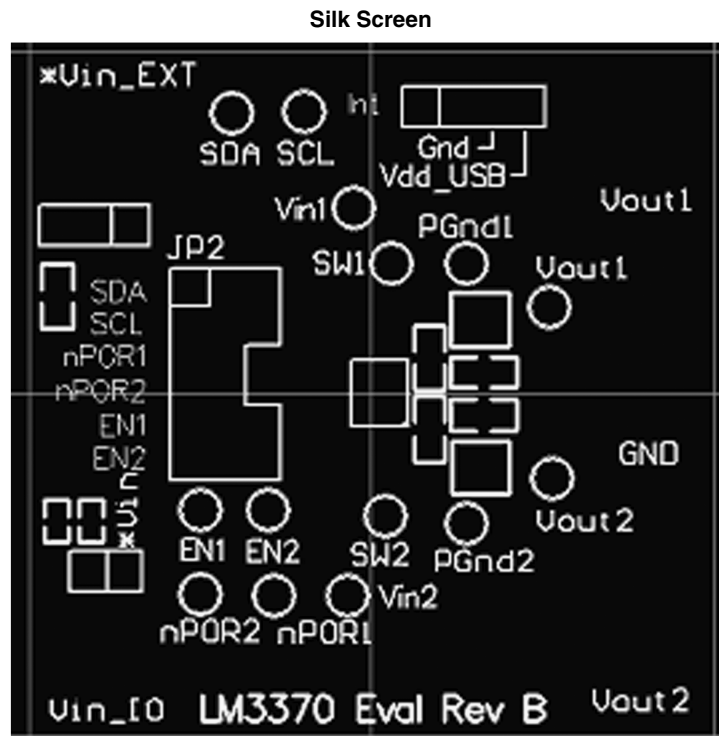


Bit 7 is not used

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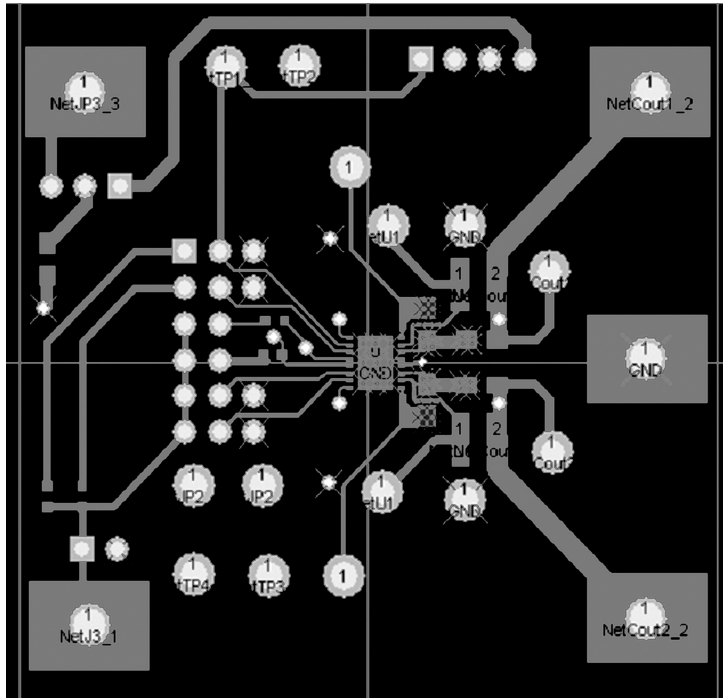
Evaluation Board Layout (LLP)

LM3370SD is a 4-layer board designed to maximize the performance for the device.



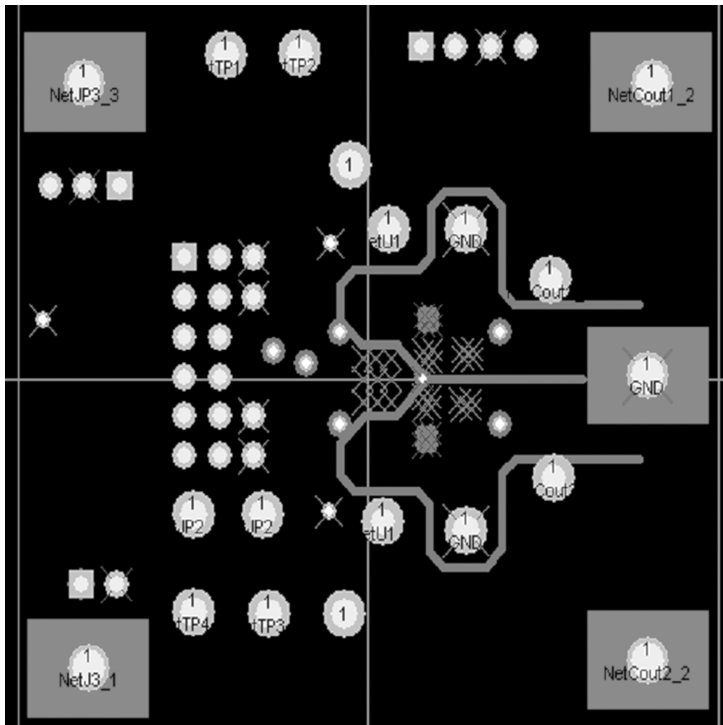
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Top Layer



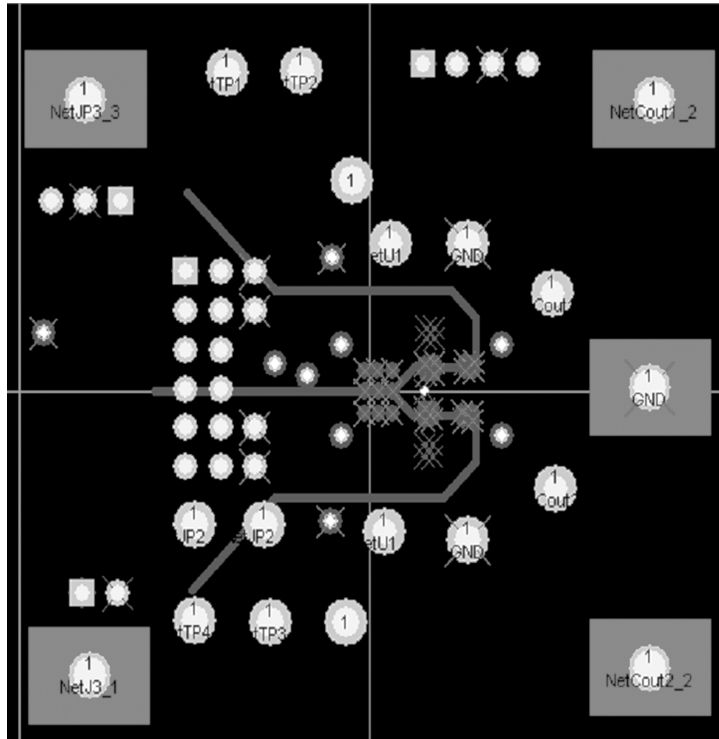
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Mid Layer 1



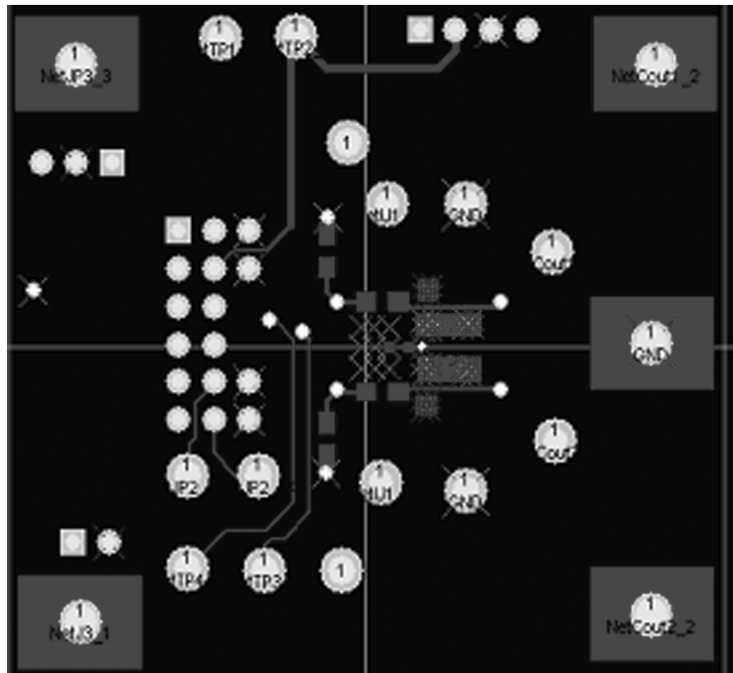
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Mid Layer 2



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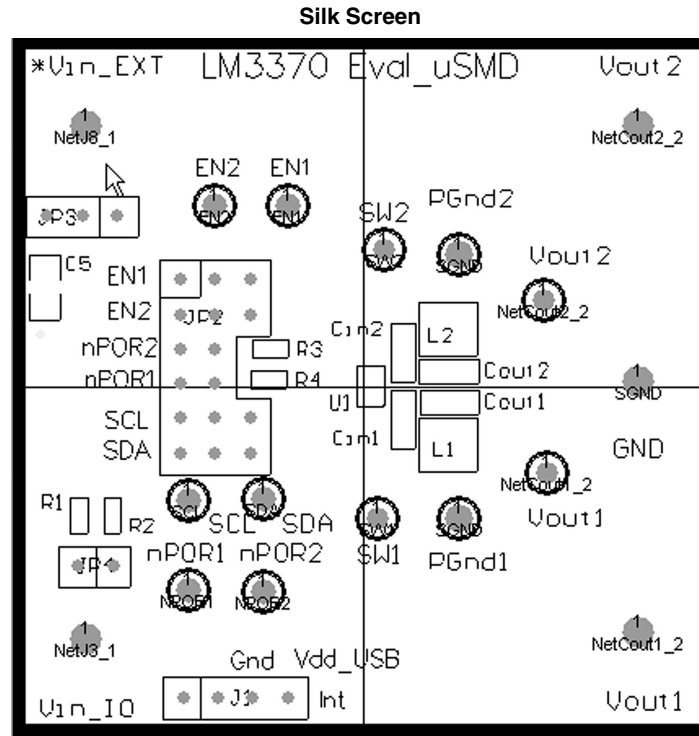
Bottom Layer



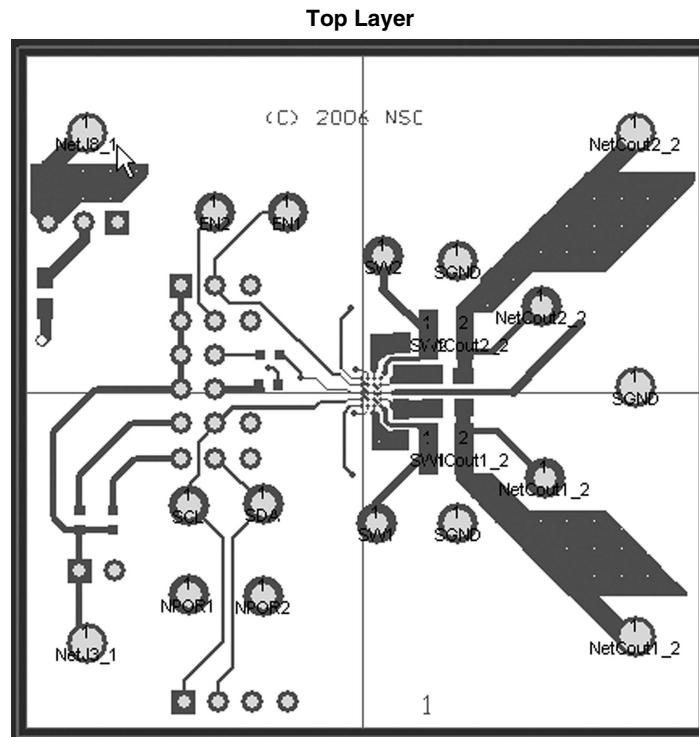
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Evaluation Board Layout (micro SMD)

The LM3370TL applications is of similar layout to the LLP board with the exception of the SCL, SDA pins. When using the USB interface cable the order of these pins is reversed.

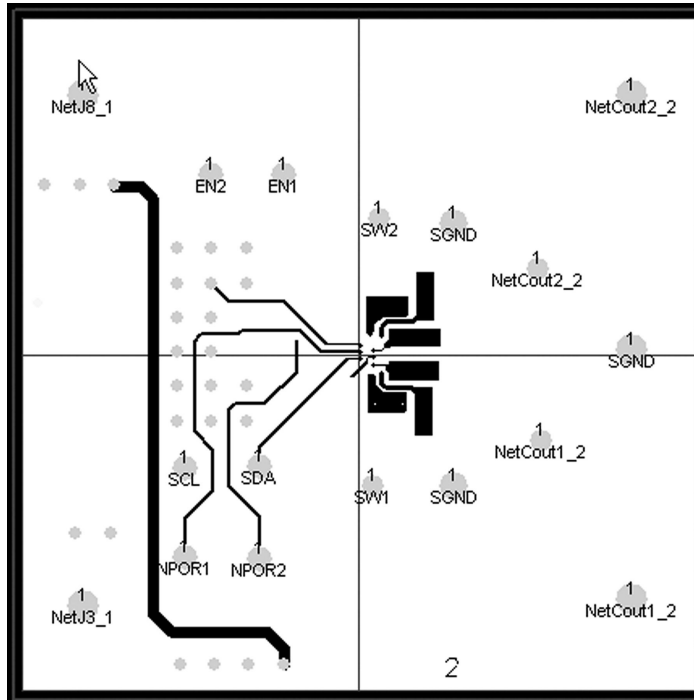


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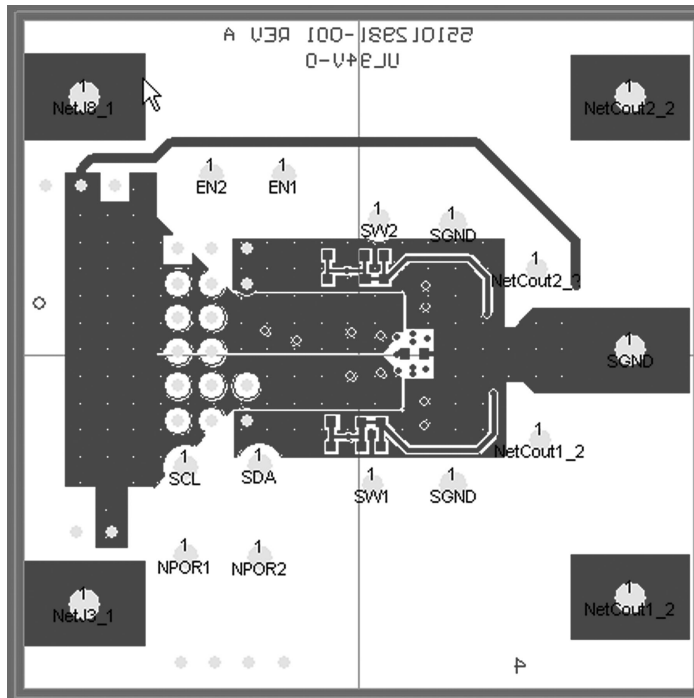
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Mid Layer 1



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Bottom Layer



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Bill of Materials

Component Name	Manufacture	Manufacture #	Specification
LM3370			
C _{IN1} & C _{IN2}	TDK	C2012X5R0J475K	4.7μF/6.3V/0805/X5R
	muRata	GRM219R60J475KE19D	
C _{OUT1} & C _{OUT2}	TDK	C2012X5R0J106K	10μF/6.3V/0805/X5R
	muRata	GRM219R60J106KE19D	
L1 & L2	Taiyo-Yuden	NR3015T-2R2M	2.2μH
R1-2(SDA+SCL)	Vishay		2k ohms
R3-4 (nPOR1-2)	Vishay		100k ohms
TEST Pins & Connectors			
V _{OUT1} , V _{OUT2} , GND, *Vin_EXT, Vin_IO			Turret 0.09 in
nPOR1, nPOR2, SDA, SCL, PGND1, PGND2, V _{IN1} , V _{IN2}			Turret 0.072 in
Jumper			
SDA/SCL/nPOR1	Jumpers Female(Handle centerline)		A26242-ND
nPOR2/EN1/EN2			
*VIN & *VIN_IO			
*VIN_IO	Berk stick	Header	2 in series (2x1)
*VIN_EXT			2 in series (2x1)
Int			4 in series (4x1)
JP2:SDA & SCL			6 in series(6x2)
nPOR1/ nPOR2/EN1& EN2			2 in series 2(2x1)

Notes

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Notes

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