

# LM5010 Evaluation Board

National Semiconductor  
Application Note 1352  
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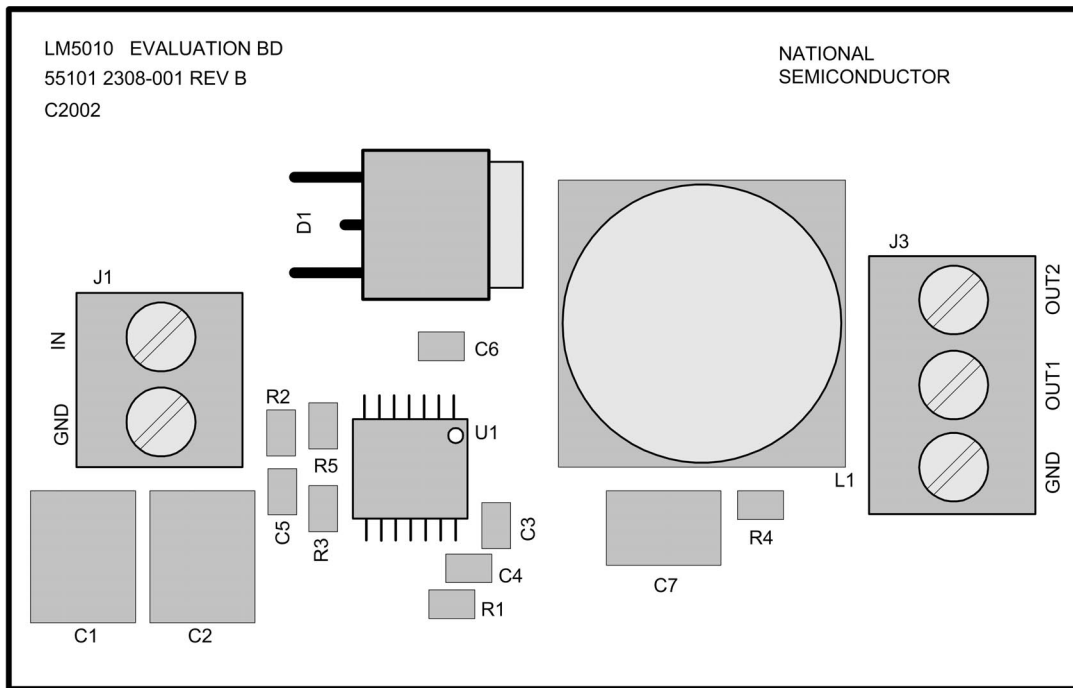


## Introduction

The LM5010EVAL evaluation board provides the design engineer with a fully functional buck regulator, employing the constant on-time (COT) operating principle. This evaluation board provides a 10V output from an input range of 12V - 75V. The circuit provides load currents > 1A, with the current limit set at  $\approx 1.3A$ .

The board's specification are:

- Input Voltage: 12V to 75V
- Output Voltage: 10V,  $\pm 3\%$
- Maximum Continuous Output current: 1.0A
- Current Limit: 1.3A
- Measured Efficiency: 93% ( $V_{IN} = 12V$ ,  $I_{OUT} = 500\text{ mA}$ )
- Switching Frequency:  $\approx 480\text{ kHz}$
- Size: 1.1 in. x 1.875 in. x 0.47 in



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FIGURE 1. Evaluation Board - Top Side

## Theory of Operation

Refer to the board's schematic in *Figure 4*, which contains a simplified block diagram of the LM5010. When the circuit is in regulation, the buck switch is on each cycle for a time determined by R1 and  $V_{IN}$  according to the equation:

$$t_{ON} = \frac{1.18 \times 10^{-10} \times (R1 + 1.4k)}{V_{IN} - 1.4V} + 67\text{ ns}$$

The on-time in this evaluation board will range from  $\approx 1750\text{ ns}$  at  $V_{IN} = 12V$ , to  $\approx 310\text{ ns}$  at  $V_{IN} = 75V$ . At the end of the on-time, the feedback voltage at FB is above 2.5V, and the Minimum Off-Timer ensures the buck switch is off for at least 265 ns. In normal operation, the off-time is longer. During the off-time, the output capacitor (C7) discharges, and when the output voltage falls so that the voltage at FB is below 2.5V,

the comparator output switches to initiate a new on-time. As required by the datasheet, this circuit provides a minimum of 25mVp-p ripple at the FB pin. Refer to the LM5010 data sheet for a more detailed block diagram, and a complete description of the various functional blocks.

## Board Layout and Probing

The pictorial in *Figure 1* shows the placement of the circuit components. The following should be kept in mind when the board is powered:

- 1) When operating at high input voltage and/or high load current, forced air flow **IS NECESSARY**.
- 2) The LM5010, and the diode D1 will be hot to the touch when operating at high input voltage and/or high load current.

## Board Layout and Probing (Continued)

- 3) Use CAUTION when probing the circuit at high input voltages. 75 volts is enough to produce shocks and sparks.
- 4) At maximum load current (1A), the wire size and length used to connect the load becomes important. Ensure there is not a significant drop in the wires.

## Board Connection/Start-up

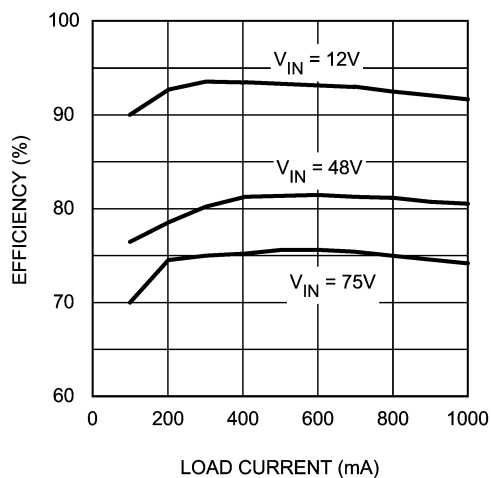
The input connections are made to the J1 connector. The load is normally connected to the OUT1 and GND terminals of the J3 connector. Ensure the wires are adequately sized for the intended load current. Before start-up a voltmeter should be connected to the input terminals, and to the output terminals. The load current should be monitored with an ammeter or a current probe. It is recommended that the input voltage be increased gradually to 8V, at which time the output voltage will be approximately 7V. If that indicates correctly, then increase the input voltage to the minimum operating value of 12V, and proceed with evaluating the circuit.

## Low Ripple Output

The ripple voltage at OUT1 will range from  $\approx 120$  mVp-p (at  $V_{IN} = 12V$ ) to  $\approx 650$  mVp-p (at  $V_{IN} = 75V$ ). If a low ripple output is desired, connect the load to OUT2. The ripple at this output varies from  $\approx 10$  mVp-p to  $\approx 60$  mVp-p over the input voltage range. However, the load regulation is not as good at OUT2 as it is at OUT1 due to the presence of R4.

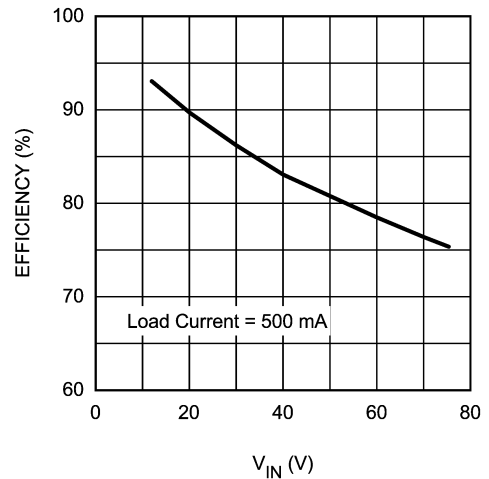
## Increased Current Limit

The evaluation board current limit activates at a load current of  $\approx 1.3A$ . If it is desired to increase the current limit for a particular application, R5 must be added to the board. Refer to the data sheet to determine the appropriate value for this resistor.



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FIGURE 2. Efficiency vs Load Current



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FIGURE 3. Efficiency vs  $V_{IN}$

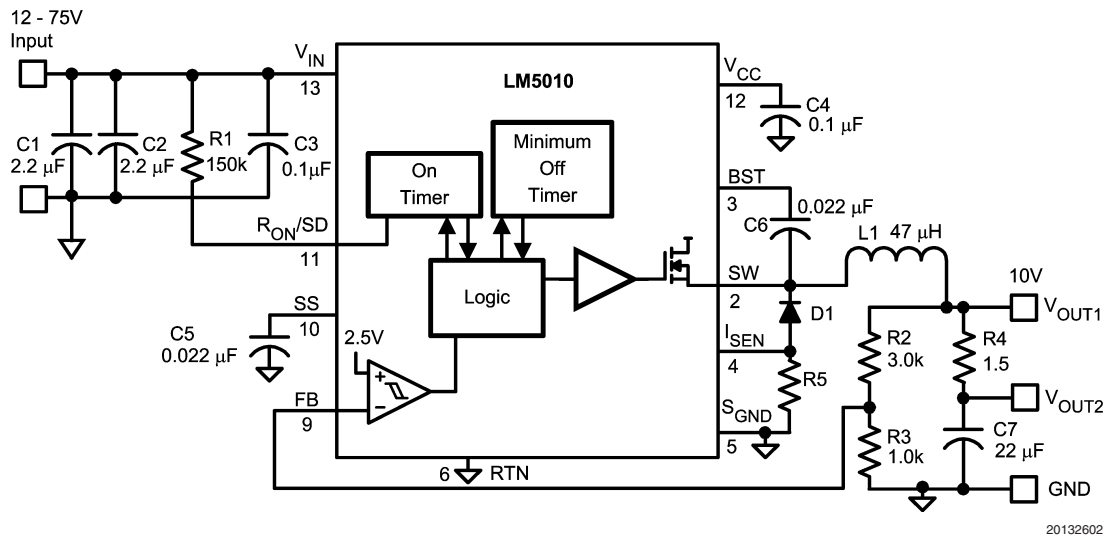
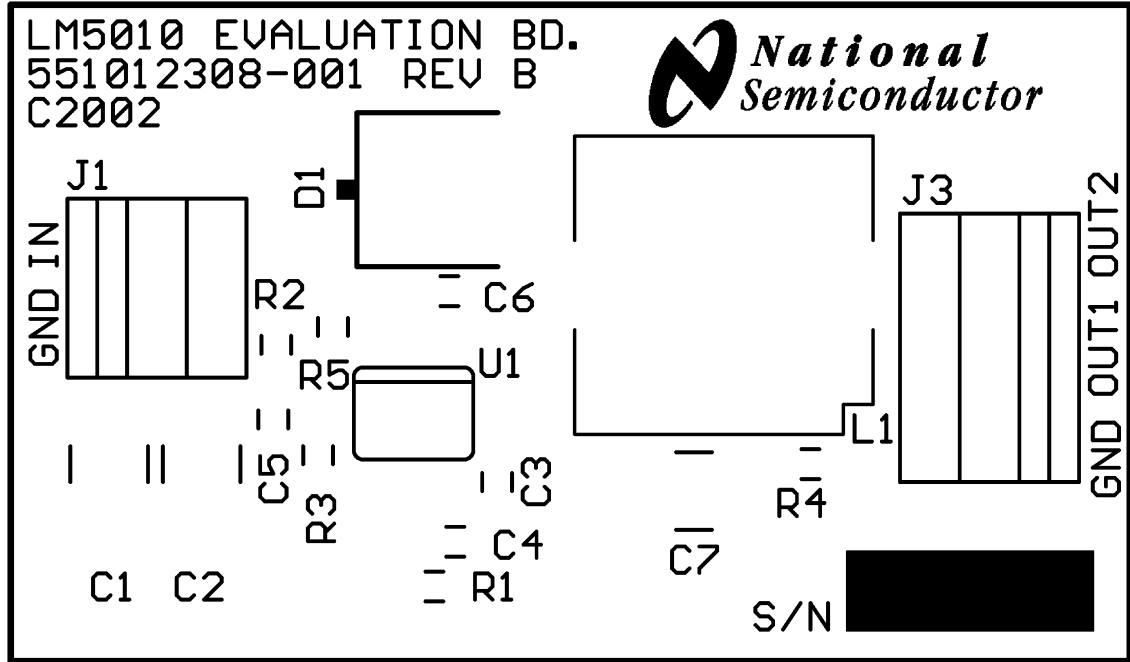


FIGURE 4. Board Schematic

## Bill of Materials

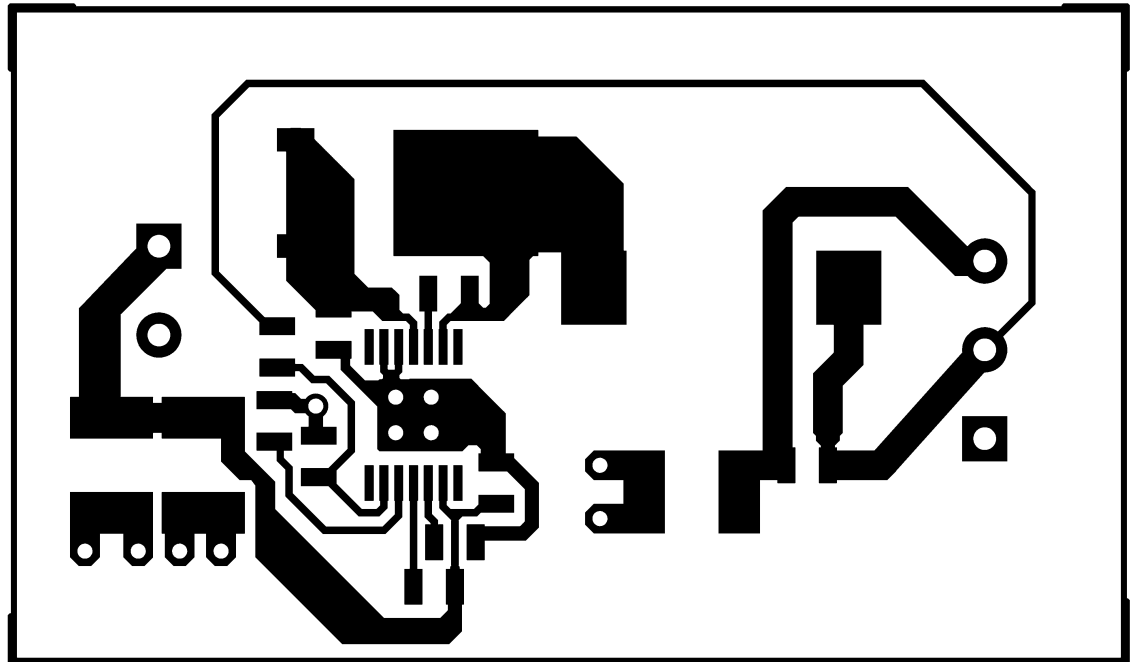
Item	Description	Mfg. Part Number	Package	Value
C1, 2	Ceramic Capacitor	TDK C4532X7R2A225M	1812	2.2 $\mu$ F, 100V
C3	Ceramic Capacitor	TDK C2012X7R2A104M	0805	0.1 $\mu$ F, 100V
C4	Ceramic Capacitor	TDK C2012X7R1C104M	0805	0.1 $\mu$ F, 16V
C5, 6	Ceramic Capacitor	TDK C2012X7R1C223M	0805	0.022 $\mu$ F, 16V
C7	Ceramic Capacitor	TDK C4532X7R1E226M	1812	22 $\mu$ F, 25V
D1	Ultra Fast Diode	Central Semi CUD6-02C	DPAK	200V, 6A, 35 ns
L1	Power Inductor	TDK SLF12575T-470M2R7	12.5 mm x 12.5 mm	47 $\mu$ H, 3A
R1	Resistor	CRCW08051503F	0805	150 k $\Omega$
R2	Resistor	CRCW08053001F	0805	3.00 k $\Omega$
R3	Resistor	CRCW08051001F	0805	1.00 k $\Omega$
R4	Resistor	CRCW08051R50F	0805	1.5 $\Omega$
R5	Resistor	See data sheet	0805	
U1	Switching Regulator	National Semiconductor LM5010MH	TSSOP - 14EP	

PCB Layout



SILKSCREEN LAYER (.PLC) AS VIEWED FROM TOP

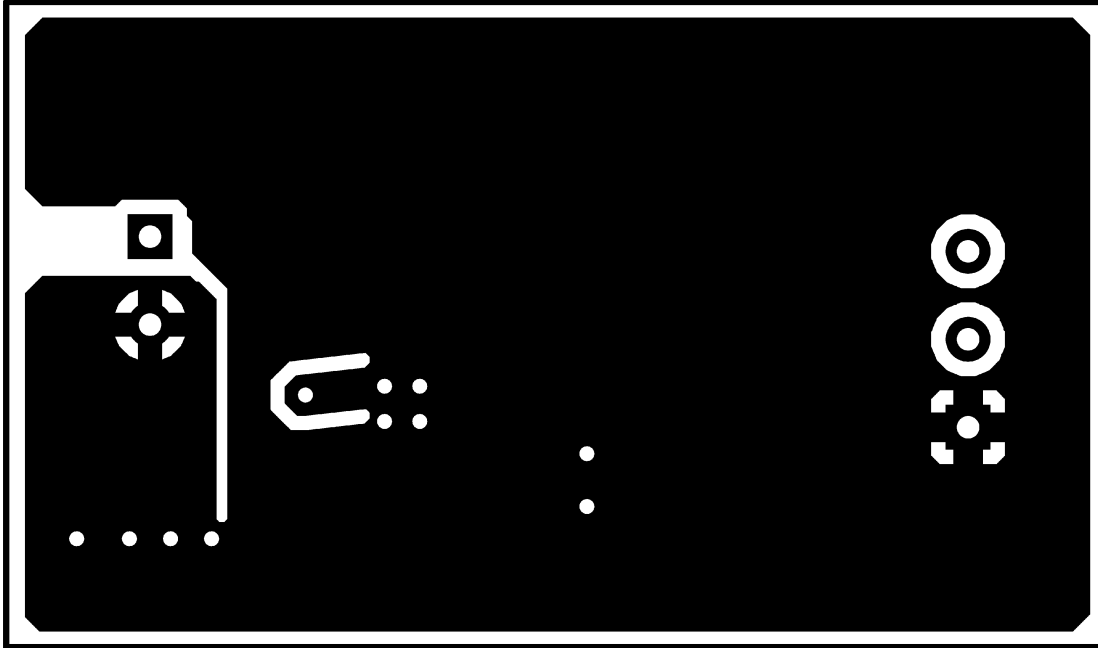
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TOP LAYER (.CMP) AS VIEWED FROM TOP

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## PCB Layout (Continued)



BOTTOM LAYER (.SOL) AS VIEWED FROM TOP

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