LM5010A Evaluation Board

National Semiconductor
Application Note 1423
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Introduction

The LM5010AEVAL evaluation board provides the design engineer with a fully functional buck regulator, employing the constant on-time (COT) operating principle. This evaluation board provides a 5V output over an input range of 6V - 75V. The circuit delivers load currents to 1A, with current limit set at ≈1.3A. The board is populated with all external components except R6 and C9-C11. These components provide options for reducing output ripple as described later in this document.

The board's specification are:

- Input Voltage: 6V to 75V
- Output Voltage: 5V
- Maximum load current: 1.0A
- Minimum load current: 0A
- Current Limit: 1.3A
- Measured Efficiency: 94.75% (V_{IN} = 6V, I_{OUT} = 200 mA)
- Nominal Switching Frequency: 200 kHz
- Size: 2.25 in. x 0.88 in. x 0.47 in

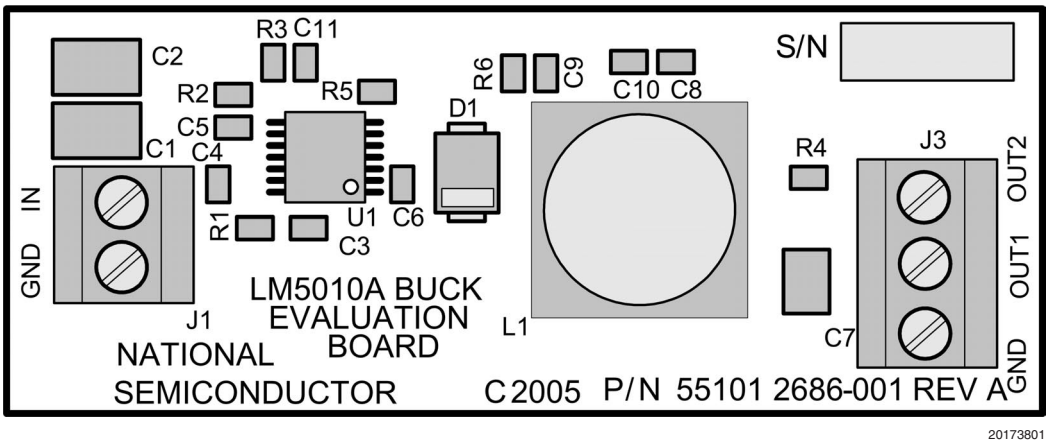


FIGURE 1. Evaluation Board - Top Side

Theory of Operation

Refer to the evaluation board schematic in Figure 3, which contains a simplified block diagram of the LM5010A. When the circuit is in regulation, the buck switch is on each cycle for a time determined by R1 and V_{IN} according to the equation:

$$t_{ON} = \frac{1.18 \times 10^{-10} \times (R1 + 1.4k)}{(V_{IN} - 1.4V)} + 67\ ns$$

The on-time of this evaluation board ranges from ≈5000 ns at V_{IN} = 6V, to ≈380 ns at V_{IN} = 75V. The on-time varies inversely with V_{IN} to maintain a nearly constant switching frequency. At the end of each on-time the Minimum Off-Timer ensures the buck switch is off for at least 260 ns. In normal operation, the off-time is much longer. During the off-time, the output capacitor (C7) is discharged by the load current. When the output voltage falls sufficiently that the voltage at FB is below 2.5V, the regulation comparator initiates a new on-time period. For stable, fixed frequency operation, ≈25 mV of ripple is required at FB to switch the regulation comparator. Refer to the LM5010A data sheet for a more detailed block diagram, and a complete description of the various functional blocks.

Board Layout and Probing

The pictorial in Figure 1 shows the placement of the circuit components. The following should be kept in mind when the board is powered:

1) When operating at high input voltage and high load current, forced air flow is necessary.

2) The LM5010A, and the diode D1 will be hot to the touch when operating at high input voltage and high load current.

3) Use CAUTION when probing the circuit at high input voltages to prevent injury, as well as possible damage to the circuit.

4) At maximum load current (1A), the wire size and length used to connect the load becomes important. Ensure there is not a significant drop in the wires between this evaluation board and the load.

Board Connection/Start-up

The input connections are made to the J1 connector. The load is normally connected to the OUT1 and GND terminals of the J3 connector. Ensure the wires are adequately sized for the intended load current. Before start-up a voltmeter should be connected to the input terminals, and to the output terminals. The load current should be monitored with an

Board Connection/Start-up (Continued)

ammeter or a current probe. It is recommended that the input voltage be increased gradually to 6V, at which time the output voltage should be 5V. If the output voltage is correct with 6V at V_{IN}, then increase the input voltage as desired and proceed with evaluating the circuit.

Reducing Output Ripple

The LM5010A requires a minimum of 25 mVp-p ripple at the FB pin, in phase with the switching waveform at the SW pin, for proper operation. In the basic application circuit shown in the data sheet, C8 is not included. The required ripple at FB is derived from the ripple at V_{OUT1}, which is generated by the inductor's ripple current passing through R4 and the ESR of capacitor C7. Since the ripple voltage at V_{OUT1} is attenuated by the R2/R3 feedback divider, a minimum of 50 mVp-p is required at V_{OUT1}. If this ripple level is acceptable for the intended application, C8 can be removed from this evaluation board, and R4 increased to 1.5Ω. In that case, the minimum ripple amplitude (≈55 mVp-p) occurs at minimum Vin (6V), and increases to ≈340 mVp-p at Vin = 75V, as shown in Figure 6.

If a low ripple output is desired three alternatives are described below.

A) **Ripple Reduction Option A:** This EVB is supplied with C8 installed, and R4 = 0.68Ω, providing a relatively low ripple output at V_{OUT1} since C8 couples the output ripple directly to FB without attenuation. The ripple amplitude at V_{OUT1} ranges from 30mVp-p to 170 mVp-p (see Figure 6) as Vin is varied over its range. The minimum value for C8 is calculated from:

$$C8 = \frac{t_{ON(max)}}{(R2//R3)}$$

where $t_{ON(max)}$ is the maximum on-time at minimum Vin, and R2//R3 is the equivalent parallel value of R2 and R3. For this evaluation board, $t_{ON(max)}$ is approximately 5000 ns, and R2//R3 = 500Ω, resulting in a minimum value of 0.01 µF for C8.

B) **Ripple Reduction Option B:** Add R6, C9, C10, replace R4 with zero ohms, and leave C8 and C11 positions open. Since the SW pin switches from -1V to V_{IN}, and the right end of C9 is a virtual ground, R6 and C9 are chosen to generate a 30-40 mVp-p triangle wave at their junction. That triangle wave is coupled to the FB pin through C10. To calculate the values for R6, C9, and C10, use the following procedure, using the minimum input voltage for Vin:

Calculate the voltage V_A:

$$V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/Vin)))$$

where V_{SW} is the absolute value of the voltage at the SW pin during the off-time (typically 1V), and Vin is the minimum input voltage. For this circuit, V_A calculates to 4.83V. This is the DC voltage at the R6/C9 junction, and is used in the next equation.

Calculate the R6•C9 product:

$$R6 \bullet C9 = \frac{(Vin - V_A) \times t_{ON}}{\Delta V}$$

where t_{ON} is the on-time at minimum Vin (≈5 µs), and ΔV is the desired ripple amplitude at the R6/C9 junction, 30mV for this example.

$$R6 \bullet C9 = \frac{(6V - 4.83V) \times 5\ \mu s}{0.03V} = 1.95 \times 10^{-4}$$

R6 and C9 are then chosen from standard value components to satisfy the above product. For example, C9 can be 1000 pF, requiring R6 to be 195 kΩ. C10 is chosen to be 0.01 µF, large compared to C9. R2 and R3 are increased to 5 kΩ each to reduce the loading on the signal provided through C10. The resulting circuit is:

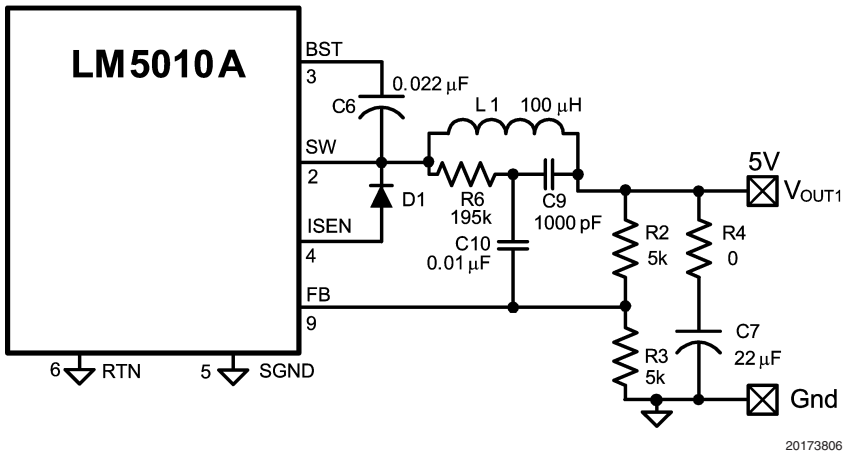


FIGURE 2. Low Ripple Output Using R6, C9, C10

The resulting ripple at V_{OUT1} ranges from 5 mVp-p at Vin = 6V, to 18 mVp-p at Vin = 75V, and varies slightly with load current. See Figure 6. These values are valid only for continuous conduction mode (load current is between 120 mA and 1.3A). If the load current is reduced below 120 mA such that the circuit operates in discontinuous conduction mode

Reducing Output Ripple (Continued)

the V_{OUT1} ripple ranges from ≈40 mVp-p to ≈100 mVp-p. If the circuit is operated in current limit mode the ripple ranges from ≈100 mVp-p to ≈300 mVp-p.

B) **Ripple Reduction Option C:** Connect the load to V_{OUT2} (leave R4 in). The ripple at this output varies from ≈3 mVp-p to ≈7.5 mVp-p over the input voltage range. See Figure 6. However, the load regulation is not as good at V_{OUT2} as at V_{OUT1} due to the presence of R4. This alternative may be preferred for applications where the load current is relatively constant.

Increasing the Current Limit

The evaluation board current limit activates at a load current of ≈1.3A. If it is desired to increase the current limit for a particular application, R5 must be added to the board. Refer to the LM5010A data sheet to determine the appropriate value for this resistor.

Minimum Load Current

The LM5010A requires a minimum load current of ≈500 µA to ensure the boost capacitor (C6) is recharged sufficiently during each off-time. In this evaluation board, the minimum load current is provided by the feedback resistor (R2, R3), allowing the board's minimum load current at V_{OUT1} (or V_{OUT2}) to be specified at zero.

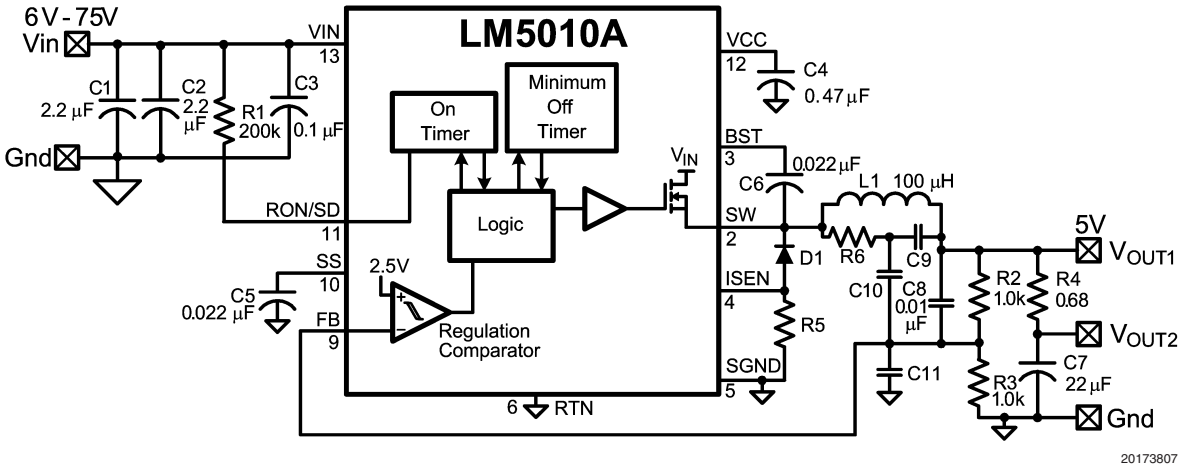


FIGURE 3. Evaluation Board Schematic

Bill of Materials

Item	Description	Mfg., Part Number	Package	Value
C1, 2	Ceramic Capacitor	TDK C4532X7R2A225M	1812	2.2 µF, 100V
C3	Ceramic Capacitor	TDK C2012X7R2A104M	0805	0.1 µF, 100V
C4	Ceramic Capacitor	TDK C2012X7R1C474M	0805	0.47 µF, 16V
C5, 6	Ceramic Capacitor	TDK C2012X7R1C223M	0805	0.022 µF, 16V
C7	Ceramic Capacitor	TDK C4532X7R1E226M	1812	22 µF, 25V
C8	Ceramic Capacitor	TDK C2012X7R1C103M	0805	0.01 µF, 16V
C9		Unpopulated		
C10		Unpopulated		
C11		Unpopulated		
D1	Schottky Diode	Central Semi CMSH2-100	SMB	100V, 2A
L1	Power Inductor	TDK SLF12575T-101M1R9, or	12.5 mm x 12.5 mm	100 µH, 1.9A
		Cooper Bussmann DR125-101		
R1	Resistor	CRCW08052003F	0805	200 kΩ
R2, 3	Resistor	CRCW08051001F	0805	1.00 kΩ
R4	Resistor	ERJ-6RQFR68V (Panasonic)	0805	0.68 Ω
R5		Unpopulated		
R6		Unpopulated		
U1	Switching Regulator	National Semiconductor LM5010AMH	TSSOP - 14EP	

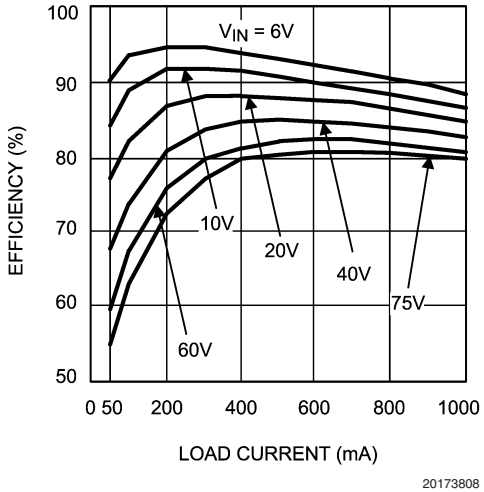


FIGURE 4. Efficiency vs Load Current

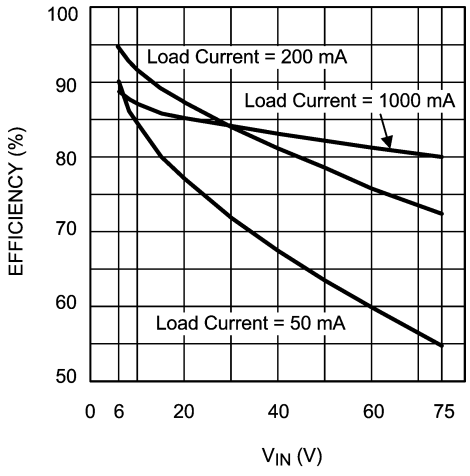


FIGURE 5. Efficiency vs V_{IN}

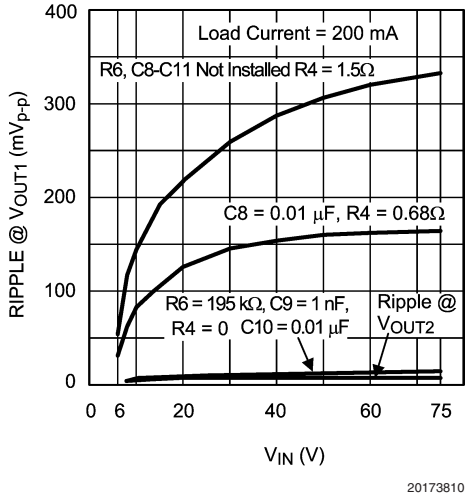
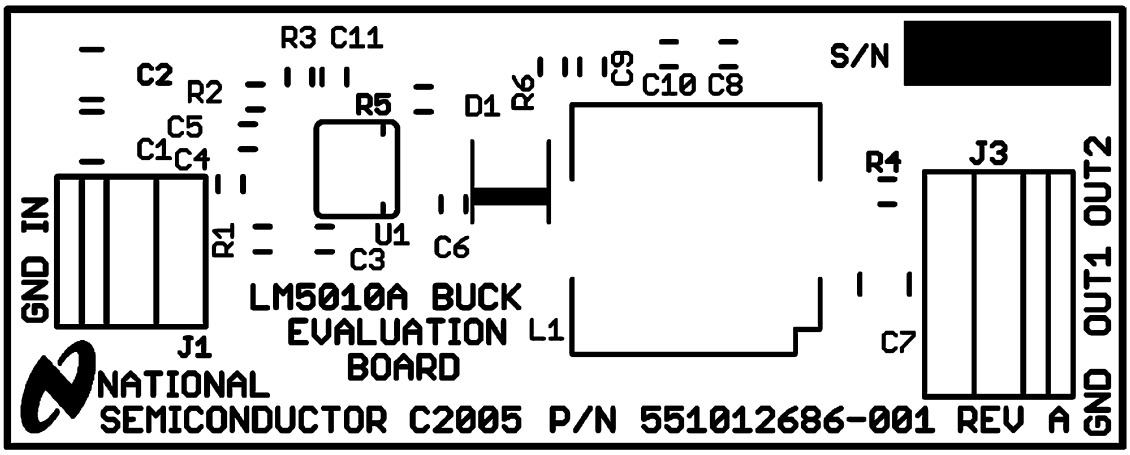


FIGURE 6. Voltage Ripple at V_{OUT1}, V_{OUT2}

PCB Layout



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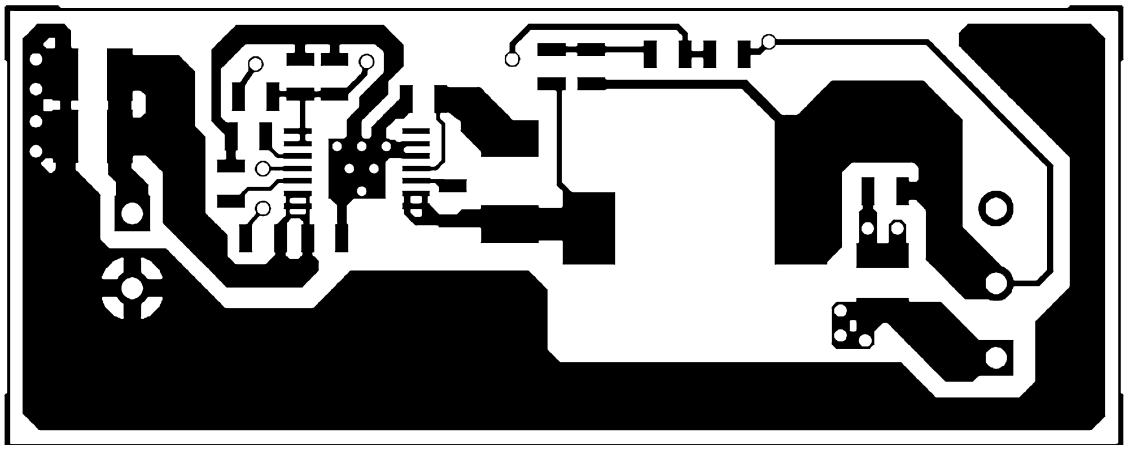
Board Silkscreen



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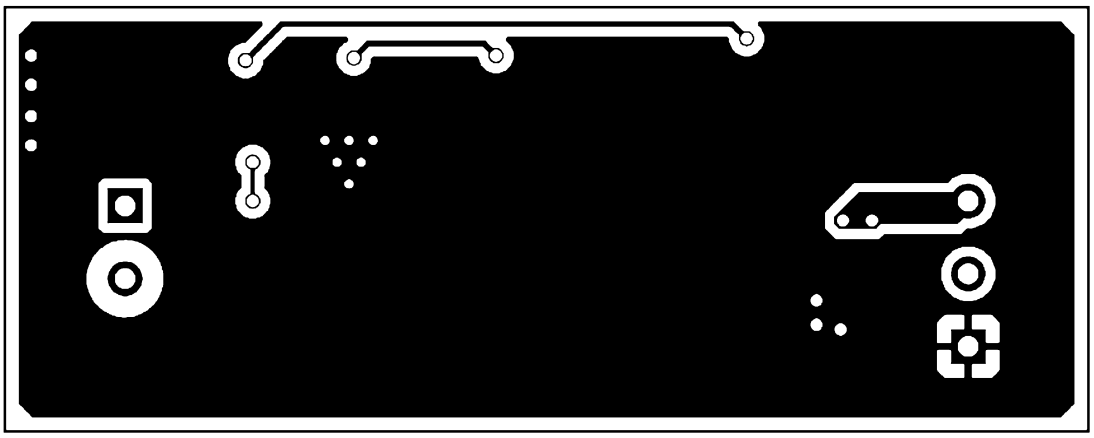
Board Top Layer



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Board Bottom Layer (viewed from top)

Notes

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