

LM3475 Evaluation Board

National Semiconductor
Application Note 1381
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May 2005



Introduction

The LM3475 evaluation board is provided as a tool for developing DC/DC converters based on the LM3475 IC. As shown in *Figure 1*, the evaluation board is configured to provide an output of 2.5V at up to 2A from an input up to 10V. The corresponding bill of material is given in *Table 1*. Typical efficiencies are shown in *Figure 2* and *Figure 3*. *Figure 4* and *Figure 5* show the board layout.

To aid in the design and evaluation of dc/dc buck converters based on the LM3475 controller, the LM3475 Evaluation Board can be easily re-configured for different output voltages.

Setting Vout

Vout can be set using R_{FB1} , as shown in the following equation:

$$V_{OUT} = V_{FB} \times (R_{FB1} + R_{FB2}) / R_{FB2}$$

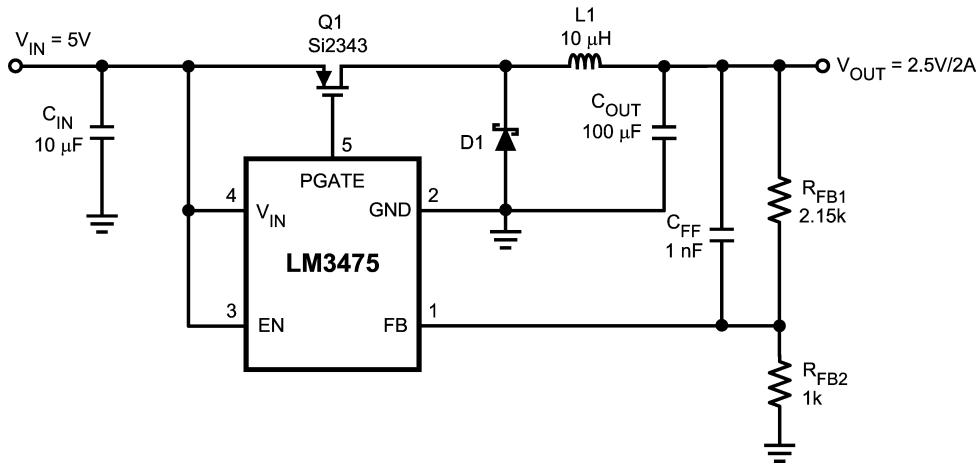
Where V_{FB} is 0.8V typically.

Refer to the datasheet before changing any component values, since additional design adjustments may be required.

Optional Components

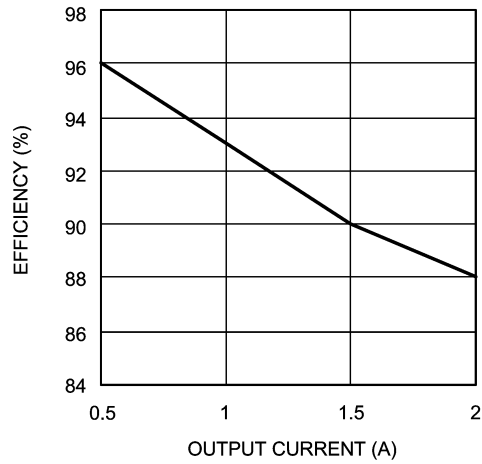
A feed-forward capacitor C_{FF} is placed on the board, which will increase operating frequency. However, the speed up effect decreases with lower output voltage and is negligible below 1.6V output.

A zero Ohm is used to pull up the EN pin for always on operation. The enable pin can be pulled low at the EN post to shutdown the device. If this resistor is removed, any analog level signal can be used to enable and disable the device.



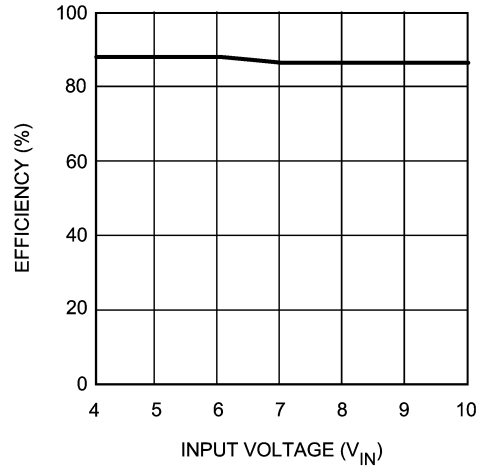
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FIGURE 1. Full Demo Board Schematic



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**FIGURE 2. Efficiency vs Output Current
($V_{in} = 5V$)**



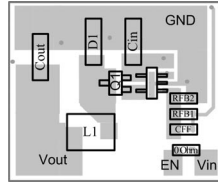
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**FIGURE 3. Efficiency vs Input Voltage
($I_{out} = 2A$)**

TABLE 1. Bill of Materials

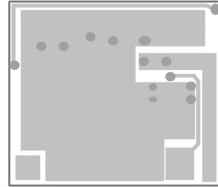
Designator	Part Description	Part Number
CIN	10 μ F 16V ceramic	Yuden EMK325BJ106MN
COUT	100 μ F 6V tantalum	AVX TPSY107M006R0100
CFF	1 nF 25V ceramic	VJ1206Y102KXXA
D1	Schottky 20V 2A	Central CMSH2-20L
L1	10 μ H 3.1 A	Sumida CDRH103R100
Q1	Si 2343 30V 2.5A	Vishay Si2343
RFB2	1 k Ω	Vishay CRCW08051001F
RFB1	2.15 k Ω	Vishay CRCW08052151F
R2	0 Ω	Vishay CRCW08050R00F

PCB Layout Diagram(s)



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FIGURE 4. Top Side Layout



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FIGURE 5. Bottom Side Layout

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