

LM22672 Evaluation Board

National Semiconductor
Application Note 1896
Frederik Dostal
July 6, 2010



Introduction

The LM22672 evaluation board is designed to demonstrate the capabilities of the LM22672 switching regulator. The LM22672 evaluation board schematic shown in [Figure 1](#) is configured to provide an output voltage of 3.3V up to 1A load current with an input voltage range of 4.5V to 42V. Due to the low $R_{DS(ON)}$ of the integrated N-channel MOSFET and maximum duty-cycle limitations, the minimum input voltage of 4.5V will only provide a 3.3V output voltage for load currents up to 500 mA. For load currents higher than 500 mA, an input voltage of 5.5V or higher is required. The typical operating frequency is 500 kHz. The evaluation board is designed to operate at ambient temperatures up to 50°C.

The performance of the evaluation board is as follows:

Input Range: 4.5V to 42V

Output Voltage: 3.3V

Output Current Range: 0A to 1A

Frequency of Operation: 500 kHz

Board Size: 1.5 X 1.5 inches

Package: PSOP-8

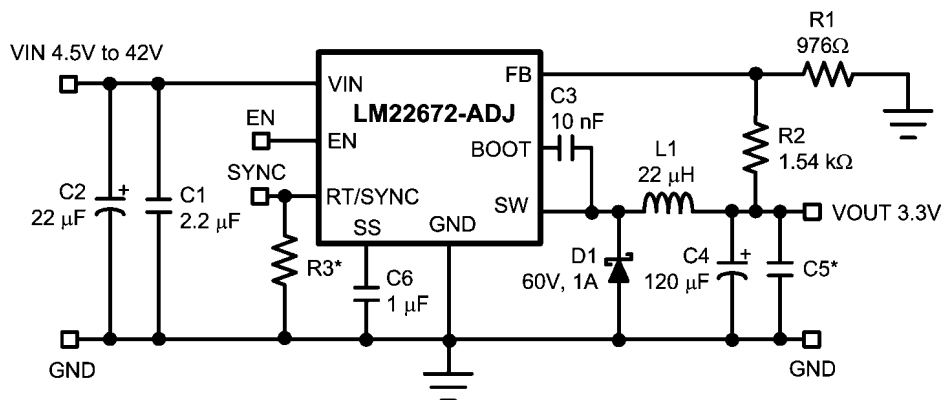
At low input voltages between 4.5V and 6V, a minimum load of approximately 5 mA may be required to reach a regulated 3.3V output voltage. See the LM22672 datasheet for more details.

To aid in the design and evaluation of DC/DC buck converter solutions based on the LM22672 switching regulator, the evaluation board can be re-configured for different output voltages.

Typical evaluation board performance and characteristics curves are shown in [Figure 2](#) through [Figure 5](#). [Figure 6](#) shows the PCB layout.

Test points are provided to enable easy connection and monitoring of critical signals. When performing over load or short circuit tests, refer to the current limit section of the LM22672 datasheet to determine if the circuit is in safe operating mode.

For more information about device function and electrical characteristics, refer to the LM22672 datasheet.



*component not populated on LM22672EVAL evaluation board

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FIGURE 1. Evaluation Board Schematic

Evaluation Board Setup

Before applying power to the LM22672 evaluation board, all external connections should be verified. The external power supply must be turned off and connected with proper polarity to the VIN and GND posts. A load resistor or electronic load should be connected between the VOUT and GND posts as desired. Both the VIN and VOUT connections should use the closest GND posts respective to VIN or VOUT. The output voltage can be monitored with a multi-meter or oscilloscope at the VOUT post.

Once all connections to the evaluation board have been verified, input power can be applied. A load resistor or electronic load does not require connection during startup. If the EN test point is left floating, the output voltage will ramp up when an input voltage is applied. Make sure that the external power supply (input voltage power source) is capable of providing enough current so that the adjusted output voltage can be obtained. Keep in mind that the startup current will be greater than the steady state current.

Synchronization and Adjustable Frequency

A SYNC test point is provided to allow synchronization of the LM22672 to an external clock signal. Space for a frequency adjust resistor, R3, is also provided. Refer to the LM22672 datasheet for more details about the synchronizing and adjustable frequency features.

Precision Enable

The EN test point provided on the LM22672 evaluation board can be used to shut down the LM22672 when connecting this test point to ground.

Soft-Start

The capacitor C6 sets the amount of soft-start. A 1 μ F soft-start capacitor is used for slow start-up. See the LM22672 datasheet for details about the soft-start function.

Component Selection

Before changing the default components refer to the LM22672 datasheet for information regarding component selection. The WEBENCH® designer online circuit simulation tool is also available at www.national.com.

The output voltage is adjustable with resistors R1 and R2 shown in the schematic. Any changes to these evaluation board feedback resistors may require changes to the inductor and output capacitor values. It is especially important to change the output capacitor, C4, if the output voltages are adjusted higher than 5V. The Schottky diode, D1, has a voltage rating of 60V to allow for a 42V maximum input voltage. If the input voltage is below 38V, a 40V Schottky diode may be used with a lower forward voltage to improve efficiency. The input capacitor, C2, is not always required. This capacitor is placed on the evaluation board to make the application robust and minimize input voltage ringing if power is suddenly applied. Capacitor C2 also helps stabilize the transfer function of the converter loop. The input capacitor C1 provides the main contribution to the switch current. Both capacitors are selected with appropriate values intended only for the evaluation of the LM22672. For production designs, the impedance of the power source as well as the ripple current rating of the selected input capacitors need to be taken into consideration and modified accordingly. See the LM22672 datasheet for more information.

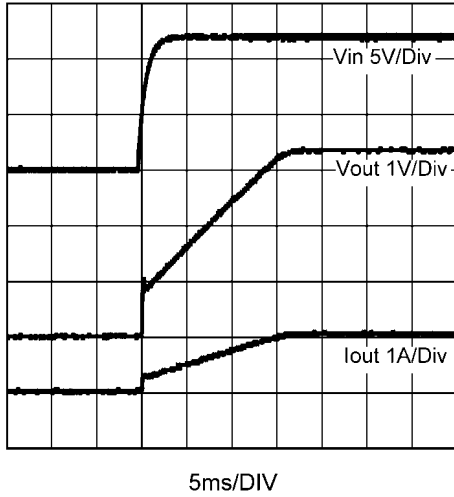
Output capacitor C5 is not populated but space is provided to add a second output capacitor. This second output capacitor may be used to further reduce output voltage ripple.

TABLE 1. LM22672EVAL Bill of Materials for VOUT = 3.3V, Designed for 1A Output Current

Ref #	Value	Supplier	Part Number
C1	2.2 μ F 50V ceramic	TDK	C3225X7R1H225K
C2	22 μ F 63V electrolytic	Panasonic	EEEFK1J220XP
C3	10 nF 50V ceramic	TDK	C1608X7R1H103K
C4	120 μ F 6.3V 24mohm	Nippon Chemi-Con	APXE6R3ARA121ME61G
C5	Not populated	-	
C6	1 μ F 10V ceramic	TDK	C1608Y5V1A105Z
D1	60V 1A CMSH1-60	Central Semiconductor	CMSH1-60
L1	22 μ H 2.5A WE-PD L	Würth	744066220
		Coilcraft	MSS1038-223NLC
R1	976 Ω 1%	-	CRCW0603976RFKEA
R2	1.54 k Ω 1%	-	CRCW06031K54FKEA
R3	Not populated	-	
U1		National Semiconductor	LM22672MR-ADJ

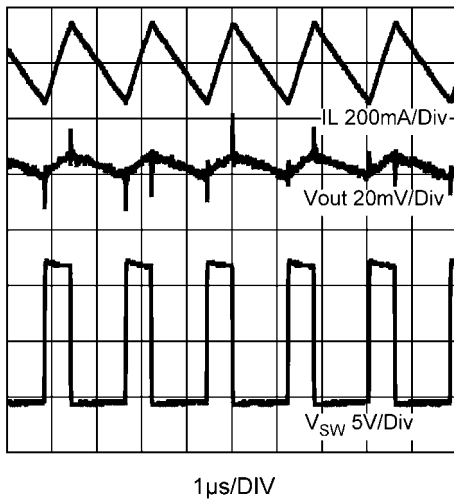
Performance Characteristics

Unless otherwise specified, $V_{IN} = 12V$, $T_A = 25^\circ C$.



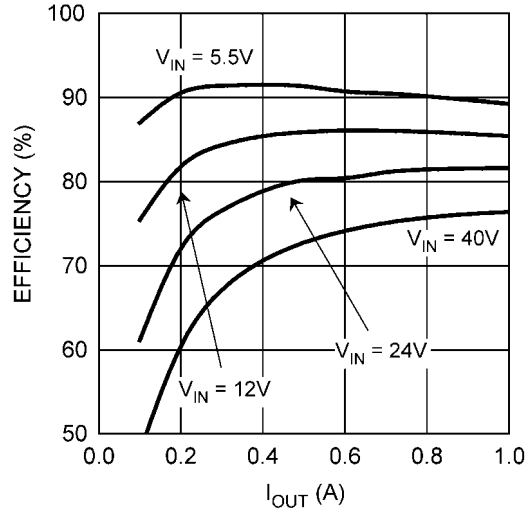
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FIGURE 2. Start-Up Waveforms
(Load Resistor = 3.3Ω)



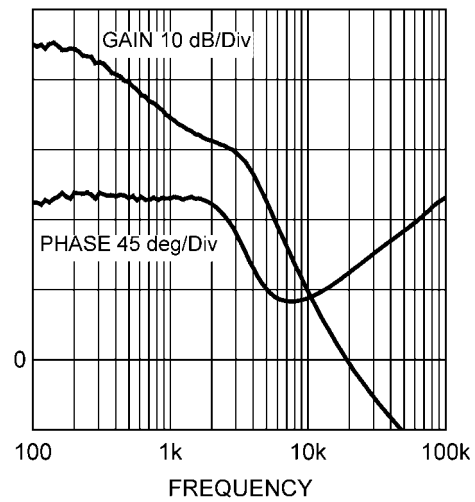
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FIGURE 3. Operation at 1A



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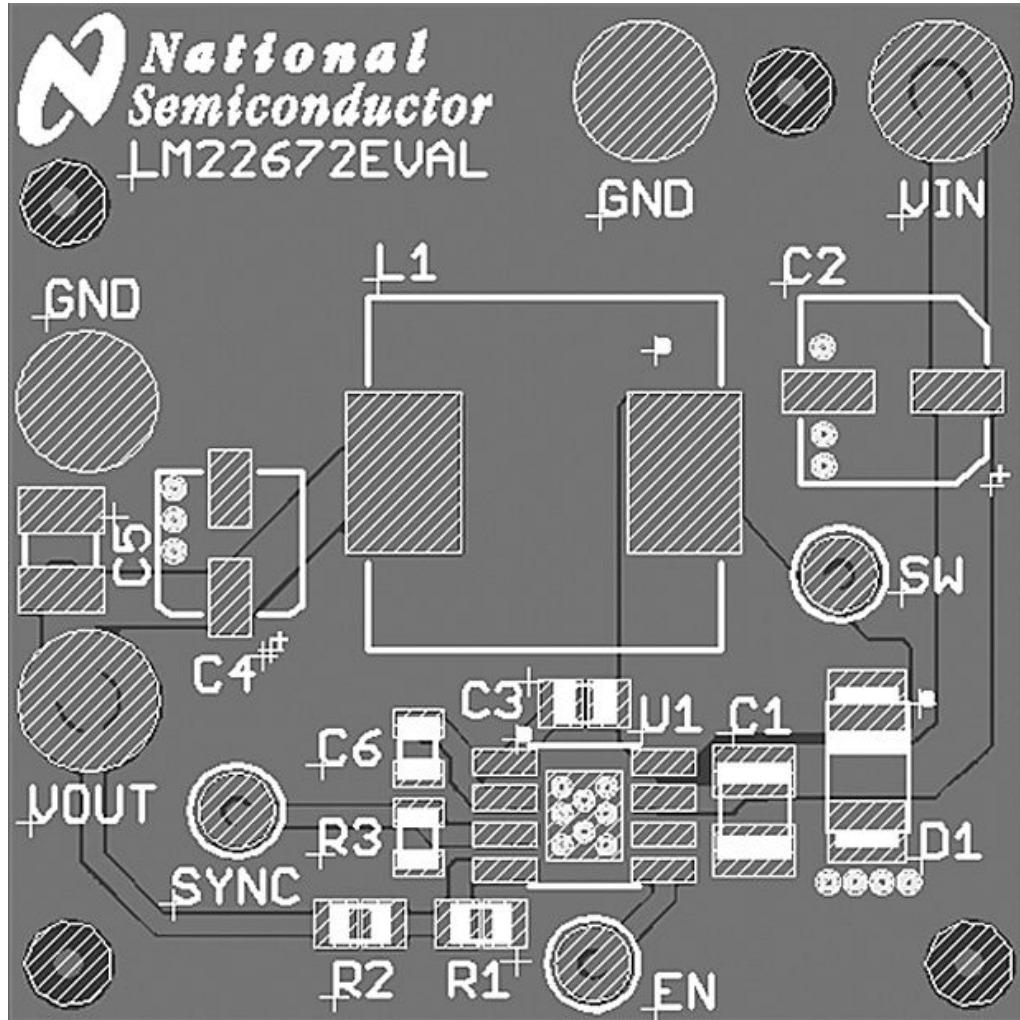
FIGURE 4. Efficiency vs I_{OUT}



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FIGURE 5. Overall Loop Gain and Phase ($I_{OUT} = 1A$)

PCB Layout Diagram



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FIGURE 6. Top Layer

Notes

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