AND8242/D

19 V, 3.0 A Universal Input AC-DC Adaptor Using NCP1271

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APPLICATION NOTE

INTRODUCTION

This application note presents an example circuit in Figure 1 using NCP1271 (65 kHz version) in the flyback topology with the design steps and measurement. The measurement shows that the 19 V, 3.0 A circuit delivers above 85% from universal input (85 to 265 Vac). The no load standby consumption is 83 mW at 230 Vac.

The NCP1271 is one of the latest fixed−frequency current−mode PWM switching controllers with (1) soft−skip standby operation for low−level audible noise (2) integrated high−voltage startup for saving PCB space and power (3) adjustable skip level to minimize standby power and (4) optional external latch protection features. Table 1 summarizes all features of an NCP1271 based power supply.

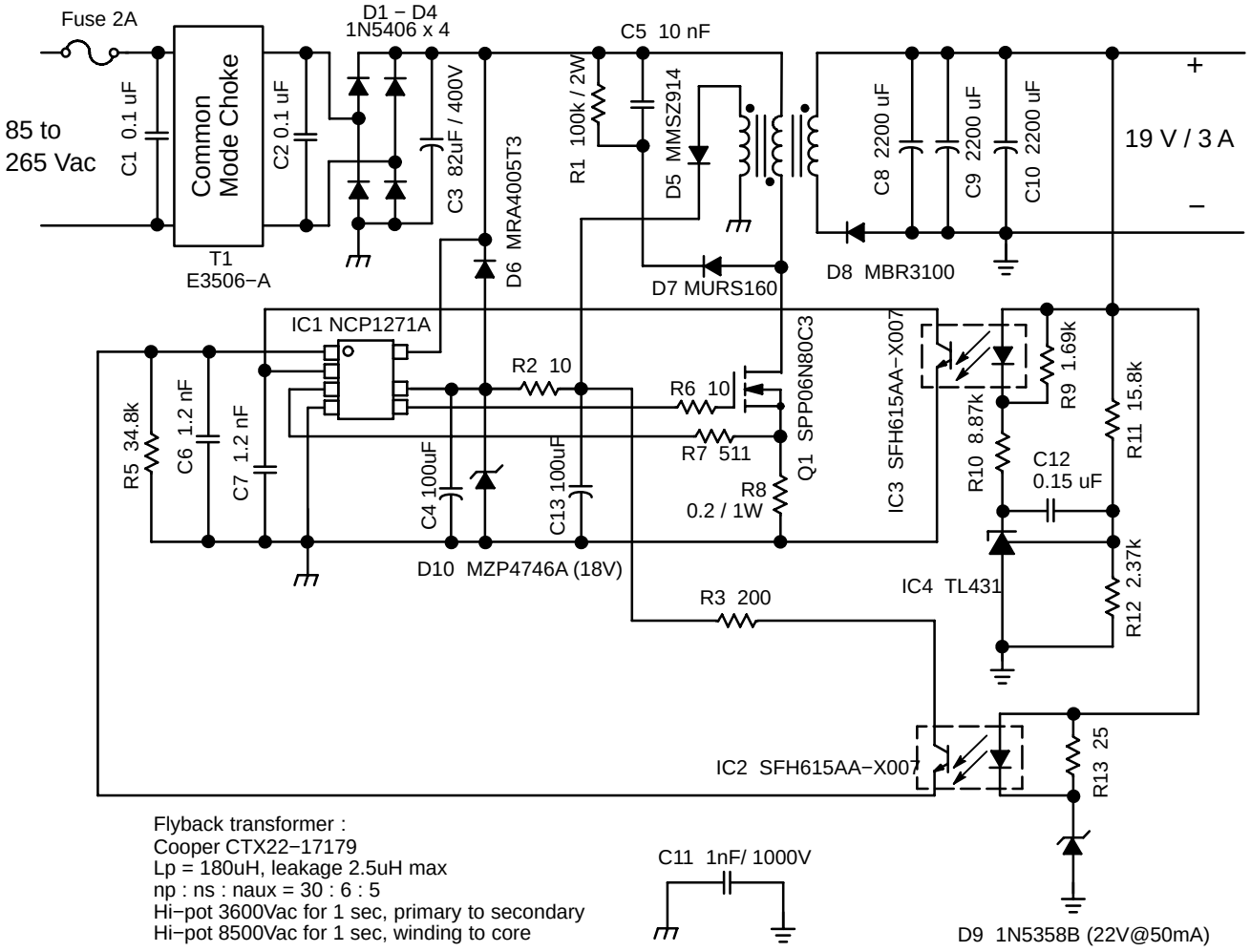

Figure 1. Application Circuit Schematic

Table 1. Features of Power Supply Using NCP1271

	Operation Mode	Features
Topology	CCM/DCM Flyback	• Fixed−frequency current−mode control/inherent primary current limitation. • Frequency jittering to soften EMI signature. • Adjustable skip duty (the borderline duty between skip operation and normal fixed−freq PWM operation). • Built−in soft−start. • Output short−circuit fault detection implemented by an internal timer that allows usage of bad coupling transformer. • Integrated high voltage startup that minimizes PCB spacing and loss.
Standby Condition	Soft−Skip Operation	• It offers excellent low standby power consumption. • It offers low level of low−frequency audible noise. • The soft−skip operation will be disabled if an abrupt transient load is applied from standby operation.
Fault Condition	Double Hiccup Restart	• It minimizes power dissipation in fault and allows auto−recovery ability when fault is cleared.
Latch Protection Activated	Latched Off	• V_{CC} stays above typical 5.8 V and PWM drive output remains off until circuit reset. • Reset needs the AC input unplugged.

Design Steps

Step 1. Define the Specification

Input	85 to 265 Vac, 50 Hz
Output	19 Vdc, 3.0 A, Isolated
Features	Excellent standby performance Output overvoltage protection latch

A Discontinuous Conduction Mode (DCM) flyback is the best choice here for (1) best stability and smallest inductor (i.e., fewer leakage inductance and smaller size), (2) few circuit components.

Step 2. Biasing the Controller

Due to the integrated high−voltage startup pin (Pin 8) of the NCP1271, the initial IC supply voltage, V_{CC}, can be obtained by connecting this pin to the high voltage DC source in Figure 2. In order to have extremely low standby power consumption, the bias supply voltage, V_{CC}, must be supplied by an external circuit that costs only one more output from the flyback.

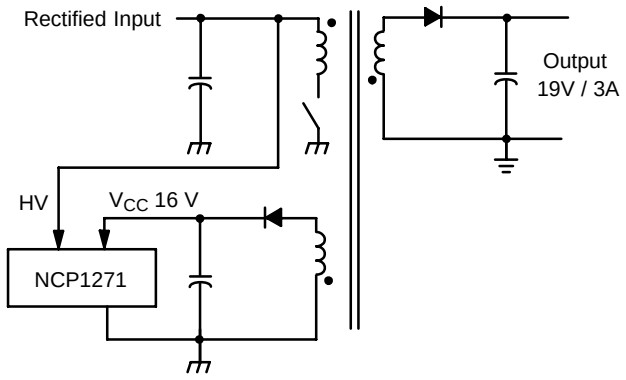

Figure 2. V_{CC} Biasing Scheme

The application range of the bias supply voltage V_{CC} of NCP1271 is from (10 V min) and (20 max). An 18 V clamping Zener is usually with ± 5% tolerance (i.e., 17.1 V min., 18.9 V max.). When the circuit is in standby mode, the main output voltage stays in high level because of no current consumption, but the bias supply voltage goes lower because of the consumption of the controller. Hence, the biasing voltage cannot be too low and it is selected as V_{CC} = 16 V. The 16 V bias supply voltage is made by a 6:5 turn ratio between the main output and auxiliary winding representing 19V:16V.

Step 3. Generic Flyback Calculation

The calculation can be made by the excel spreadsheet in (http://www.onsemi.com/pub/Collateral/NCP1271SHEET.XLS). This section describes the details.

Step 3a. Define the Flyback Basic Parameter

The flyback itself is a DC−to−DC converter. An estimated rectified input voltage to supply to the circuit is required. It is generally assumed that the rectified input voltages are from 100 to 400 V that covers the rectified universal AC input range.

$$V_{in(L)} = 100\ V$$

$$V_{in(H)} = 400\ V$$

With the output voltage V_{out} = 19 V and output diode drop V_d = 1.0 V.

The design here is using the 65 kHz version of NCP1271.

$$f = 65\ kHz$$

Step 3b. Define the Transformer Turn Ratio

The maximum allowable duty of the NCP1271 is (75% min, 85% max) and the skip duty (borderline duty between normal operation and skip mode operation) is externally adjustable. That is the design constraint in the transformer

turn ratio (n1/n2). The Continuous Conduction Mode (CCM) lossless flyback is with the following basic conversion equation.

$$\frac{V_{out} + V_d}{V_{in}} = \frac{n_2}{n_1}\frac{D}{1-D} \quad \text{(eq. 1)}$$

V_{in} is the input voltage. V_{out} is the output voltage. D is the duty ratio.

Rearrange the equation, it gives:

$$D = \frac{\frac{n_1}{n_2}(V_{out} + V_d)}{V_{in} + \frac{n_1}{n_2}(V_{out} + V_d)} \quad \text{(eq. 2)}$$

With the assumption that the primary−to−secondary turn ratio n_1/n_2 is 5. It gives 20% and 50% duty ratio at high and low line conditions respectively that are well within the allowable duty ratio constraint and the worst−case MOSFET and diode stress are acceptable.

$$n_1/n_2 = 5$$

$$D_{high\_line} = \frac{\frac{n_1}{n_2}(V_{out} + V_d)}{V_{in} + \frac{n_1}{n_2}(V_{out} + V_d)} = \frac{5 \cdot (19 + 1)}{400 + 5 \cdot (19 + 1)} = 20\% \quad \text{(eq. 3)}$$

$$D_{low\_line} = \frac{\frac{n_1}{n_2}(V_{out} + V_d)}{V_{in} + \frac{n_1}{n_2}(V_{out} + V_d)} = \frac{5 \cdot (19 + 1)}{100 + 5 \cdot (19 + 1)} = 50\% \quad \text{(eq. 4)}$$

$$V_{MOSFET} = V_{in} + \frac{n_1}{n_2}(V_{out} + V_d) = 400 + 5 \cdot (19 + 1) = 500\ V \quad \text{(eq. 5)}$$

$$V_{diode} = V_{out} + \frac{n_2}{n_1}V_{in} = 19 + \frac{1}{5} \cdot 400 = 99\ V \quad \text{(eq. 6)}$$

It is a trade−off here in picking the appropriate turn ratio. Lower the diode stress V_{diode} always comes with higher the MOSFET stress V_{MOSFET}. It is noted that the reflected MOSFET stress here excludes the consideration of the leakage inductance that will be covered later. The diode stress is a little bit close to 100 V limitation of MBR3100 but that is okay since 400 V input voltage will not exist in real application.

Step 3b. Define the Primary Current Limit

The primary current limit (or the peak current) I_{pk} directly limits the maximum power that the circuit can be transferred. In flyback topology, the input current is always discontinuous and it conducts when duty is on. Hence, the maximum input power with zero current ripple (infinity inductance) is 200 W at low line 100 V when I_{pk} = 4.0 A. That is the worst case. It is enough for the 57 W (19 V × 3.0 A) output power and the 200 W will be reduced when it goes to finite inductance and DCM later.

$$I_{pk} = 4.0\ A$$

$$P_{in(max)} = D \cdot V_{in} \cdot I_{pk} = 50\% \cdot 100 \cdot 4 = 200\ W$$

Step 3c. Define the Primary Inductance

The inductance L selection is based on the fundamental inductor equation V = L di/dt.

$$L_{high-line,\ CCM,\ lossless} = \frac{V_{in}D}{I_{pk}f} = \frac{400 \cdot 20\%}{4 \cdot 65 \times 10^3} = 307.7\ \mu H \quad \text{(eq. 7)}$$

$$L_{low-line,\ CCM,\ lossless} = \frac{V_{in}D}{I_{pk}f} = \frac{100 \cdot 50\%}{4 \cdot 65 \times 10^3} = 192.31\ \mu H \quad \text{(eq. 8)}$$

In order to have the circuit operate in DCM, the inductor is selected smaller than the above reference.

$$L = 180\ \mu H$$

Step 3d. DCM Parameter Study

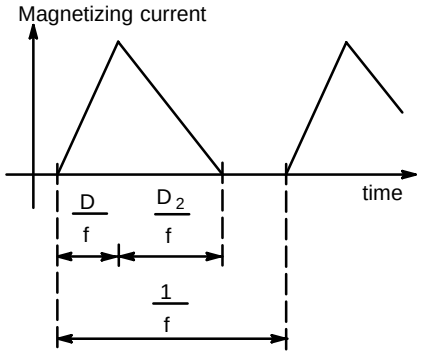

Figure 3. DCM Magnetizing Current

Based on the defined inductor L and peak current I_{pk}, the duty ratio D of the DCM operation can be obtained by the V = L di/dt equation again.

$$D_{high-line} = \frac{I_{pk}fL}{V_{in}} = \frac{4 \cdot 65 \times 10^3 \cdot 180 \times 10^{-6}}{400} = 11.7\% \quad \text{(eq. 9)}$$

$$D_{low-line} = \frac{I_{pk}fL}{V_{in}} = \frac{4 \cdot 65 \times 10^3 \cdot 180 \times 10^{-6}}{100} = 46.8\% \quad \text{(eq. 10)}$$

The equation of DCM flyback is:

$$\frac{V_{out}}{V_{in}} = \frac{n_2}{n_1}\frac{D}{D_2} \quad \text{(eq. 11)}$$

Based on this equation, the discharge duty D_2 is calculated.

$$D_{2-high-line} = \frac{V_{in}}{V_{out} + V_d}\frac{n_2}{n_1} \cdot D = \frac{400 \cdot 11.7\%}{(19 + 1) \cdot 5} = 46.8\% \quad \text{(eq. 12)}$$

$$D_{2-low-line} = \frac{V_{in}}{V_{out} + V_d}\frac{n_2}{n_1} \cdot D = \frac{100 \cdot 46.8\%}{(19 + 1) \cdot 5} = 46.8\% \quad \text{(eq. 13)}$$

Hence, the DCM operation is confirmed here for $D + D_2 < 100\%$.

In an energy perspective, the total maximum input power in DCM is 93.6 W. That is more than enough (at 57 W/93.6 W = 60.9% efficiency) to deliver the required output power of 3.0 A × 19 V = 57 W.

$$P_{in} = \frac{1}{2}LI^2f = \frac{1}{2} \cdot 180 \times 10^{-6} \cdot 4^2 \cdot 65 \times 10^3 = 93.6\ W \quad \text{(eq. 14)}$$

Step 3e. Snubber Calculation

The objective of flyback snubber is to limit the transient voltage stress on the MOSFET because of transformer leakage inductance. Hence, the calculation starts with the leakage inductance. From the transformer specification, the maximum leakage inductance is 2.5 μH. When the leakage inductance is charged with the peak current 4.0 A, the maximum possible power to be stored there is 1.3 W.

$$P_{snubber} = \frac{1}{2} \cdot L_{leakage} \cdot I_{pk}^2 \cdot f = \frac{1}{2} \cdot 2.5 \times 10^{-6} \cdot 4^2 \cdot 65 \times 10^3 = 1.3\ W \quad \text{(eq. 15)}$$

If a 2−Watt 100 kΩ snubber resistor is used to dissipate this 1.3 W, the voltage across this snubber resistor will be 360.6 V.

$$P_{snubber} = \frac{V_{snubber}^2}{R_{snubber}} \quad \text{(eq. 16)}$$

$$V_{snubber} = \sqrt{P_{snubber} \cdot R_{snubber}} = \sqrt{1.3 \cdot 100 \times 10^3} = 360.6\ V \quad \text{(eq. 17)}$$

Thus, the maximum MOSFET stress due to the leakage inductance will be 400 + 360.6 = 760.6 V and it is under the 800 V maximum allowable limit.

The minimum capacitor to deliver this power will be 307 pF. A 10 nF capacitor is used here.

$$P_{snubber} \le \frac{1}{2} \cdot C_{snubber} \cdot V_{snubber}^2 \cdot f \quad \text{(eq. 18)}$$

$$C_{snubber} \ge \frac{2 \cdot P_{snubber}}{V_{snubber}^2 \cdot f} = \frac{2 \cdot 1.3}{360.6^2 \cdot 65 \times 10^3} = 307\ pF \quad \text{(eq. 19)}$$

Step 4. Special Setting on NCP1271 Circuit

This section describes how to set the circuit parameter in the circuit using NCP1271.

Step 4a. Optional Output OVP Latch

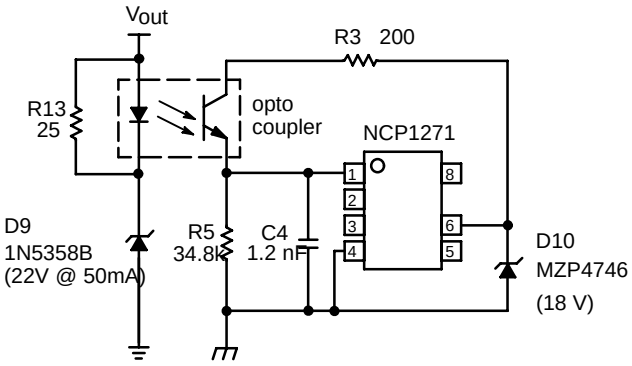

Figure 4. Output Overvoltage Protection Scheme

Figure 4 shows the output overvoltage protection (OVP) latch circuit. When output voltage is too high, a current from the optocoupler pulls high the latch pin (Pin 1) voltage and eventually latches off the controller.

In implementation, the Zener diode, D9 1N5358B, has a leakage current 50 mA at 22 V. It means that there is an up−to−50−mA current flowing through the Zener when the biasing voltage is somewhere below 22 V. This leakage current can let the optocoupler conducts and triggers the OVP latch even if the voltage is below the OVP threshold. In order to prevent it, a R13 resistor is added to bypass the leakage current. The typical optocoupler diode forward voltage drop is 1.25 V and the value of R13 is 1.25 V ÷ 50 mA = 25 Ω. Hence, the OVP threshold includes the Zener biasing voltage 22 V (with ±5% tolerance) and the optocoupler input diode forward bias voltage (1.25 V typical). As long as it is lower than the 25 V rating of the output capacitor, it's fine.

The latch threshold is 8.0 V. When Pin 1 is opened for default 1.0 V skip level, the Pin 1 voltage is tied to the internal bias voltage of the NCP1271. That is typically 6.5 V. When a R5 34.8 kΩ skip resistor is used, the nominal Pin 1 voltage goes down to 34.8 kΩ × 43 μA = 1.5 V. Hence, it is always recommended to put a skip resistor on Pin 1 to make sure that there is a good margin between the 8.0 V latch threshold and the nominal Pin 1 voltage to prevent fault triggering due to noise or leakage current from the latch protection circuit.

In addition, an nF−order capacitor is generally added to the latch protection pin to increase noise immunity there. In order to pull the Pin 1 voltage above the 8.0 V (typical) latch threshold, a greater−than−8.0−V source is needed. That is

usually the bias supply voltage V_{CC}. Hence, the optocoupler is connected to the V_{CC} source that can be as high as 18 V (±5%). In order to protect Pin 1, a 200 Ω is connected to limit the current below the maximum allowed 100 mA. In addition, an internal ESD diode will limit the maximum voltage on Pin 1 in 10 V without damage.

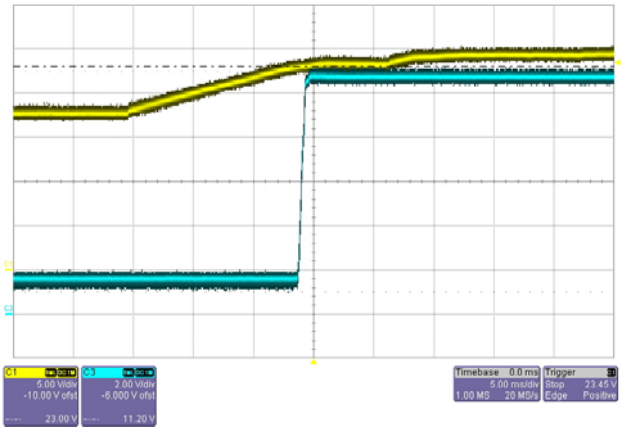

Figure 5. Output OVP Testing

Figure 5 shows how the Pin 1 voltage reacts when the output voltage is connected to a 24 V source. It can be seen that the voltage jumps up and clamps to 10.5 V from the nominal 1.5 V (34.8 kΩ × 43 μA) when the output voltage is over 23 V typically. Once the voltage is over the 8.0 V latch threshold, the circuit goes latch off.

Step 4b Skipping Adjustment

The skip resistor, R5, provides two functions: (1) the setting of the skip duty that the borderline duty between the normal and skipping operation; (2) and the optimization of the standby power consumption; (3) and indirectly increase the latch−off immunity by lowering the Pin 1 voltage. Due to the soft−skip mode standby operation. The low−frequency audible noise is not a critical issue here. Basically, the skip level (or skip duty) is set to be as high as possible because higher value can save more power by allowing more skipping period during standby. The skip−level upper limit is limited by the skip duty of the flyback, because it is not desirable to enter skip mode operation in full load or nominal condition.

When R5 = 34.8 kΩ, the skip level is R_{skip} = 0.338 V that corresponds to skip duty D_{skip} = 9%. The 9% skip duty is below the nominal operating duty range (11.7% to 46.8% in Step 3d) and hence the circuit does not skip in full load or nominal condition.

$$V_{skip} = (R_{skip} I_{skip} - 1.25\ V)/0.73 = 0.338\ V \quad \text{(eq. 20)}$$

$$D_{skip} = \frac{V_{skip}}{3\ V} \cdot D_{max} = \frac{0.338}{3} \cdot 80\% = 9\% \quad \text{(eq. 21)}$$

Step 4c. Maximum Primary Current Setting

Current sense resistor, R8, provides two functions: (1) current sensing for current−mode operation; (2)and the maximum primary current limitation. When the voltage exceeds 1.0 V, the PWM output goes low because of overcurrent condition. When R8 = 0.2 Ω, the maximum allowable current is 5.0 A that is greater than the required 4.0 A in Step 3b.

$$I_{D,max} = \frac{1\ V}{R_{CS}} = \frac{1\ V}{0.2\ \Omega} = 5\ A > 4\ A \quad \text{(eq. 22)}$$

Step 4d. Maximum Allowable Duty Setting and Stability/Transient Response

The ramp resistor, R7, provides two functions: (1) compensation ramp function in current−mode operation; (2) and reduce the maximum duty when it is above 10 kΩ.

Higher ramp resistor value means more compensation ramp in the modulation. It also means the modulation method becomes more voltage−mode (or voltage−loop depended) and less current−mode (or current−loop depended). It results in slower transient response, but better stability. If better transient response is wanted, more current−mode modulation is needed, and the ramp resistor value is low that makes higher loop gain. On the other hand, if better stability is wanted, fewer current−mode modulation is needed and the ramp resistor is high that makes slow voltage−loop response but better stability. Figures 6 and 7 shows the transient response of the circuit recovering from standby (output current = 0 A) to full load (output current = 3.0 A) with different values of R7. The output current is 1.0 A/div changing from 0 A to 3.0 A in green color. The output voltages are AC−coupled, 200 mV/div, and 2.0 V/div respectively. The input voltage is 110 Vac. It shows that the transient response with low ramp resistor, R7, value is better. Figures 6 and 7 also explain why the ramp resistor is below 10 kΩ because the transient can be bad otherwise.

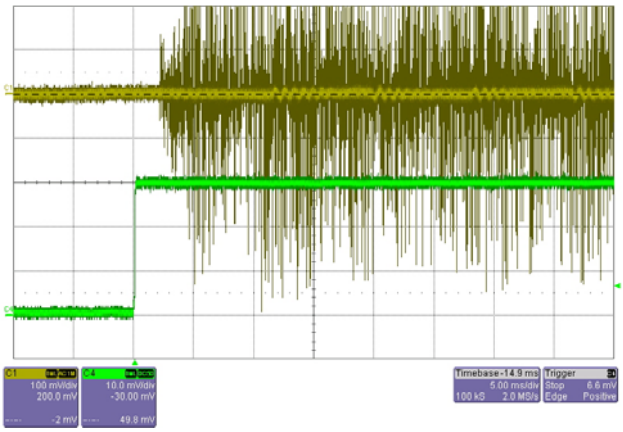

Figure 6. Transient Response with R7 = 511 Ω

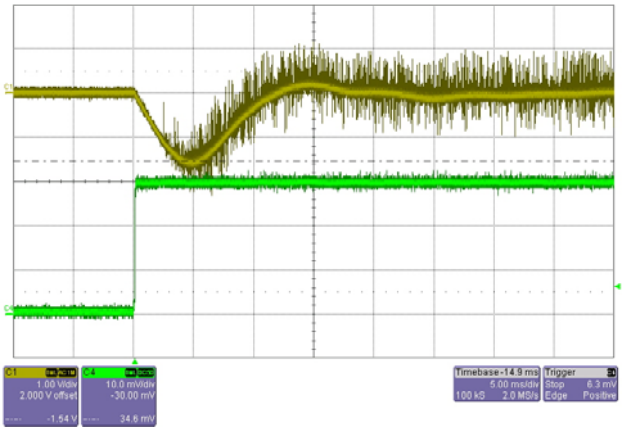

Figure 7. Transient Response with R7 = 2.0 kΩ

The maximum allowable duty is 80% when ramp resistor, R7, is smaller than 10 kΩ. Now that R7 = 511 Ω and the maximum allowable duty is 80% that covers the operating duty (11.7% to 46.8% in Step 3d).

Step 4e. HV−Vcc Reverse Diode

The diode, D6, is a standard protection of the HV pin (Pin 8). When the main power is interrupted in application, the HV pin voltage may potentially go negative in a short transient period. It creates a reverse current that goes out of the HV pin and the current can damage the device. The inserted diode turns on when the HV pin voltage goes below the V_{CC} biasing voltage, and hence eliminate the chance of negative voltage on the HV pin or the reverse current.

Step 4f. Decoupling Capacitors

There are three pins in the NCP1271 that may need external decoupling capacitors.

1. Skip/latch pin (Pin 1) – If the voltage on this pin is above 8.0 V, the circuit goes latch off. Hence, a decoupling capacitor on this pin is essential to increase noise immunity there.
2. Feedback pin (Pin 2) – In order to save current consumption, the feedback pin sinking current in μA−order is very easy to get polluted in a noisy switch−mode power−supply environment and the circuit operation may be affected.
3. V_{CC} pin (Pin 6) – The NCP1271 maintains normal operation when V_{CC} is above $V_{CC(off)}$ (9.1 V typical). If V_{CC} drops below $V_{CC(off)}$ by switching noise, the circuit wrongly recognizes it as a fault condition. Hence, it is important to locate the V_{CC} capacitor or additional decoupling capacitor as close as possible to the NCP1271.

Step 5. Auxiliary Supply

Figure 8 shows the auxiliary supply circuit. There is a resistor to increase flexibility to further redesign the circuit for other higher output voltage by dumping the extra bias supply voltage across the resistor.

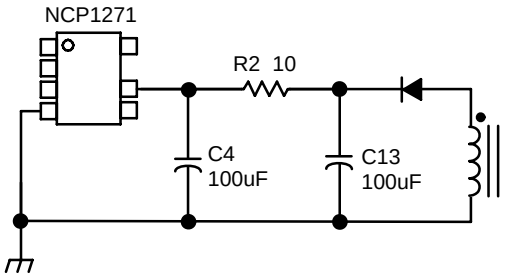

Figure 8. Auxiliary Supply

Step 6. Layout Consideration

Figures 9−10 show the layout of the design. It is a single−layer PCB. R4 is a cancelled component in order to save some extra standby power consumption. The major concerns are the following.

1. To minimize the high−current loop and locate the IC controller outside the high−current loop to prevent malfunction of the IC internal logic due to strong magnetic field from the high current.
2. To locate the decoupling capacitors closely to the device to improve noise immunity.
3. To locate the V_{CC} capacitor very close to the device to prevent the circuit enter fault condition because of noise.
4. To locate the output voltage sense resistor closely to the output load points.
5. To minimize the current sense trace that is low−impedance and easily polluted.
6. To minimize the distance between the feedback opto coupler and controller because the trace is easily polluted.
7. To minimize the distance between the MOSFET and controller because the PCB trace is high frequency and high current that it can easily pollute other part of the circuit.

It can be observed that the electrolytic through−hole Vcc capacitor is located exactly on the top side where the SO−7 controller is located on the bottom side. That minimizes the Vcc pin noise that may potential lead the controller to fault condition.

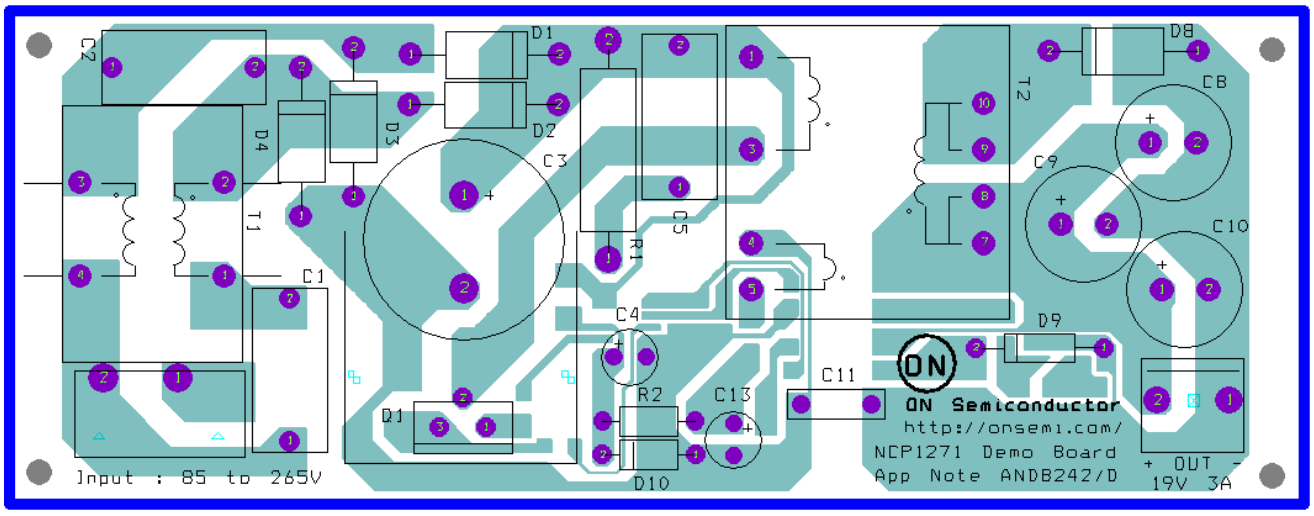

Figure 9. Top View

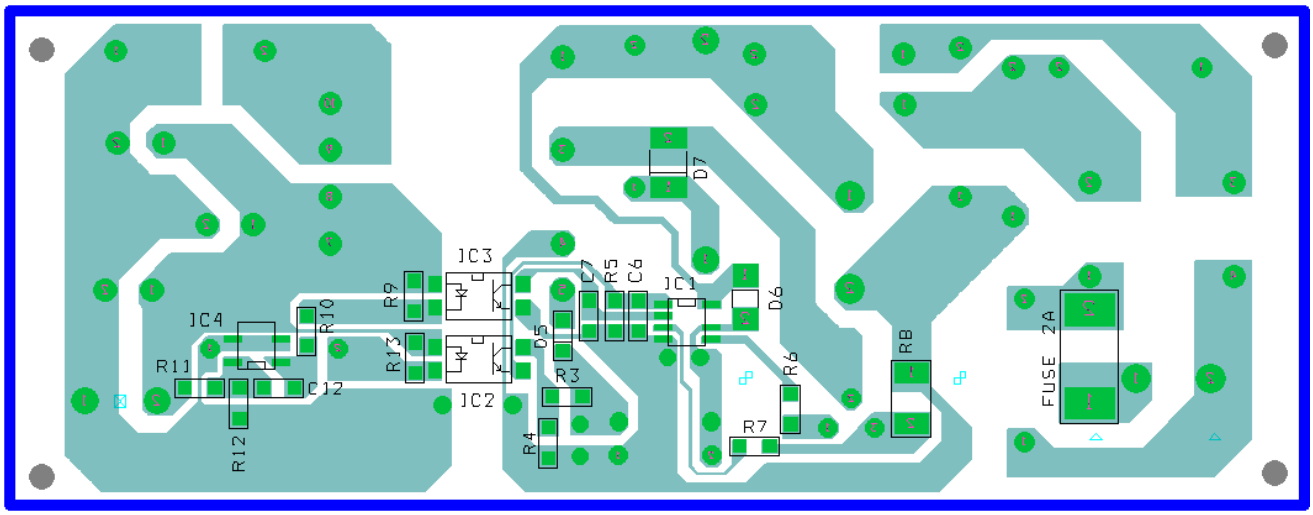

Figure 10. Bottom View

Measurement

Part I. Standby Performance

The circuit offers excellent no load standby performance. The 230−Vac power consumption of the 57 W circuit is 83 mW. When input is 230 Vac and output is 503 mW (19.13 V × 26.3 mA), the input power is 710 mW.

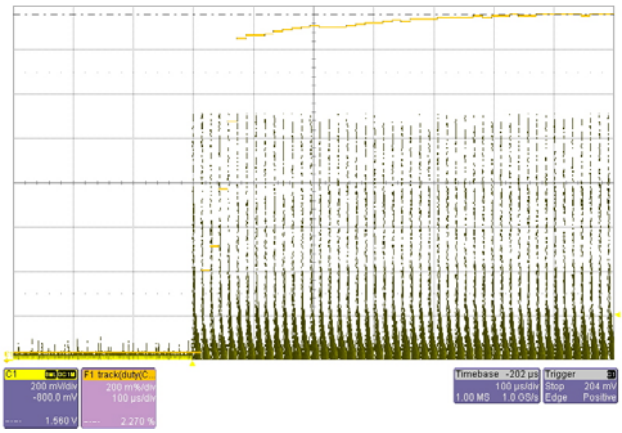

Figure 11. Standby Pulse

Figure 11 shows a typical soft−skip pulse train during the standby operation. The yellow trace is the CS pin (Pin 3) voltage at 200 mV/div. The orange trace shows the duty that comes from 0% to 2.27%. The figure shows that the soft−skip time is not effectively 300 μs. In the figure, the first five switching cycles, for about 80 μs, are in a soft−skip period where the duty is gradually increasing. Then, the duty follows the feedback voltage variation because the soft−skip reference voltage is higher than the divided−by−3 feedback voltage. It is described in Figure 34 of the data sheet.

Part II. Normal Operation

Table 2 shows the full load efficiency of the circuit is above 85%.

Table 2. Normal Operation Performance

Input	Output	Efficiency
85 Vac 66.4 W	19 V 3.0 A	85.8%
110 Vac 65.4 W	19 V 3.0 A	87.2%
120 Vac 65.4 W	19 V 3.0 A	87.2%
180 Vac 65.2 W	19 V 3.0 A	87.4%
220 Vac 65.2 W	19 V 3.0 A	87.4%
230 Vac 65.2 W	19 V 3.0 A	87.4%
265 Vac 65.2 W	19 V 3.0 A	87.4%

Part III. Dynamic Study

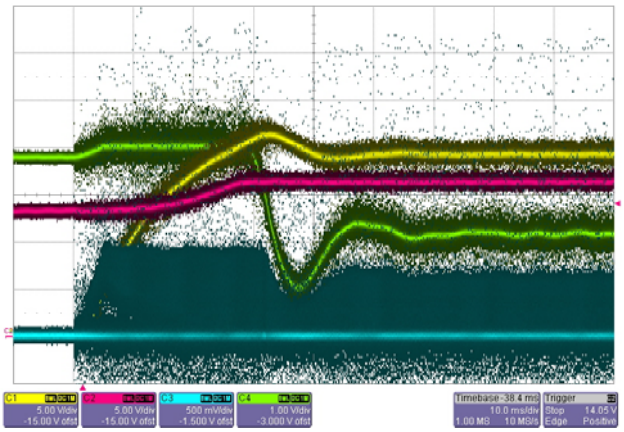

Figure 12. Startup Transient

Figure 12 shows the startup transient waveforms of the circuit when input is 110 Vac. Looking from the top right side, the yellow trace is the output voltage in 5.0 V/div. The red trace is the V_{CC} voltage in 5.0 V/div. The green trace is the feedback pin voltage in 1.0 V/div. The blue trace is the voltage across current sense resistor R8 in 500 mV/div representing the drain current. The waveforms are captured when V_{CC} reaches $V_{CC(on)}$ (i.e., red trace reaches 12.6 V). A beginning 5.0 ms soft−start is observed in the drain current. The green trace V_{FB} drops below 3.0 V after 32 ms that is shorter than the 130 ms fault validation time and hence the circuit does not enter fault condition and able to maintain in the normal operation condition.

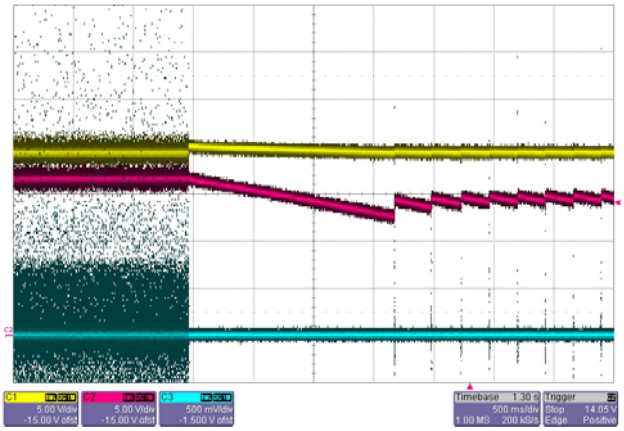

Figure 13. Operating to Standby

Figure 13 shows the go−to−standby transition from full load operation. The output voltage does not consume current and remains at 19 V, but the V_{CC} voltage drops from 16 V to 15 V because the V_{CC} auxiliary winding still supplies current to the controller. The minimum V_{CC} voltage in the transition can be 12 V. That explains why the 16 V biasing voltage is selected and a pair of 100 μF V_{CC} capacitor is needed to maintain V_{CC} above $V_{CC(off)}$ (9.1 V typical) in order to prevent V_{CC} reset.

Conclusion

A 19 V/3.0 A flyback circuit using NCP1271 is presented. Because of the PWM controller, NCP1271, the circuit offers low−audible−noise soft−skip mode operation, excellent standby performance, and output overvoltage protection latch. The design consideration of most components in the design is explained. The design procedure is also summarized in an excel spreadsheet in http://www.onsemi.com. When design with the NCP1271, special care on (1) locate a decoupling capacitor on the latch/skip pin (Pin 1) in order to prevent fault latchoff due to noise and (2) locate the Vcc capacitor very close to the controller in order to prevent entering fault condition due to noise.

Appendix I. Bill of Material for the NCP1271 19 V/3.0 A Example Circuit

Designator	Qty	Part Number	Description	Manufacturer
T1	1	E3506−A	3.0 A 508 μH Common−Mode Filter	Coilcraft
T2	1	CTX22−17179	Custom Transformer 180 μH 30:6:5, 2.5 μH Max Leakage	Cooper/Coiltronics
IC1	1	NCP1271D65R2	65 kHz Flyback PWM Controller, SO−7	ON Semiconductor
IC2	1	TL431AID	2.5 V 1% Voltage Reference, SO−8	ON Semiconductor
IC3–IC4	2	SFH615AA−X007	Optocoupler	Vishay
D1–D4	4	1N5406	3.0 A 600 V Diode, Axial 267−05	ON Semiconductor
D5	1	MMSZ914	1.0 A 100 V Diode, SOD−123	ON Semiconductor
D6	1	MRA4005T3	1.0 A 600 V Diode, SMA	ON Semiconductor
D7	1	MURS160	1.0 A 600 V Diode, SMB	ON Semiconductor
D8	1	MBR3100	3.0 A 100 V Schottky Diode, Axial 267−05	ON Semiconductor
D9	1	1N5358B	22 V @ 50 mA Zener Diode	ON Semiconductor
D10	1	MZP4746A	18 V @ 14 mA Zener Diode	ON Semiconductor
Q1	1	SPP06N80C3	6.0 A 800 V N−MOSFET, TO−220AB	Infineon
R1	1	P100KW−2BK	100 kΩ 2.0 W, Axial 5%	Digi−key
R2	1	CFR−25JB−10R	10 Ω, 1/4 W Axial	Yageo
R3	1	CRCW12062000F	200 Ω, 1206	Vishay
R4	1	(Deleted)	N/A	N/A
R5	1	CRCW12063482F	34.8 kΩ, 1206	Vishay
R6	1	CRCW120610R0F	10 Ω, 1206	Vishay
R7	1	CRCW12065110F	511 Ω 1206	Vishay
R8	1	WSL2512R2000FEA	0.2 Ω 1.0 W 1%	Vishay
R9	1	CRCW12061691F	1.69 kΩ, 1206	Vishay
R10	1	CRCW12061502F	15 kΩ, 1206	Vishay
R11	1	CRCW12061582F	15.8 kΩ, 1206	Vishay
R12	1	CRCW12062371F	2.37 kΩ, 1206	Vishay
R13	1	CRCW120624R9F	24.9 Ω, 1206	Vishay
C1−C2	2	PHE840MA6100MA04	0.1 μF X2 Cap 10 mm Pitch	Evox Rifa
C3	1	ECOS2GP820BA, EETED2G820BA, or EETXB2G820BA	82 μF 400 V Electrolytic	Panasonic
C4, C13	2	ECA1EM101	100 μF 25 V Electrolytic	Panasonic
C5	1	630MMB103J	10 nF 630 V Film Cap	Rubycon
C6−C7	1	VJ1206Y122KXXA	1.2 nF 25 V, 1206	Vishay
C8–C10	3	025YXG220M12.5X30	2200 μF 25 V Electrolytic	Rubycon
C11	1	ERO610RJ4100M	1.0 nF 1.0 kV 5.0 mm Pitch Y2 Cap	Evox Rifa
C12	1	VJ1206Y154KXXA	0.15 μF 25 V Ceramic	Vishay
Fuse	1	1025TD2−R	250 V 2.0 A Tie Delay Fuse	Cooper Fuse
Heatsink	1	590302B03600	Heatsink for TO−220 Package	Aavid
Heatsink Insulation	1	4672	TO−220 Mica Insulation	Keystone
AC Connector	1	770W−X2/10	IEC60320 C8 Connector	Qualtek
DC Connector	1	26−60−4030 or 009652038	3−Terminal 3.96 mm Pitch Male Header	Molex
Standoff	4	4804 K	Standoff M/F Hex 4−40 Nyl 0.750”	Digi−key
Heatsink Mechanic	1	30F698	4−40 1/4 Inch Screw	Newark
Heatsink/Standoff Mechanic	5	31F2106	4−40 Screw Nuts	Newark

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