Test Procedure for the NCP5425 Single Output Evaluation Board

ON Semiconductor®

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1.0 Diagrams

1.1 Test Configuration

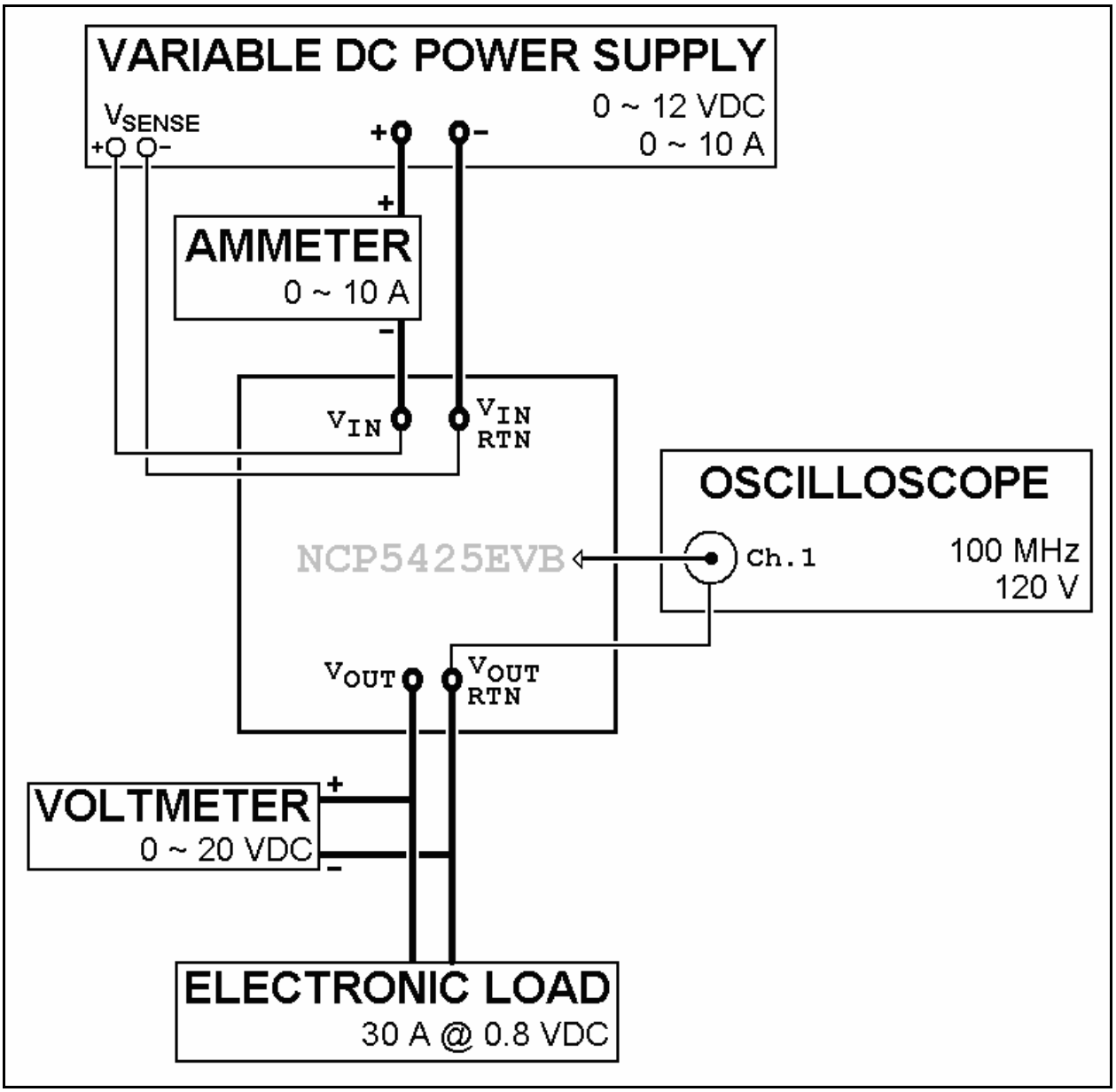

Figure 1. NCP5425EVB Single Output Test Configuration.

1.2 Test Points

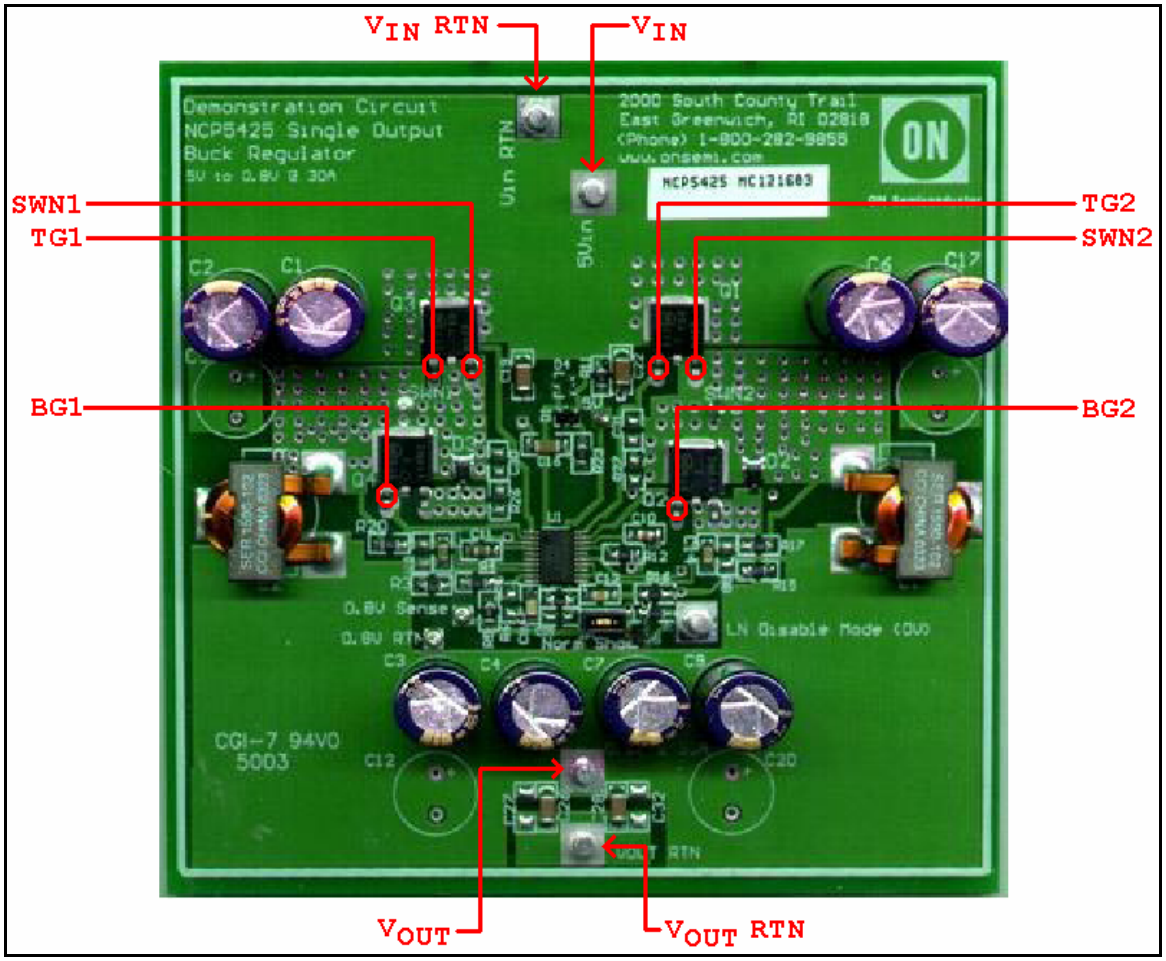

Figure 2. NCP5425EVB Single Output Test Points.

2.0 Equipment

- Variable DC power supply (0 ~ 12 V_{DC}, 10 A)
- Ammeter (0 ~ 10 A)
- Voltmeter (0 ~ 20 V_{DC})
- Electronic Load (capable of sinking 310 A at 0.8 V_{DC})
  OR
  Resistive Load (0.027 Ω, 30 W)
- Oscilloscope (100 MHz, 120 V)

3.0 Procedure

3.1 Configure equipment as shown in Figure 1.

3.2 With no load connected, set supply current limit to 1.0 A. Increase supply voltage to 5.0 V, and verify that V_{OUT} = 0.8 V ±5.0%.

3.3 Increase supply current limit to 8.0 A. Apply full 30 A load. Verify again that V_{OUT} = 0.8 V ±5.0%.

3.4 Probe test points SWN1, TG1, BG1, SWN2, TG2, and BG2 with oscilloscope. Verify that the switching frequency is 224 – 376 kHz and that there is no excessive jitter.

3.5 Remove load. Briefly short V_{OUT} to V_{OUT} RTN. Verify that input current does not exceed 8.0 A and that output returns to regulation when short is removed.

4.0 Notes

4.1 The board should not produce audible noise during normal operation.

4.2 A parallel array of high-power resistors is recommended as a test load.