# Evaluation Board for PWM, Step-Down DC-to-DC Controller with Margining and Tracking

# EVAL-ADP1822

## INTRODUCTION

This data sheet describes the design, operation, and test of the ADP1822 standard evaluation board. In all tests, the board is operated from an input voltage range of 9 V to 15 V, and generates up to 10 A at $V_{OUT}$ = 1.8 V. The switching frequency is fixed at 300 kHz.

## GENERAL DESCRIPTION

The ADP1822 is a versatile and inexpensive synchronous buck PWM controller. The converter power input voltage range is 1 V to 24 V, while the ADP1822 controller is specified from 3.0 V to 5.5 V. The ADP1822 free-running frequency is logic-selectable at either 300 kHz or 600 kHz. Alternatively, it can be synchronized to an external clock at any frequency between 300 kHz and 1.2 MHz. The internal gate drivers control an all N-channel power stage to regulate a converter output voltage as low as 0.6 V with up to 20 A load current.

The regulated output of the ADP1822 can track another power supply and be dynamically adjusted up or down with the margining control inputs of the controller.

The ADP1822 includes an adjustable soft start to limit input inrush current and to facilitate sequencing. It provides current-limit and short-circuit protection, and a power-good logic output.

The ADP1822 is well suited for a wide range of power applications, such as DSP and processor core power in telecommunications, medical imaging, high performance servers, and industrial applications.

## SPECIFICATIONS

**Table 1. Evaluation Board Specifications**

| Description | Parameter |
|---|---|
| $V_{IN}$ | 12 V |
| $V_{OUT}$ | 1.8 V |
| Frequency | 300 kHz |
| Maximum $I_{OUT}$ | 10 A |
| Current Limit | 15 A |
| High and Low Voltage Margining | 5% |

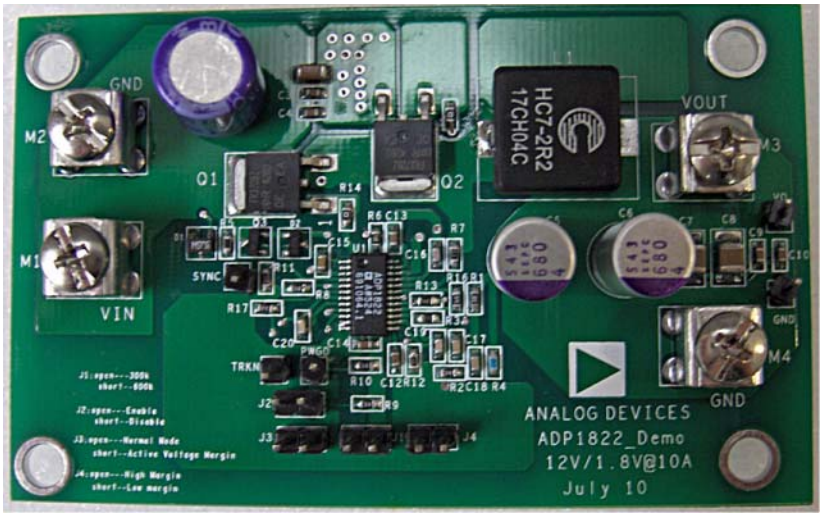


*Figure 1. ADP1822 Evaluation Board*



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## REVISION HISTORY

**11/06—Revision 0: Initial Version**

# TEST INSTRUCTIONS

Test instructions:

1. Make sure that Jumper 2 is open. Power on the board (output voltage is at 1.8 V).
2. If Jumper 1 is shorted, replace the inductor to another value to fit 600 kHz operation.
3. If Jumper 3 is shorted, the output high margining is at 1.89 V. If Jumper 4 is open, the output low margining is at 1.71 V.
4. Verify the output voltage tracking features when connecting the external generator to the TRKN point.
5. Use the PWGD point for monitoring operation behavior.

**Table 2. Jumper and Connector Descriptions**

| Name | Description | Default Status |
|---|---|---|
| M1 | $V_{IN}$ | |
| M2 | GND In | |
| M3 | $V_{IN}$ | |
| M4 | GND Out | |
| Jumper 1 | Open: 300 kHz<br>Short: 600 kHz | Open |
| Jumper 2 | Open: enable the board<br>Short: disable the board | Open |
| Jumper 3 | Open: output voltage normal mode.<br>Short: active voltage margin | Open |
| Jumper 4 | Open: high margin<br>Short: low margin | Open |

**Table 3. Margining Description**

| MAR | MSEL | Voltage Margin |
|---|---|---|
| Low (Jumper 3 open) | X | None |
| High (Jumper 3 shorted) | High (Jumper 4 open) | High margin (FB connected to MUP) |
| High (Jumper 3 shorted) | Low (Jumper 4 shorted) | Low margin (FB connected to MDN) |

# COMPONENT SELECTION

## INPUT CAPACITOR

In continuous mode, the source current of the high-side MOSFET is a square wave of duty cycle $V_{OUT}/V_{IN}$. To prevent large voltage transients, use a low ESR input capacitor sized for the maximum rms current. The maximum rms capacitor current is given by $I_L\sqrt{D(1-D)}$

## OUTPUT INDUCTOR

In high switching applications, if the inductor is too big, the dI/dt is too low and cannot respond to load changes quickly. If the inductor is too small, the output ripple would be high. Therefore, if good transient response is needed, smaller inductors and larger capacitors are better, within the constraint of the maximum allowed ripple current in the capacitor and the maximum dissipation of the core (core temperature).

The output inductor can be chosen according to the following equation:

$$L = \frac{V_{OUT}}{I_{OUT} K_{CR} f_{SW}}(1 - D) \quad (1)$$

where:

$V_{OUT}$ is the output voltage.
$I_{OUT}$ is the rated output current.
$K_{CR}$ is the ratio of current ripple, $\Delta I_L/I_O$.
$f_{SW}$ is the switching frequency.
$D$ is the duty cycle

Generally, $K_{cr}$ should be chosen around 20% ~ 40%.

## OUTPUT CAPACITOR

The selection of $C_{OUT}$ is determined by the ESR and the capacitance. The output voltage ripple can be approximated as

$$\Delta V_{OUT} = \Delta I_L \left( ESR + \frac{1}{8 f_{SW} C_{OUT}} \right) \quad (2)$$

Generally, the voltage ripple caused by the capacitance or ESR depends on the capacitor chosen.

ESR affects the output voltage ripple; thus, an MLCC capacitor is recommended because of its low ESR.

During a load transient on the output, the amount of capacitance needed is determined by the maximum energy stored in the inductor. The capacitance must be sufficient to absorb the change in inductor current when a high current to low current transition occurs and to supply the load when a low current to high current transition occurs.

$$C_{OUT,min1} = \frac{\Delta I_{OUT}{}^2 L}{2 V_{OUT} \Delta V_{up}} \quad (3)$$

$$C_{OUT,min2} = \frac{\Delta I_{OUT}{}^2 L}{2(V_{IN} - V_{OUT}) \Delta V_{down}} \quad (4)$$

where:

$\Delta I_{OUT}$ is the step load.
$\Delta V_{up}$ is the output voltage overshoot when the load is stepped down.
$\Delta V_{down}$ is the output voltage overshoot when the load is stepped up.
$V_{IN}$ is the input voltage.
$C_{OUT,min1}$ is the minimum capacitance according to the overshoot voltage $\Delta V_{up}$.
$C_{OUT,min2}$ is the minimum capacitance according to the overshoot voltage $\Delta V_{down}$.

Select an output capacitance that is greater than both $C_{OUT, min1}$ and $C_{OUT, min2}$.

Make sure that the ripple current rating of the output capacitors is greater than the following current:

$$I_{COUT} = \sqrt{\frac{\Delta I_L{}^2}{12}} \quad (5)$$

## MOSFET SELECTION

The choice of MOSFET directly affects the dc-to-dc converter performance. The MOSFET must have low on resistance ($R_{DSON}$) to reduce the conduction loss, and low gate charge to reduce switching loss.

For the low-side (synchronous) MOSFET, the dominant loss is the conduction loss. It can be calculated as

$$P_{C,low} = (1 - D)\left( I_{OUT}{}^2 + \frac{\Delta I_L{}^2}{12} \right) R_{DSON} \quad (6)$$

The gate charge loss is approximated by the following equation:

$$P_G = V_G Q_G f_{SW} \quad (7)$$

where:

$V_G$ is the driver voltage.
$Q_G$ is the MOSFET total gate charge.

The high-side (switching) MOSFET has to be able to handle conduction loss and switching loss. The high-side MOSFET switching loss is approximated by the equation

$$P_T = \frac{V_{IN} I_L (t_R + t_F) f_{SW}}{2} \quad (8)$$

where $t_R$ and $t_F$ are the rise and fall times of the MOSFET.

$t_R$ and $t_F$ can be calculated using

$$t_R = \frac{\frac{Q_{GS}}{2} + Q_{GD}}{\frac{V_G - V_{SP}}{R_G}}$$

and

$$t_F = \frac{\frac{Q_{GS}}{2} + Q_{GD}}{\frac{V_{SP}}{R_G}}$$

where:

$Q_{GS}$ and $Q_{GD}$ are provided in the MOSFET data sheet.
$R_G$ is the gate resistance
$V_{SP}$ is approximated using

$$V_{SP} \approx V_{TH} + \frac{I_{OUT}}{g_m}$$

where $g_m$ is the MOSFET transconductance.

The high-side MOSFET conduction loss can be calculated as

$$P_{C,high} = D\left(I_{OUT}{}^2 + \frac{\Delta I_L{}^2}{12}\right)R_{DSON} \quad (9)$$

## OUTPUT VOLTAGE

The regulation threshold at the FB pin is 0.6 V, and the maximum input bias current is 100 nA. This bias current can introduce significant error if the divider impedance is too high. In order to get the best accuracy, the bottom resistor, R2, should be no higher than 50 kΩ. On the other hand, very low values of R2 will dissipate excess power. For R2, a 1% resistor with a value between 1 kΩ and 10 kΩ is recommended.

The upper divider is then set using the following formula (it should also be a 1% type):

$$R1 = R2\,\frac{V_{OUT} - 0.6}{0.6} \quad (10)$$

## CURRENT LIMIT SET RESISTOR

The voltage on the CSL pin can be calculated by the following formula:

$$V_{CSL} = I_{CSL}\left(R_{CSL} + R_{DSON\_low}\right) - \left(I_L + \frac{\Delta I_L}{2}\right)R_{DSON\_low} \quad (11)$$

where:

$V_{CSL}$ is the voltage on the CSL pin.
$I_{CSL}$ is the current out from the CSL pin, $I_{CSL}$ = 42 µA.
$R_{CSL}$ is the current limited resistor.
$R_{DSON\_low}$ is the conduction resistor of the lower side MOSFET.
$I_L$ is the output current.
$\Delta I_L$ is the output current ripple.

In normal operation, the direction of current flow through the low-side FET causes a negative voltage to appear on its drain. This voltage is V = IR, where I is the instantaneous FET current and R is its $R_{DSON}$. A +42 µA current source at the ADP1822 CSL pin causes a fixed voltage drop in the current sense resistor that is connected from the CSL pin to the drain of the low-side FET. This current through the current limit set resistor produces a voltage in the opposite direction, thus raising (in the positive direction) the potential at the CSL pin. The resulting net voltage on the CSL pin is compared with ground. During normal operation, the CSL pin stays above ground potential. The overcurrent protection circuitry is triggered when increased FET current produces increased negative voltage on the low-side MOSFET drain, thus causing the voltage on the CSL pin to go negative with respect to ground.

Therefore, the resistor $R_{CSL}$ can be calculated from the following equation:

$$R_{CSL} = \frac{\left(I_{limit} + \frac{\Delta I_L}{2}\right)R_{DSON\_low}}{I_{CSL}} \quad (12)$$

## SETTING THE SOFT START

The soft start characteristic is set by the capacitor connected from SS to GND. The ADP1822 charges $C_{SS}$ to 0.8 V through an internal resistor. The soft start period ($t_{SS}$) is achieved when $V_{CSS}$ = 0.6 V.

$$C_{SS} = \frac{t_{SS}}{-\ln\left(1 - \frac{0.6}{0.8}\right) \times 100\ \text{k}\Omega} \quad (13)$$

where 100 kΩ is the internal resistor.

## OUTPUT VOLTAGE TRACKING

The ADP1822 features an internal comparator that forces the output voltage to track an external voltage at startup, which prevents the output voltage from exceeding the tracking voltage.

The comparator turns off the high-side switch if the positive tracking (TRKP) input voltage exceeds the negative tracking (TRKN) input voltage. Connect TRKP to the output voltage and drive TRKN with the voltage to be tracked. If the voltage at TRKN is below the regulation voltage, the output voltage at TRKN is below the regulation voltage, and the output voltage is limited to the voltage at TRKN. If the voltage at TRKN is above the regulation voltage, the output voltage regulates the desired voltage set by the voltage divider.

## OUTPUT VOLTAGE MARGINING

The ADP1822 features output voltage margining. MSEL is the margin select input. Drive MSEL high to activate the voltage margining feature. Drive MSEL low to regulate the output voltage to the nominal value. If not used, connect MSEL to GND. MAR is the margin control input. MAR is used with MSEL to control output voltage margining. MAR chooses between high voltage and low voltage margining when MSEL is driven high. If not used, connect MAR to GND.

The internal switches from FB are connected to MUP and MSEL terminals to determine the high and low margining. The high voltage is margined by switching a resistor from FB to GND, and the low voltage is margined by switching a resistor from FB to the output voltage.

**Table 4. Voltage Margining Control**

| MAR | MSEL | Voltage Margin |
|---|---|---|
| Low | X | None |
| High | High | High margin (FB connected to MUP) |
| High | Low | Low margin (FB connected to MDN) |

# CONTROL LOOP DESIGN AND EQUATIONS

Figure 2 is a simplified schematic diagram of the overall control loop.

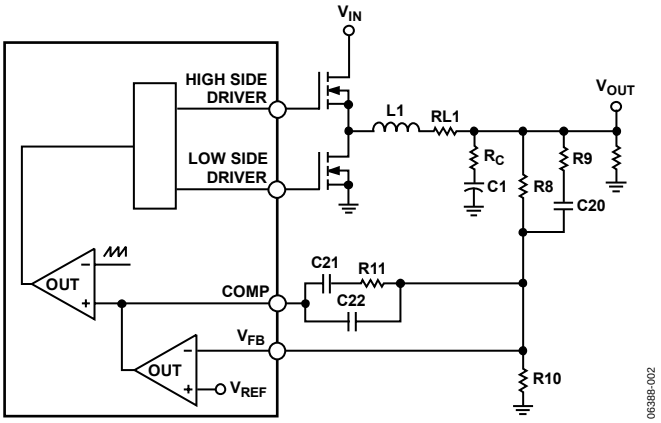


*Figure 2. Control Loop*

## POWER STAGE TRANSFER FUNCTION

The power stage transfer function of the ADP1822 is given by the following equation:

$$G_{VD}(s) = \frac{V_{OUT}(s)}{D(s)} \tag{14}$$

$$G_{VD}(s) = \frac{V_{IN}}{1+\frac{R_L}{R}} \times \frac{1+R_C \times C \times s}{1+\frac{s}{Q\omega_O}+\frac{s^2}{\omega_O^2}} \tag{15}$$

where:

$$\omega_O = \frac{\sqrt{\frac{R_L+R}{R_C+R}}}{\sqrt{LC}}$$

$$Q = \frac{\frac{R_L}{R}+1}{\frac{L}{R}+(R_L+R_C)\times C+\frac{R_C R_L C}{R}} \cdot \frac{1}{\omega_O}$$

$R_C$ is the ESR of the output capacitor.
$R_L$ is the series resistance of output inductor.

## CONTROL CIRCUIT AND TRANSFER FUNCTION

Refer to the compensation circuit shown in Figure 3.

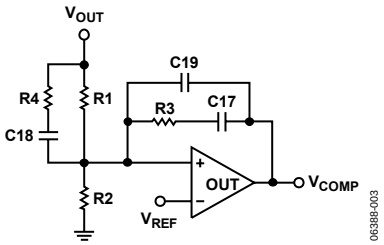


*Figure 3. Compensation Circuit*

The equation for the compensation transfer function is

$$G_{EA}(s) = k \frac{\left(1+\frac{s}{2\pi f_{Z1}}\right)\left(1+\frac{s}{2\pi f_{Z2}}\right)}{\left(1+\frac{s}{2\pi f_{P1}}\right)\left(1+\frac{s}{2\pi f_{P2}}\right)} \tag{16}$$

where:

$$k = -\frac{R3}{R1}$$

$$f_{Z1} = \frac{1}{2\pi R3 C17}$$

$$f_{Z2} = \frac{1}{2\pi(R1+R2)C18}$$

$$f_{P1} = \frac{1}{2\pi R3 \frac{C17 \cdot C19}{C17+C19}}$$

$$f_{P2} = \frac{1}{2\pi R4 C18}$$

The switching frequency is 300 kHz. For best performance, set the crossover frequency to about 1/10 of switching frequency, $f_{SW}$, or around 60 kHz. Lower crossover frequencies cause poor dynamic response, while higher crossover frequencies can cause instability. The best performance usually results from the highest possible crossover frequency that allows adequate gain and phase margins. A phase margin in the range of 40° to 60° is recommended.

## OVERALL LOOP GAIN

The transfer function for the overall control loop can be written as

$$T(s) = \frac{G_{VD}(s) \times G_{EA}(s)}{V_{RAMP}} \quad (17)$$

where $V_{RAMP}$ is the PWM peak ramp voltage (typically 1.25 V) of the ADP1822 controller.

Use the following guidelines to select the compensation components:

1. Set the loop gain cross frequency $f_C$. A good choice is to place the cross frequency $f_C$ at $f_{SW}/10$ for fast response.
2. Cancel ESR zero $f_Z$ by compensator pole $f_{P1}$.
3. Place the high frequency pole $f_{P2}$ to achieve maximum attenuation of switching ripple and high frequency noise.
4. Place two compensator zeros nearby at the power stage resonant frequency $f_O$. Typically, place $f_{Z1}$ below $f_O$ and place $f_{Z2}$ between $f_O$ and $f_C$.
5. Check the phase margin to ensure good regulation performance.

# TEST RESULTS AND MAJOR WAVEFORMS

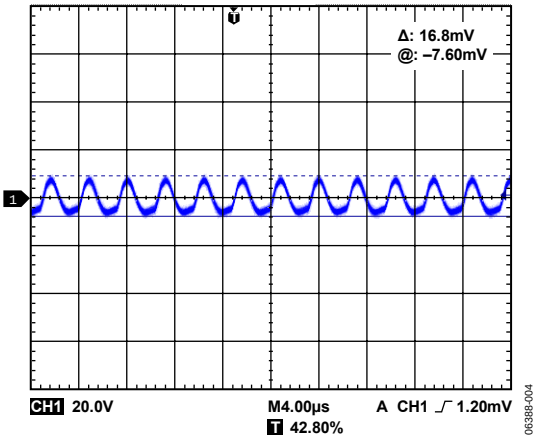


Figure 4. Output Voltage Ripple, Without Load, Channel 1: Output Voltage

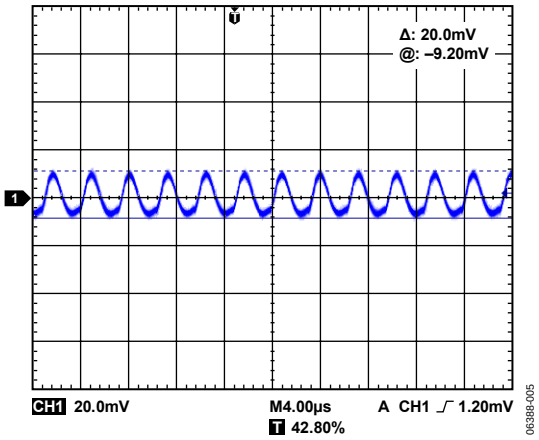


Figure 7. Output Voltage Ripple, 10 A, Channel 1: Output Voltage

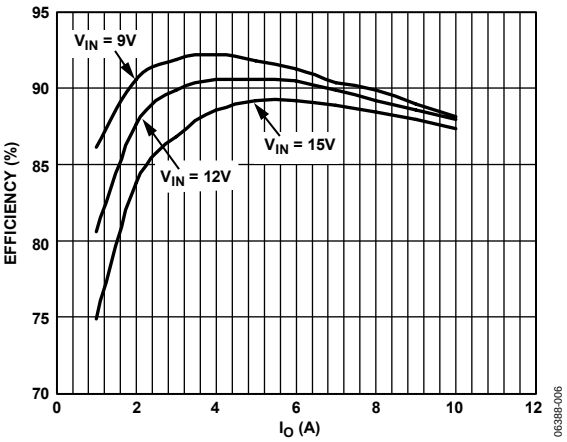


Figure 5. Efficiency vs. Load Current

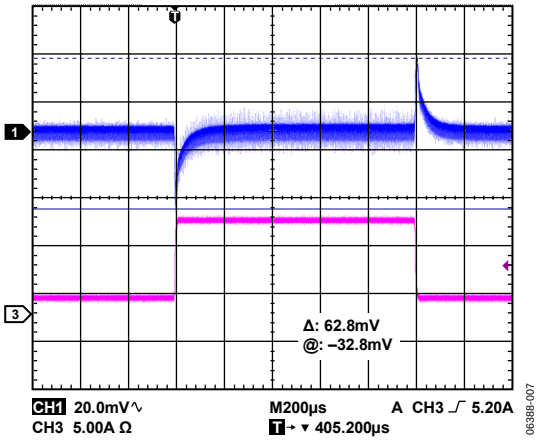


Figure 8. Load Transient Response, Channel 1: Output Voltage (AC-Coupled), Channel 3: Output Current

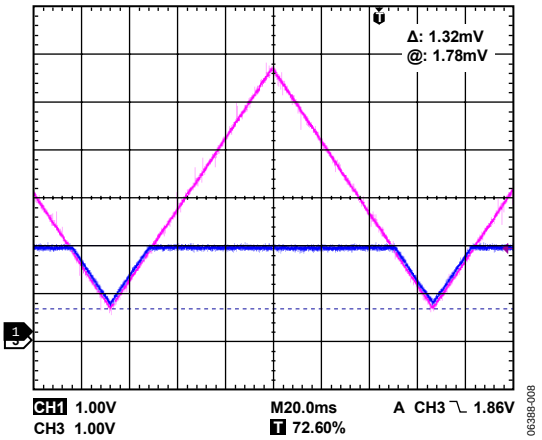


Figure 6. Output Tracking, Channel 1: Output Voltage, Channel 3: Tracking Input

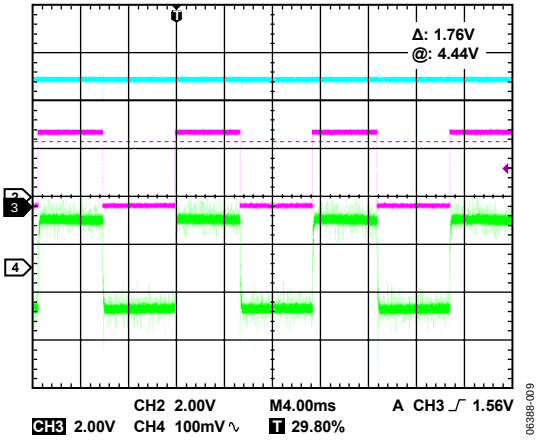


Figure 9. Output Voltage with Margin Up and Margin Down, Channel 2: MAR Pin (Blue Trace), Channel 3: MSEL Pin (Pink Trace), Channel 4: Output Voltage

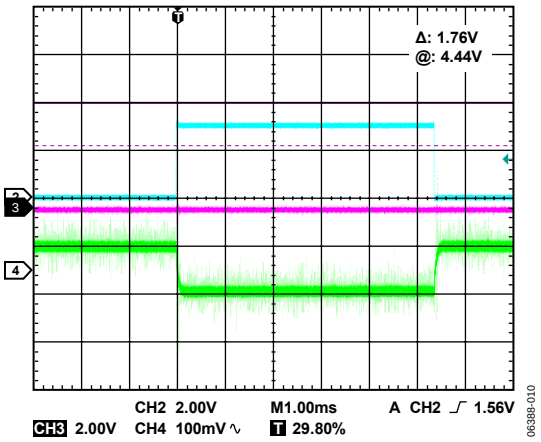


*Figure 10. Output Voltage Margin Down,*
*Channel 2: MAR Pin, Channel 3: MSEL Pin, Channel 4: Output Voltage*

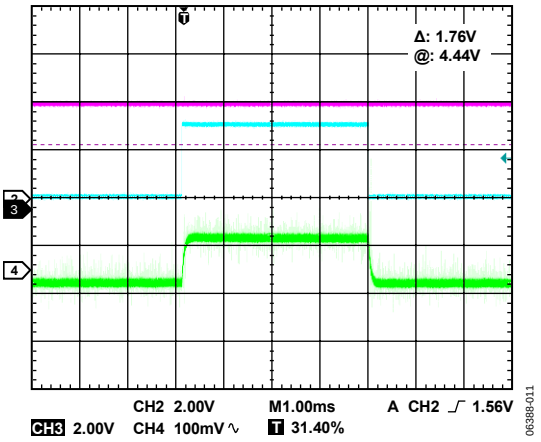


*Figure 12. Output Voltage Margin Up,*
*Channel 2: MAR Pin, Channel 3: MSEL Pin, Channel 4: Output Voltage*

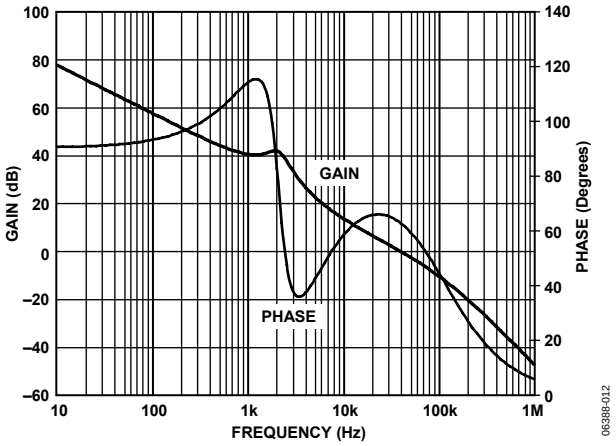


*Figure 11. Control Loop,*
*Cross Frequency: 35.4 kHz, Phase Margin: 63.1°*

# PCB LAYOUT GUIDELINES

1. Use separate analog and power ground planes. Connect the analog circuitry to analog ground. Connect the power circuitry to power ground.
2. To keep the inductance down, the traces from the high-side MOSFET and the low-side MOSFET to the DH and DL pins of the ADP1822, respectively, need to be relatively short and wide.
3. Place the source of Q1 and the drain of Q2 very close to each other to minimize inductance. Use a wide copper trace for this connection. However, too much copper area on this switch node can increase capacitive-coupled common-mode noise.
4. Place ceramic input decoupling capacitors (C2, C3, and C4) close to the Q1 drain and the Q2 source.
5. Place C13 and C14 close to the $V_{IN}$ pin of the IC.
6. The compensation components should also be placed as close as possible to the FB pin.
7. Connect the trace connecting R7 should be directly to the drain of Q2 to ensure an ideal Kelvin connection,.

# EVALUATION BOARD SCHEMATIC AND LAYOUT

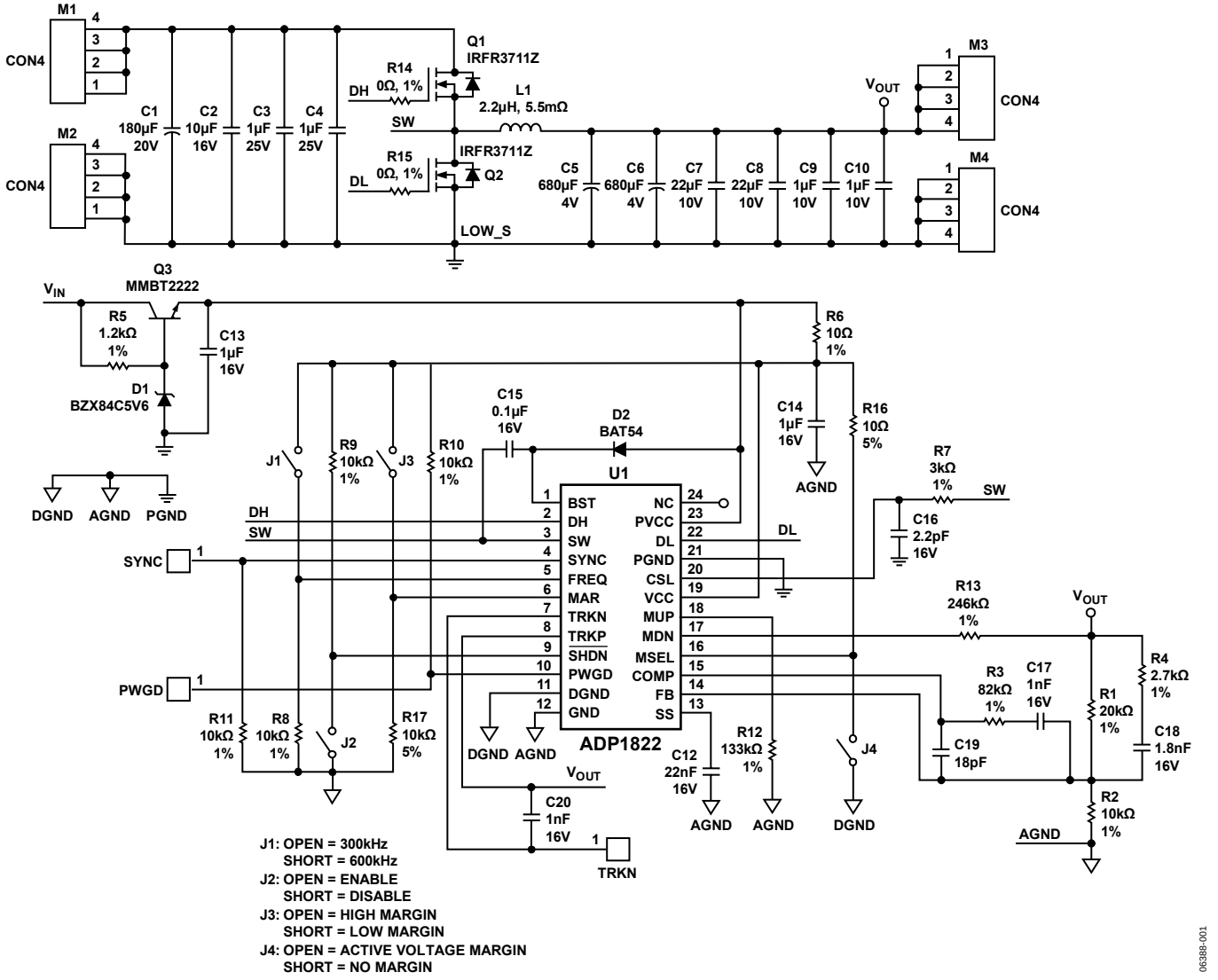


*Figure 13. Typical Application Schematic Diagram*

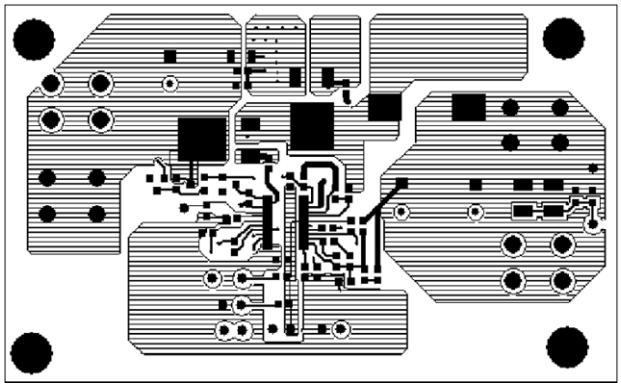


*Figure 14. Top Layer*

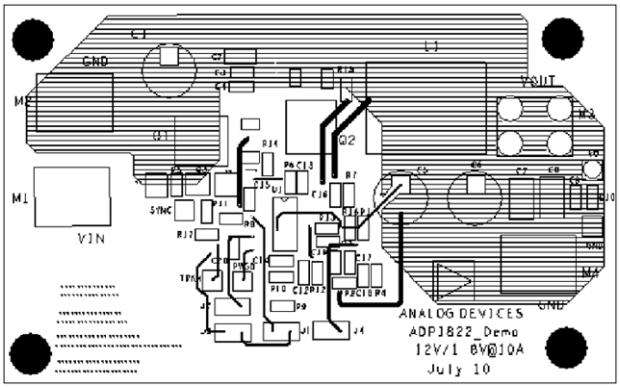


*Figure 15. Bottom Layer*

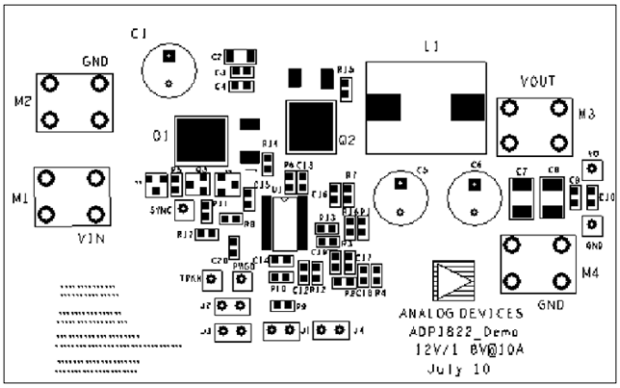


*Figure 16. Silkscreen Top*

# ORDERING INFORMATION

## BILL OF MATERIALS

**Table 5. Bill of Materials for ADP1822 Typical Application Circuit (12 V to 1.8 V @ 10 A, $f_{SW}$ = 300 kHz)**

| Item | Description | Manufacturer | Part No. | Designator | Qty |
|---|---|---|---|---|---|
| 1 | Capacitor, OS-CON, 180 µF, 20 V, 20 mΩ, 11 mm × 10 mm × 5 mm | Sanyo | 20SP180M | C1 | 1 |
| 2 | Capacitor, Ceramic, 10 µF, 25 V, X5R,1206 | Murata | GRM31CR61E106KA12 | C2 | 1 |
| 3 | Capacitor, Ceramic, 1 µF, 25 V, X5R, 0603 | Murata | GRM188R61E105KA12 | C3, C4 | 2 |
| 4 | Capacitor, Ceramic, 1 µF, 16 V, X5R, 0603 | Murata | GRM185R61C105KE44 | C9, C10 | 2 |
| 5 | Capacitor, OS-CON, 680 µF, 4 V, 7 mΩ, 13 mm × 8 mm × 3.5 mm | Sanyo | 4SEPC680M | C5, C6 | 2 |
| 6 | Capacitor, Ceramic, 22 µF, 10 V, X5R, 1210 | Murata | GRM32NR61A226KE19 | C7, C8 | 2 |
| 7 | Capacitor, Ceramic, 22 nF, 16 V, X7R, 0603 | Vishay or equivalent | VJ0603Y233KXXA | C12 | 1 |
| 8 | Capacitor, Ceramic, 1 µF, 16 V, X5R, 0603 | Murata | GRM188R61C105KA93 | C13, C14 | 2 |
| 9 | Capacitor, Ceramic, 0.1 µF, 16 V, X7R, 0603 | Vishay or equivalent | VJ0603Y104MXQ | C15 | 1 |
| 10 | Capacitor, Ceramic, 2.2 pF, 16 V, NPO, 0603 | Vishay or equivalent | VJ0603Y2R2KXXA | C16 | 1 |
| 11 | Capacitor, Ceramic, 1 nF, 16 V, X7R, 0603 | Vishay or equivalent | VJ0603Y102KXXA | C17, C20 | 2 |
| 12 | Capacitor, Ceramic, 1.8 nF, 16 V, X7R, 0603 | Vishay or equivalent | VJ0603Y182KXXA | C18 | 1 |
| 13 | Capacitor, Ceramic, 18 pF, NPO, 0603 | Vishay or equivalent | VJ0603Y180KXXA | C19 | 1 |
| 15 | Diode, Zener, 5.6 V, SOT-23 | FairChild | BZX84C5V6LT1 | D1 | 1 |
| 16 | Diode, Schottky, 30 V, SOT-23 | FairChild | BAT54 | D2 | 1 |
| 17 | Inductor, 2.2 µH, 5.2 mΩ, 13 A (rms) | Cooper Bussmann | HC7-2R2 | L1 | 1 |
| 18 | N MOSFET, 30 V, 61 A, 6.5 mΩ, D-PAK, 17 nC | IR | IRFR3709ZPBF | Q1,Q2 | 2 |
| 19 | Transistor, BJT-NPN, 40 V, SOT-23 | ON Semiconductor | MMBT2222 | Q3 | 1 |
| 20 | Resistor, 20 kΩ, 1/10 W, 1%, 0603 | Vishay or equivalent | CRCW06032002F | R1 | 1 |
| 21 | Resistor, 10 kΩ, 1/10 W, 1%, 0603 | Vishay or equivalent | CRCW06031002F | R2, R8, R9, R10, R11 | 5 |
| 22 | Resistor, 82 kΩ, 1/10 W, 1%, 0603 | Vishay or equivalent | CRCW06038202F | R3 | 1 |
| 23 | Resistor, 2.7 kΩ, 1/10 W, 1%, 0603 | Vishay or equivalent | CRCW06032701F | R4 | 1 |
| 24 | Resistor, 1.2 kΩ, 1/10 W, 1%, 0603 | Vishay or equivalent | CRCW06031201F | R5 | 1 |
| 25 | Resistor, 10 Ω, 1/10 W, 1%, 0603 | Vishay or equivalent | CRCW060310R0F | R6 | 1 |
| 26 | Resistor, 3 kΩ, 1/10 W, 1%, 0603 | Vishay or equivalent | CRCW06033001F | R7 | 1 |
| 27 | Resistor, 133 kΩ, 1/10 W, 1%, 0603 | Vishay or equivalent | CRCW06031334F | R12 | 1 |
| 28 | Resistor, 246 kΩ, 1/10 W, 1%, 0603 | Vishay or equivalent | CRCW06032464F | R13 | 1 |
| 29 | Resistor, 0 Ω, 1/10 W, 1%, 0603 | Vishay or equivalent | CRCW06030R0F | R14, R15 | 2 |
| 30 | Resistor, 10 kΩ, 1/10 W, 5%, 0603 | Vishay or equivalent | CRCW06031002J | R16, R17 | 2 |
| 32 | Input and Output Terminal | Keystone Electronics | CAT.NO.8191 | M1, M2, M3, M4 | 4 |
| 33 | Test Point | Any | Any | PWGD, SYNC, TRKN, VOUT, GND | 5 |
| 34 | Jumper | Any | Any | J1, J2, J3, J4 | 4 |
| 35 | IC— 20 A Step Down DC-to-DC Controller with Tracking and Margining | Analog Devices | ADP1822 | U1 | 1 |

## ORDERING GUIDE

| Model | Package Description |
|---|---|
| ADP1822-EVAL | Evaluation Board |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## NOTES


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