Title	***Engineering Prototype Report for EP-85 – 2 W Charger using*** *LinkSwitch®-LP* ***(LNK564P)***
Specification	90 – 265 VAC Input, 6 V, 330 mA Output
Application	Low Cost, Line Frequency Transformer Based Charger Replacement
Author	Power Integrations Strategic Marketing Department
Document Number	EPR-85
Date	04-Oct-2005
Revision	1.0

Summary and Features

- Low cost, low part count solution (only 14 components)
  - Proprietary IC and Circuit technology enable *Clampless*™ design and very simple *Filterfuse*™ input stage
- Integrated *LinkSwitch-LP* safety/reliability features
  - Over-temperature protection – tight tolerance (+/-5%) with hysteretic recovery for safe pcb temperature under all conditions
  - Auto-restart output short circuit and open-loop protection
  - Extended pin creepage distance for reliable operation in humid environments - >3.2 mm minimum at package
- *EcoSmart®* – Easily meets all existing and proposed international energy efficiency standards – China (CECP) / CEC / EPA / European Commission
  - No-load consumption 140 mW at 265 VAC
  - 64.9% average efficiency measured to CEC spec (versus target 55.2%)
- Ultra-low leakage current: <5 µA at 265 VAC input – No Y cap
- Meets EN550022 and CISPR-22 Class B EMI with >9 dBµV margin
- Meets IEC61000-4-5 Class 3 AC line surge

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Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document describes a universal input charger power supply designed to replace linear transformer based chargers/adapters in low power applications. The power supply utilizes a *LinkSwitch-LP* IC, LNK564P. The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

The *LinkSwitch-LP* IC has been developed to replace linear transformers in low power charger applications. The integrated 700 V switching MOSFET and ON/OFF control function achieve very high efficiency operation under all load conditions with simple bias winding voltage feedback. No-load and operating efficiency performance exceeds all international energy efficiency standards either present or proposed in the future.

Thermal shutdown is included as a minimum requirement to match the safety thermal cut out (thermal fuse) in linear transformers. The IC's intelligent thermal shutdown feature is specified with a very tight tolerance (142 ˚C +/-5%) and includes a hysteretic auto-recovery feature to automatically restart the power supply while maintaining the average pcb temperature at safe levels under all conditions. This auto-recovery is designed to eliminate the potential for field returns since the power supply automatically recovers when ambient temperatures return to the normal operating range. However, with latching thermal shutdown, often used in RCC discrete switching power supply designs, the input AC typically needs to be removed to reset the thermal latching function. With RCCs, there is therefore a potential that power supplies will be returned after a thermal latch off, as customers are often unaware of the need to reset by unplugging the power supply. The auto-recovery thermal shutdown also eliminates noise sensitivity associated with discrete latch circuits, which can be sensitive to circuit design, environmental conditions and component age.

The IC package provides extended creepage distance between high and low voltage pins (both at the package and pcb), which is required in high humidity conditions to prevent arcing. Other features include pulsed auto-restart operation under output short circuit and open loop conditions.

Worst-case no-load power consumption is approximately 140 mW at 265 VAC, well within the 300 mW European standards and even 150 mW at 230 VAC targets set in some customer specifications. Heat generation is minimized with high operating efficiency under all load and line conditions.

The EE16 transformer bobbin provides extended creepage to meet safety spacing requirements.

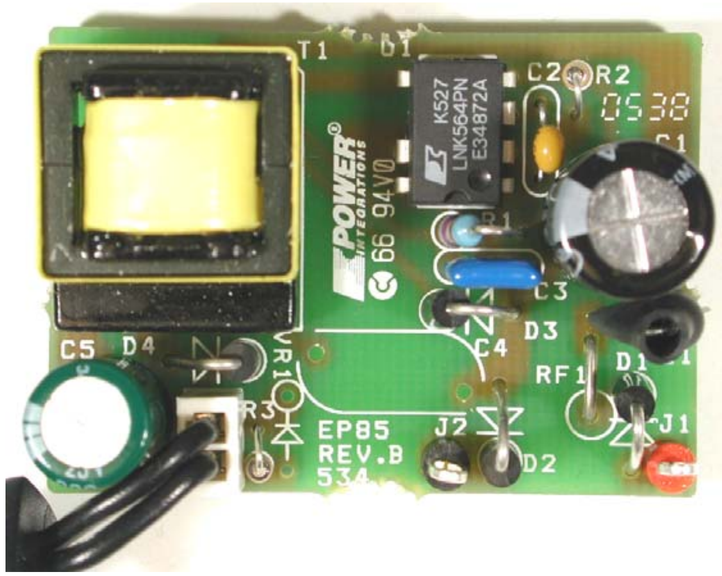

Figure 1 – LNK564 Low Cost Cell Phone Charger Populated Circuit Board Photograph.

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47		63	Hz	
No-load Input Power				0.15	W	230 VAC, 25 °C
Output						
Output Voltage	V_{OUT1}	5.5	6		V	90VAC max. power point
Output Ripple Voltage	$V_{RIPPLE1}$		200		mVpp	0 – 20 Hz
	$V_{RIPPLE2}$		200		mVpp	20 Hz – 20 kHz
	$V_{RIPPLE3}$		200		mVpp	20 kHz – 200 kHz
	$V_{RIPPLE4}$		400		mVpp	200 kHz – 400 kHz
	V_{RIPPLE_TOTAL}		800		mVpp	Total combined
Output Current	I_{OUT1}	0.3	0.33		A	90 VAC, max. power point
Total Output Power						
Continuous Output Power	P_{OUT}		2.0		W	
Efficiency	η	57			%	Measured at 115/230 VAC Ave. 25/50/75/100% load, 25 °C
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				>6 dB margin
Safety		Designed to meet IEC950, UL1950 Class II				
Surge		Meets IEC61000-4-5 Class 3				
External Ambient Temperature	T_{AMB}	-5		45	°C	Free convection, sea level

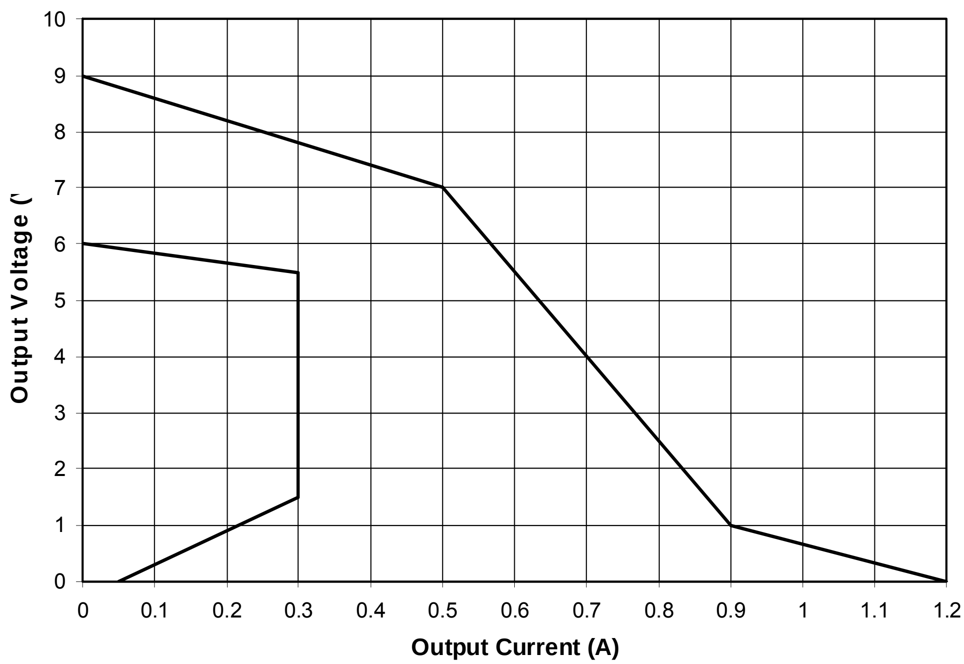

Figure 2 – Low Cost Charger Output Envelope Specification.

3 Schematic

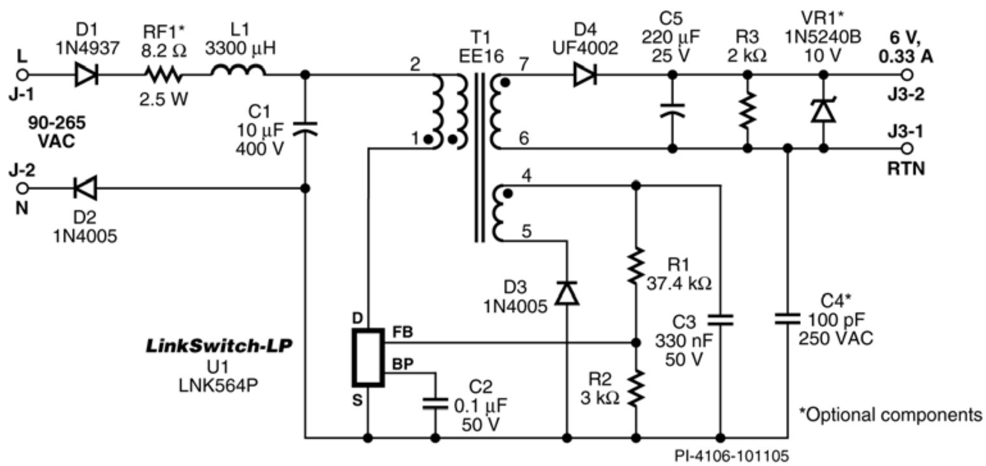

Figure 3 – LNK564 Low Cost Charger Schematic.

4 Circuit Description

4.1 Input and EMI Filtering

AC input differential filtering is accomplished with the very low cost input filter stage formed by C1 and L1. The proprietary frequency jitter feature of the LNK564 eliminates the need for an input pi filter, so only a single bulk capacitor is required. This allows the input inductor L1 to be used as a fuse as well as a filter component. This very simple *Filterfuse* input stage further reduces system cost. The L1 is sleeved to allow it to function as a fuse. An optional fusible resistor, RF1, may be used to provide the fusing function.

Input diode D2 may be removed from the neutral phase in applications where decreased EMI margins and/or decreased input surge withstand is allowed.

4.2 LinkSwitch-LP Feedback

The power supply utilizes simplified bias winding voltage feedback enabled by LNK564 ON/OFF control. The resistor divider formed by R1 and R2 determine the output voltage across the transformer bias winding during the switch off time. In the V/I constant voltage region, the LNK564 device enables/disables switching cycles to maintain 1.69 V on the FB pin. Diode D3 and low cost ceramic capacitor C3 provide rectification and filtering of the primary feedback winding waveform. At increased loads, beyond the constant power threshold, the FB pin voltage begins to reduce as the power supply output voltage falls. The internal oscillator frequency is linearly reduced in this region until it reaches typically 50% of the starting frequency when the FB pin voltage reaches the auto-restart threshold voltage (typically 0.8 V on the FB pin, which is equivalent to 1 V to 1.5 V at the output of the power supply). This function limits the output current in this region without fold back until the output voltage is low.

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No-load consumption can be further reduced by increasing C3 to 0.47 µF or higher.

4.3 Primary Clamp and Transformer Construction

A *Clampless* primary circuit is achieved due to the very tight tolerance current limit trimming techniques used in manufacturing the LNK564, plus the transformer construction techniques used. Peak drain voltage is therefore limited to typically less than 550 V at 265 VAC – providing significant margin to the 700 V minimum drain voltage specification (BV_{DSS}).

4.4 Output Rectification and Filtering

Output rectification and filtering is achieved with output rectifier D4 and filter capacitor C5. Due to the auto-restart feature, the average short circuit output current is significantly less than 1 A, allowing low cost rectifier D4 to be used. Output circuitry is designed to handle a continuous short circuit on the power supply output. Diode D4 is an ultra-fast type, selected for optimum V/I output characteristics. Optional resistor R3 provides a pre-load, limiting the output voltage level under no-load output conditions. Despite this pre-load, no-load consumption is within targets at approximately 140 mW at 265 VAC. The additional margin of no-load consumption requirement can be achieved by increasing the value of R4 to 2.2 kΩ or higher while still maintaining output voltage well below the 9 V maximum specification. Placement is left on the board for an optional Zener clamp (VR1) to limit maximum output voltage under open loop conditions, if required.

4.5 Optional Components

Fusible resistor RF1, VR1 and C4 are all optional components. Resistor RF1, VR1 and C4 are not fitted on the board as standard, RF1 being replaced with a wire link.

- Resistor RF1 may be fitted to designs where a traditional fuse is preferred over the *Filterfuse* configuration.
- Zener diode VR1 is fitted where the output voltage must be limited to a lower value during open loop conditions. The auto-restart feature of *LinkSwitch-LP* limits the output power under this condition, requiring only a zener with a low, 0.5 W rating.
- The use of *E-Shield*™ techniques in the transformer removes the need for a Y1 safety capacitor across the safety isolation barrier to meet EMI. However, the use of C4, a small value (100 pF) Y1 capacitor provides improved EMI consistency if transformer construction variation is a concern.

5 PCB Layout

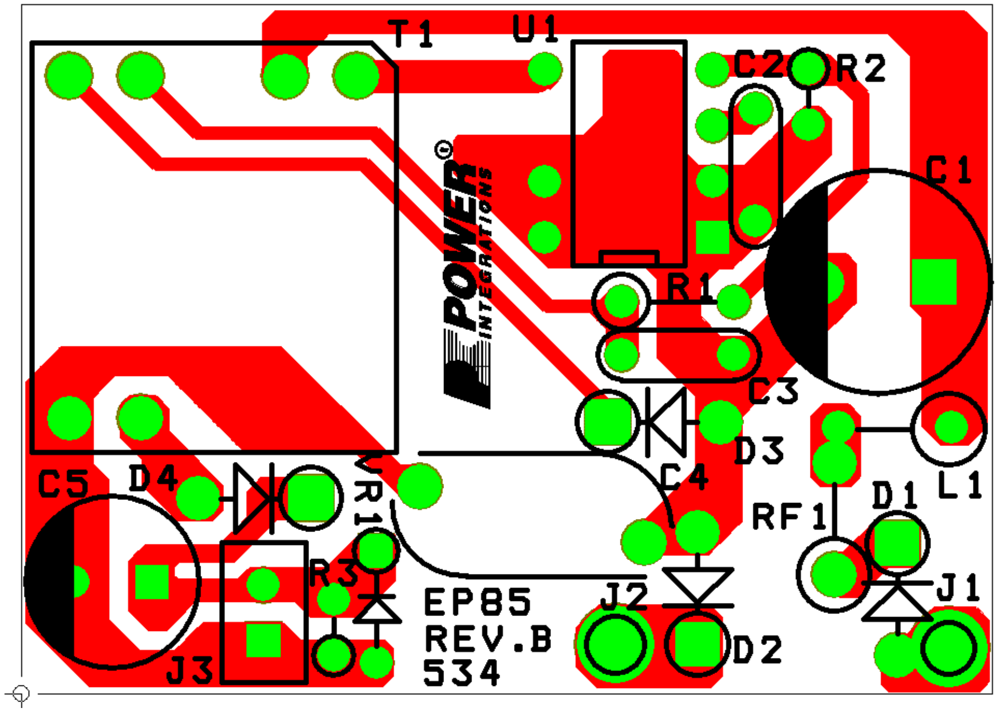

Figure 4 – LNK564 Low Cost Charger Printed Circuit Layout.

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6 Bill Of Materials

Item	Qty	Ref	Description	Manufacturer	Manufacturer Part #
1	1	C1	10 µF, 400 V, Electrolytic, Low ESR, 79 mA, (10 x 12.5)	Ltec	TYD2GM100G13O
2	1	C2	100 nF, 50 V, Ceramic, Z5U	Kemet	C317C104M5U5CA
3	1	C3	330 nF, 50 V, Ceramic, X7R	Panasonic	ECU-S1H334KBB
4*	1	C4	100 pF, Ceramic, Y1	Vishay	440LT10
5	1	C5	220 µF, 25 V, Electrolytic, Very Low ESR, 72 mΩ, (8 x 11.5)	United Chemi-Con	KZE25VB221MH11LL
6	1	D1	600 V, 1 A, Fast Recovery Diode, 200 ns, DO-41	Vishay	1N4937
7	2	D2 D3	600 V, 1 A, Rectifier, DO-41	Vishay	1N4005
8	1	D4	100 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	Vishay	UF4002
9	2	J1 J2	Test Point	Keystone	5011
10	1	J3	6 ft, 22 AWG, 0.25 Ω, 2.1 mm	Generic	
11	1	L1	3300 µH, 62 mA, 59.5 Ω, Axial Ferrite Inductor	Epcos	B78108S1335J
12	1	-	Heatshrink tubing, 3/16” diameter, 0.5” length	Generic	Generic
13	1	R1	37.4 kΩ, 1%, 1/4 W, Metal Film	Yageo	MFR-25FBF-37K4
14	1	R2	3 kΩ, 5%, 1/8 W, Carbon Film	Yageo	CFR-12JB-3K0
15	1	R3	2 kΩ, 5%, 1/8 W, Carbon Film	Yageo	CFR-12JB-2K0
*16***	*1*	*RF1*	*8.2 Ω, 2.5 W, Fusible/Flame Proof Wire Wound*	*Vitrohm*	*CRF253-4 5T 8R2*
17	1	T1	Bobbin, EE16, Horizontal, 10 pins	Ngai Cheong Electronics	EE-16 10PINs
			Assembled unit available from	Falco Hical CWS Li Shin Woo Jin	E09077 SIL6036 CWS-T1-DAK85 LSLA40342 SLP-2218P1
18	1	U1	*LinkSwitch-LP*, LNK564P, DIP-8B	Power Integrations	LNK564P
*19**	*1*	*VR1*	*10 V, 5%, 500 mW, DO-35*	*Microsemi*	*1N5240B*

*Optional component

** Optional components - not fitted replaced with jumper on board

7 Transformer Specification

7.1 Electrical Diagram

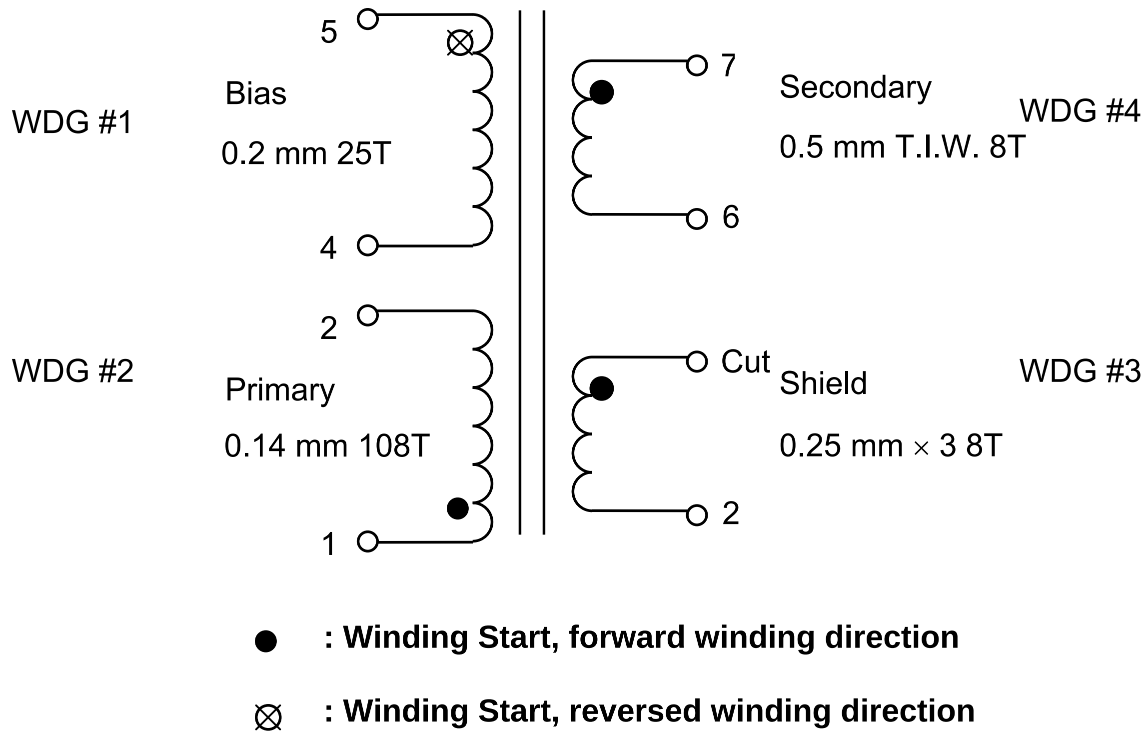

Figure 5 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	60 Hz 1 min, from pins 1-5 to pins 6-7	3000 VAC
Primary Inductance	From pins 1-2, all other windings open	2.7 mH, -/+5%
Primary Winding Capacitance	All windings open	50 pF (Max.)
Primary Leakage Inductance	From pins 1-2 with pins 6-7 shorted	75 μH (Max.)

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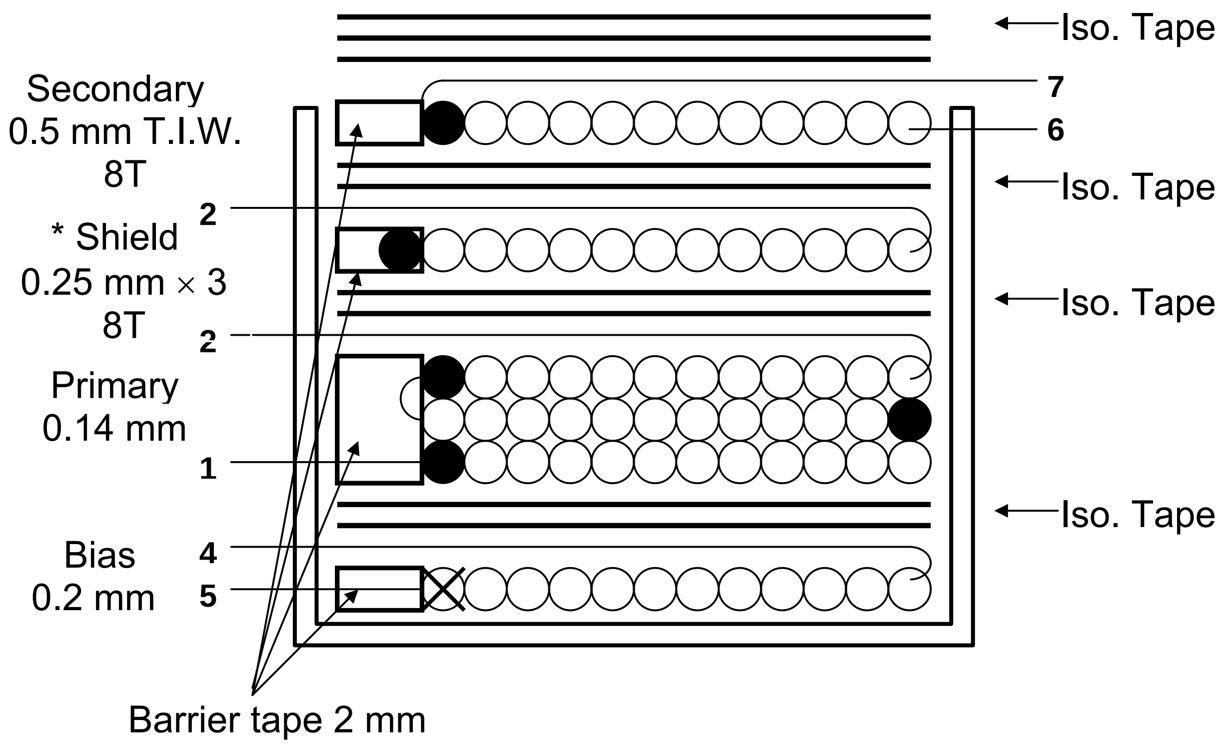
7.3 Materials

Item	Description
[1]	Core : EE16, PC40EE13, TDK – A_{LG} 230 nH/T^2
[2]	Bobbin: Horizontal 10 pin – pins 3, 8, 9, and 10 removed
[3]	Magnet Wire: 0.20 mm Polyurethane coated class 2 wire
[4]	Magnet Wire: 0.14 mm Polyurethane coated class 2 wire
[5]	Magnet Wire: 0.25 mm Polyurethane coated class 2 wire
[6]	Triple Insulated Wire: 0.5 mm
[7]	Tape: 3M 1298 Polyester Film (white) 320 mils wide by 1 mil thick
[8]	Barrier Tape: 2 mm width
[9]	Varnish (dip)

7.4 Transformer Build Diagram



* See Fig. 7 for detail of shield winding start technique.

Figure 6 – Transformer Build Diagram.

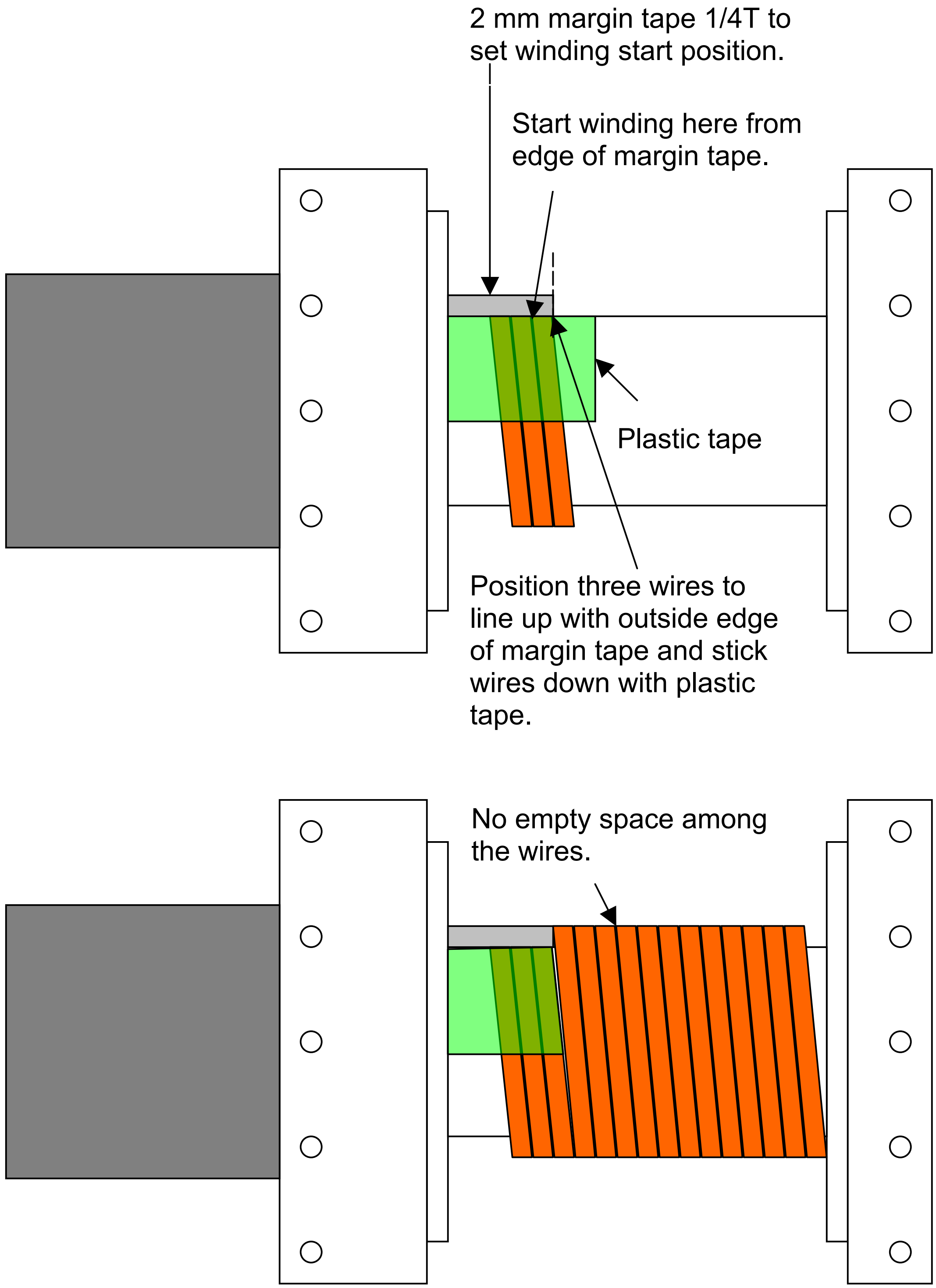


Figure 7 – Winding Method of Shield Winding.

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7.5 Design Spreadsheet

ACDC_LinkSwitch-LP_091605; Rev.1.0; Copyright Power Integrations 2005	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-LP_091605_Rev1-0.xls; LinkSwitch-LP Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					**EP85 Design**
VACMIN	90			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	6.00			Volts	Output Voltage (main) measured at the end of output cable (For CV/CC designs enter typical CV tolerance limit)
IO	0.33			Amps	Power Supply Output Current (For CV/CC designs enter typical CC tolerance limit)
Constant Voltage / Constant Current Output	YES		CVCC	Volts	Enter "YES" for CV/CC output. Enter "NO" for CV only output
Output Cable Resistance	0.05		0.05	Ohms	Enter the resistance of the output cable (if used)
PO			1.99	Watts	Output Power (VO x IO + dissipation in output cable)
Feedback Type	BIAS			Bias Winding	Enter 'BIAS' for Bias winding feedback and 'OPTO' for Optocoupler feedback
Add Bias Winding	YES		Yes		Enter 'YES' to add a Bias winding. Enter 'NO' to continue design without a Bias winding. Addition of Bias winding can lower no load consumption
Clampless design	YES		Clampless		Enter 'YES' for a clampless design. Enter 'NO' if an external clamp circuit is used.
n	0.70				Efficiency Estimate at output terminals. For CV only designs enter 0.7 if no better data available
Z	0.50		0.5		Loss Allocation Factor (Secondary side losses / Total losses)
tC	2.80			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	10.00			uFarads	Input Capacitance
Input Rectification Type	H		*H*		Choose H for Half Wave Rectifier and F for Full Wave Rectification
ENTER LinkSwitch-LP VARIABLES					
LinkSwitch-LP	LNK564				LinkSwitch-LP device
Chosen Device		*LNK564*			
ILIMITMIN			*0.124*	Amps	Minimum Current Limit
ILIMITMAX			*0.146*	Amps	Maximum Current Limit
fSmin			*93000*	Hertz	Minimum Device Switching Frequency
I^2fMIN			1665	A^2Hz	I^2f Minimum value (product of current limit squared and frequency is trimmed for tighter tolerance)
I^2fTYP			1850	A^2Hz	I^2f typical value (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	88.00		88	Volts	Reflected Output Voltage
VDS			10	Volts	LinkSwitch-LP on-state Drain to Source Voltage
VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
KP			1.54		Ripple to Peak Current Ratio (0.9<KRP<1.0 : 1.0<KDP<6.0)
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type			EE16		Suggested smallest commonly available core
Core		*EE16*		*P/N:*	PC40EE16-Z
Bobbin		*EE16_BOBBIN*		*P/N:*	EE16_BOBBIN
AE			0.192	cm^2	Core Effective Cross Sectional Area
LE			3.5	cm	Core Effective Path Length
AL			1140	nH/T^2	Ungapped Core Effective Inductance
BW			8.6	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			2		Number of primary layers
NS	8		8		Number of Secondary Turns
NB			27		Number of Bias winding turns
VB			21.93	Volts	Bias Winding Voltage
R1			36.89	k-ohms	Resistor divider component between bias wiinding and FB pin of LinkSwitch-LP

R2			3.00	k-ohms	
Recommended Bias Diode			1N4003		
DC INPUT VOLTAGE PARAMETERS					
VMIN			80	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.48		Maximum Duty Cycle
IAVG			0.04	Amps	Average Primary Current
IP			0.12	Amps	Minimum Peak Primary Current
IR			0.12	Amps	Primary Ripple Current
IRMS			0.05	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			2738	uHenries	Typical Primary Inductance. +/- 5%
LP_TOLERANCE	5.00		5	%	Primary inductance tolerance
NP			108		Primary Winding Number of Turns
ALG			233	nH/T^2	Gapped Core Effective Inductance
BM		***Info***	1922	Gauss	!!! Info. Flux densities above ~ 1500 Gauss may produce audible noise. Verify with dip varnished sample transformers. Increase NS to greater than or equal to 11 turns or increase VOR
BAC			801	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1654		Relative Permeability of Ungapped Core
LG		*Warning*	0.08	mm	!!! INCREASE GAP>>0.1 (increase NS, decrease VOR,bigger Core
BWE			17.2	mm	Effective Bobbin Width
OD			0.16	mm	Maximum Primary Wire Diameter including insulation
INS			0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.12	mm	Bare conductor diameter
AWG			37	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			20	Cmils	Bare conductor effective area in circular mils
CMA			374	Cmils/Amp	Primary Winding Current Capacity (150 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			1.68	Amps	Peak Secondary Current
ISRMS			0.65	Amps	Secondary RMS Current
IRIPPLE			0.56	Amps	Output Capacitor RMS Ripple Current
CMS			130	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			28	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.32	mm	Secondary Minimum Bare Conductor Diameter
ODS			1.08	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.38	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			-	Volts	Peak Drain Voltage is highly dependent on Transformer capacitance and leakage inductance. Please verify this on the bench and ensure that it is below 650 V to allow 50 V margin for transformer variation.
PIVS			34	Volts	Output Rectifier Maximum Peak Inverse Voltage

Note: Gap size was verified with transformer vendor as being acceptable. Higher flux density resulted in peak audible noise of <35 dBA without enclosure, also acceptable as a further 10 dB reduction is typical once inside sealed enclosure.

8 Performance Data

All measurements performed at room temperature, 47 Hz input frequency.

8.1 Efficiency

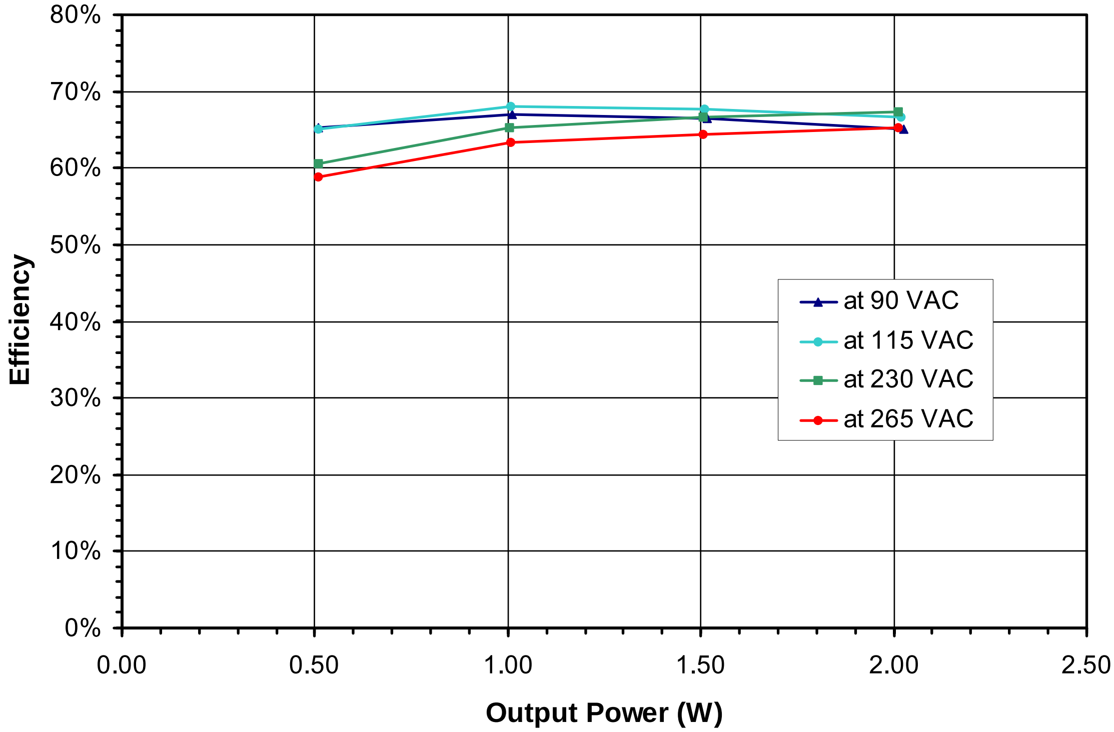

Figure 8 – Efficiency vs. Output Power.

8.1.1 Active Mode CEC Measurement Data

The table below lists the operating efficiencies at specific load points measured at the nominal input voltages. For the purposes of the CEC & EPA calculations, 2 W output was taken as the 100% load point. The CEC & EPA spec shown in the table below was calculated based on 2 W as the nominal 100% load.

Input Voltage	25% Relative P_{OUT}	50% Relative P_{OUT}	75% Relative P_{OUT}	100% Relative P_{OUT}	Average Efficiency (%)	CEC / EPA Spec. (%)
115 VAC	65.0	68.1	67.7	66.6	66.8	55.2
230 VAC	60.5	65.3	66.6	67.3	64.9	55.2

8.2 No-Load Input Power

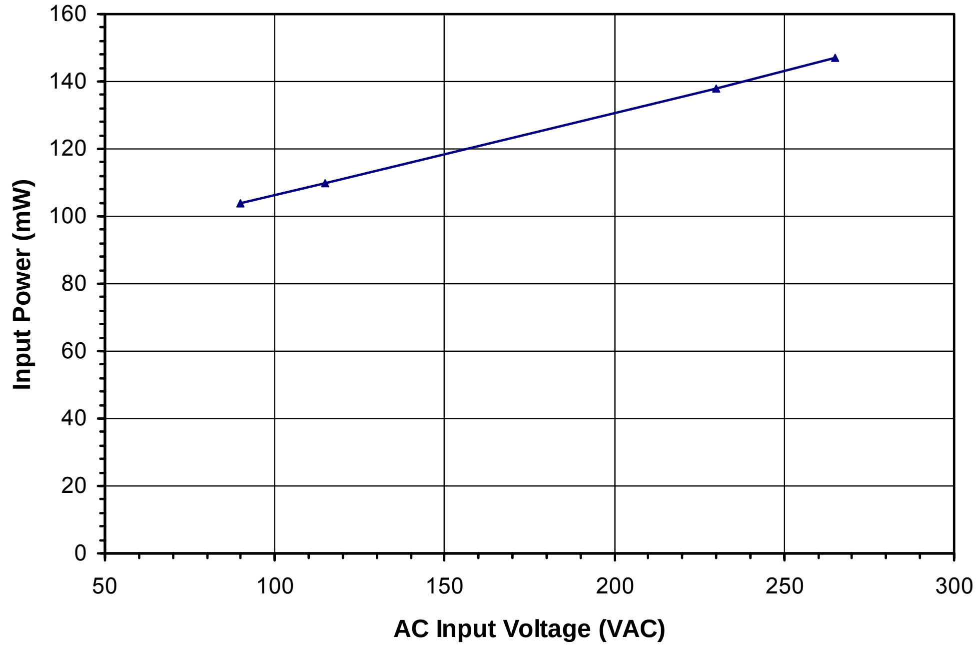

Figure 9 – No-Load Input Power vs. Input Line Voltage.

8.3 Regulation

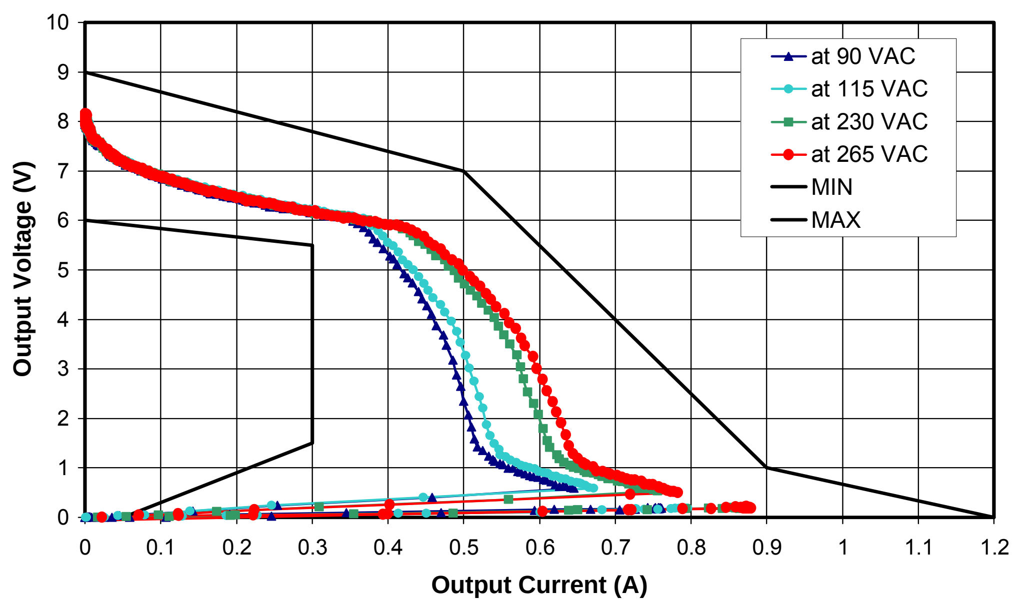

Figure 10 – Load and Line Regulation.

The LNK564 device enters auto-restart for output voltages below typically 1.5 V, thus preventing excessive short circuit current.

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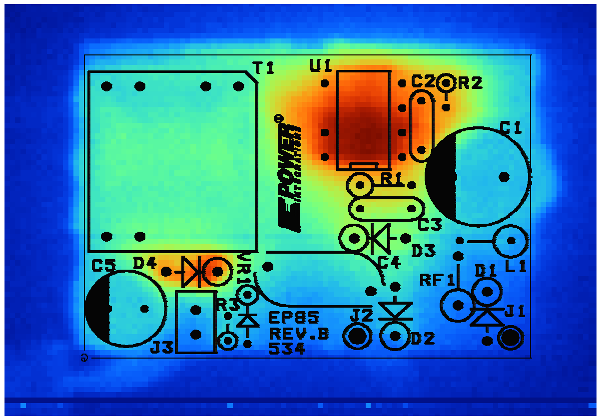
9 Thermal Performance

High temperature testing was completed in a sealed adapter enclosure at elevated ambient of 45 °C under conditions of natural convection. Input voltage was set to 90/265 VAC with 47 Hz line frequency. The output was adjusted to maintain full load 1.93 W and 2.1 W, respectively.

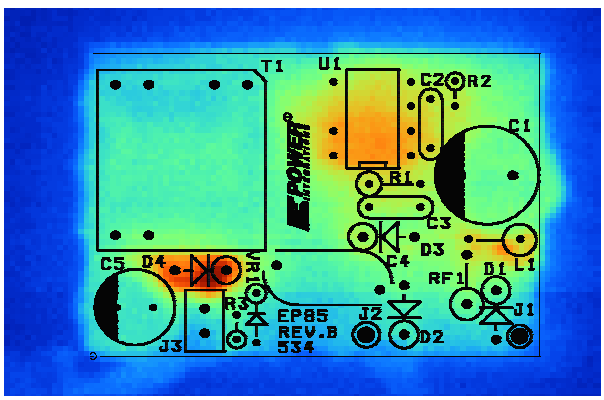
Thermocouple Location	Reference	Measured Temperature Rise (°C)	
		90 VAC, 1.93 W_{OUT}	265 VAC, 2.1 W_{OUT}
LNK564P, pins 1,2	U1	37.1	55
Bulk Input Capacitor	C1	16	12
Transformer	T1	14	17
Output Rectifier	D4	40	43

All temperatures are regarded as well within normally acceptable operating temperature ranges.

An infrared thermograph was taken of the unit operating open frame at room ambient. This confirms that the correct components were selected for temperature measurement in the table above and that high line is worst case for U1.



265 VAC, 2 W load, 22°C Ambient



90 VAC, 2 W load, 22°C Ambient

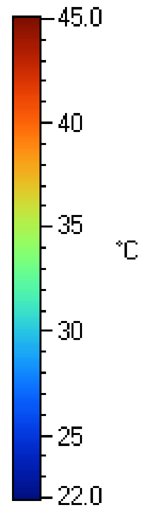


Figure 11 – Infra-Red Thermograph of Unit Operating Open Frame, Room Ambient

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10 Waveforms

10.1 Drain Voltage and Current, Normal Operation

Figure 12 – 90 VAC, Full Load.
Upper: I_{DRAIN}, 0.10 A / div.
Lower: V_{DRAIN}, 200 V, 2 µs / div.

Figure 13 – 265 VAC, Full Load.
Upper: I_{DRAIN}, 0.10 A / div.
Lower: V_{DRAIN}, 200 V / div, 2 µs / div.

10.2 Output Voltage Start-Up Profile, Battery Load

A simulated battery load was used to verify the power supply start-up profile.

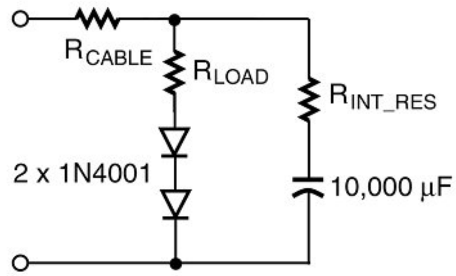

Figure 14 – Battery Output Load, R_{LOAD} = 15 Ω.

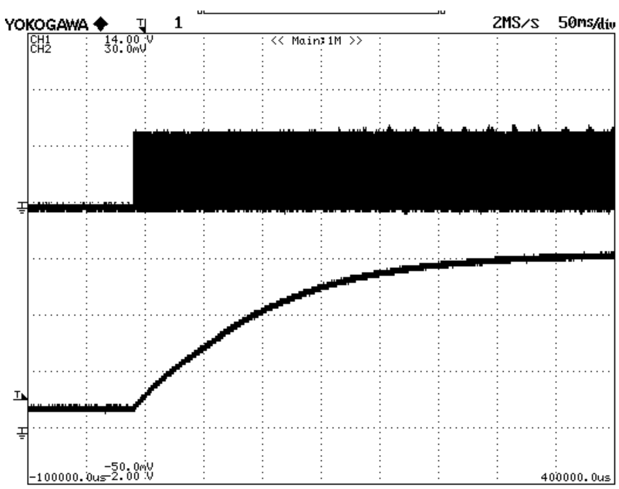

Figure 15 – Battery Start-Up Profile, 90 VAC.
Upper: I_{DRAIN}, 0.10 A / div.
Lower: V_{OUT}, 2 V, 50 ms / div.

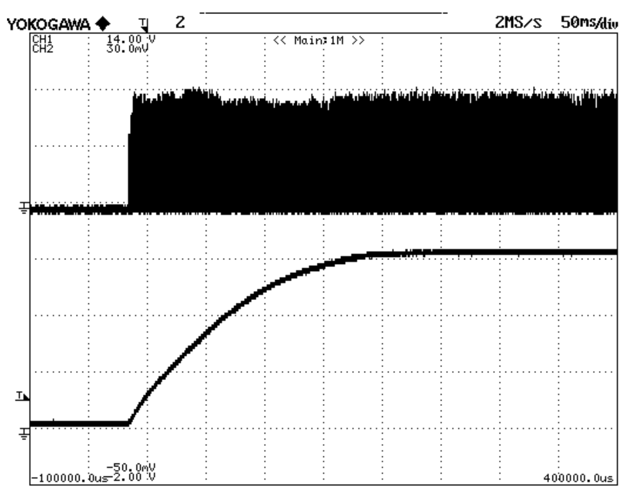

Figure 16 – Battery Start-Up Profile, 265 VAC.
Upper: I_{DRAIN}, 0.10 A / div.
Lower: V_{OUT}, 2 V, 50 ms / div.

With a simulated battery load, the output voltage reaches regulation within 200 ms. No output overshoot is observed. Note that the peak of the I_{DRAIN} waveform in Figure 15 is the leading edge current spike, not I_{DRAIN} at the end of the switching cycle.

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10.3 Drain Voltage and Current Start-Up Profile

Drain Voltage and Current waveforms are presented with the simulated battery load.

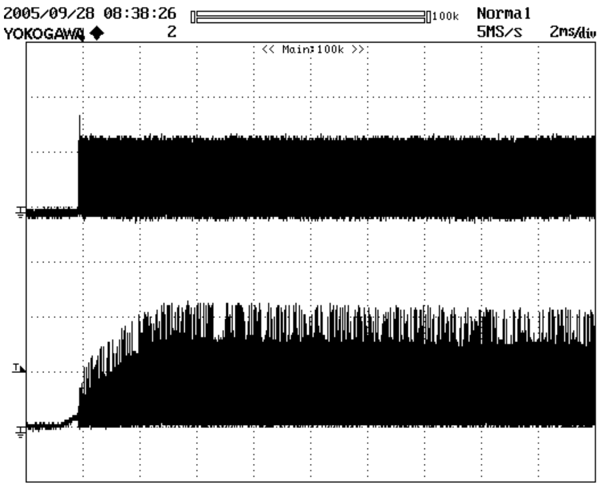

Figure 17 – 90 VAC Input and Maximum Load.
Upper: I_{DRAIN}, 0.10 A / div.
Lower: V_{DRAIN}, 100 V, 2 ms / div.

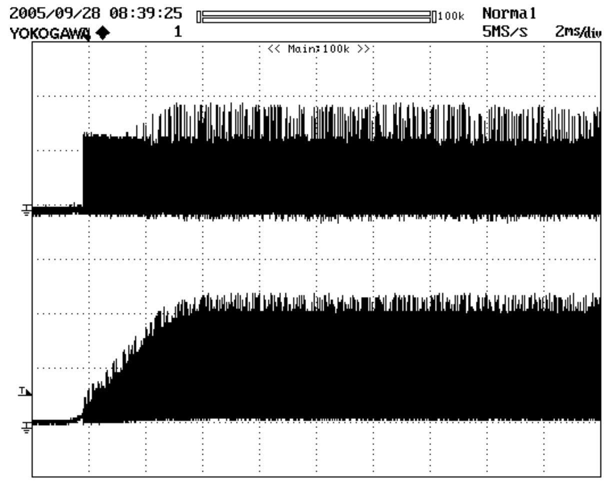

Figure 18 – 265 VAC Input and Maximum Load.
Upper: I_{DRAIN}, 0.10 A / div.
Lower: V_{DRAIN}, 200 V, 2 ms / div.

At start-up with a battery load, Drain current and Drain voltages are well controlled and within acceptable operating limits. Note that the peak of the I_{DRAIN} waveform in Figure 17 is the leading edge current spike not I_{DRAIN} at the end of the switching cycle.

10.4 Output Ripple Measurements

10.4.1 Ripple Measurement Technique

A ripple probe, which included a 1.0 μF Aluminum electrolytic capacitor in parallel with a 0.1 μF ceramic capacitor, was used for all ripple measurements. The probe was located at the end of the DC output cable assembly.

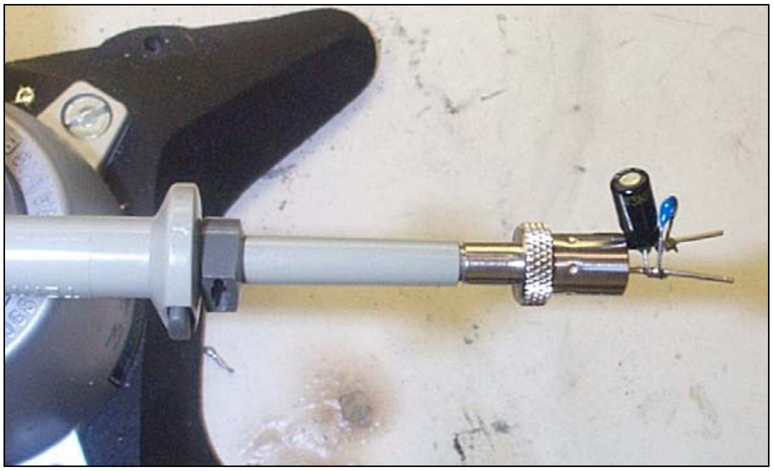

Figure 19 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter (modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added).

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10.4.2 Measurement Results

Output ripple measurements were carried out at room temperature. A programmable AC source was used with line frequency set to 60 Hz. Output ripple measurement recorded at end of DC harness. Carbon film resistive loads were utilized.

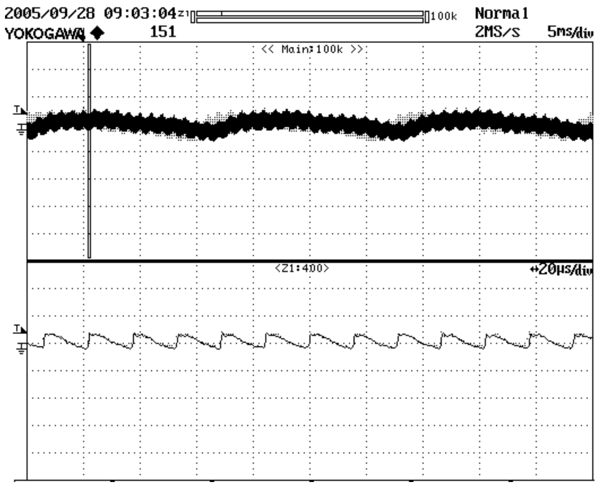

Figure 20 – V_O Ripple, 90 VAC / 60 Hz, V_O = 2.5 V. 5 ms & 20 µs, 100 mV / div.

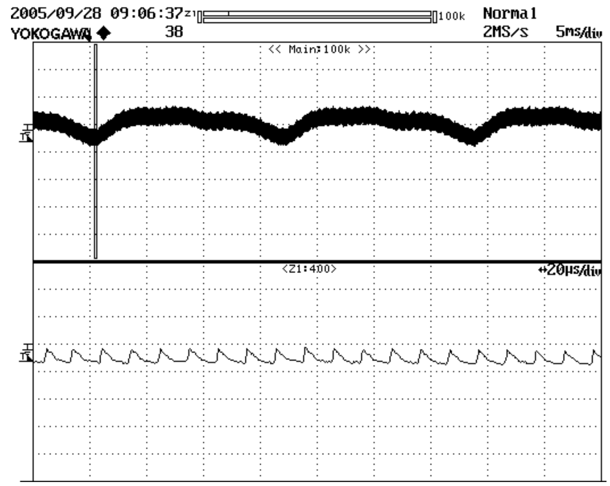

Figure 21 – V_O Ripple, 90 VAC / 60 Hz, V_O = 6 V. 5 ms & 20 µs, 100 mV / div.

Under worst-case 90 VAC and 265 VAC and maximum loading conditions, total switching output ripple is below 150 mV pk-pk.

11 Conducted EMI

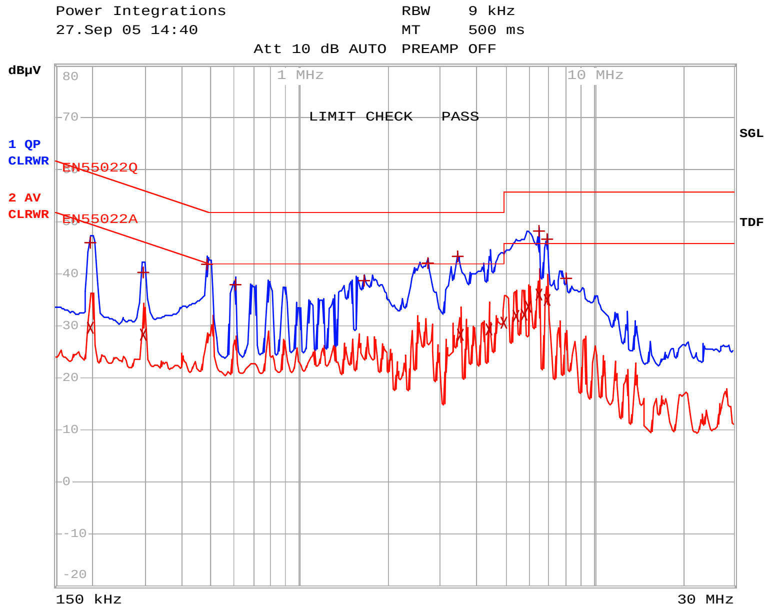

Figure 23 – Conducted Emissions, Neutral 115 VAC, 17 Ω Load, with Artificial Hand at Output. QP-Dark Blue, AVG-Red.

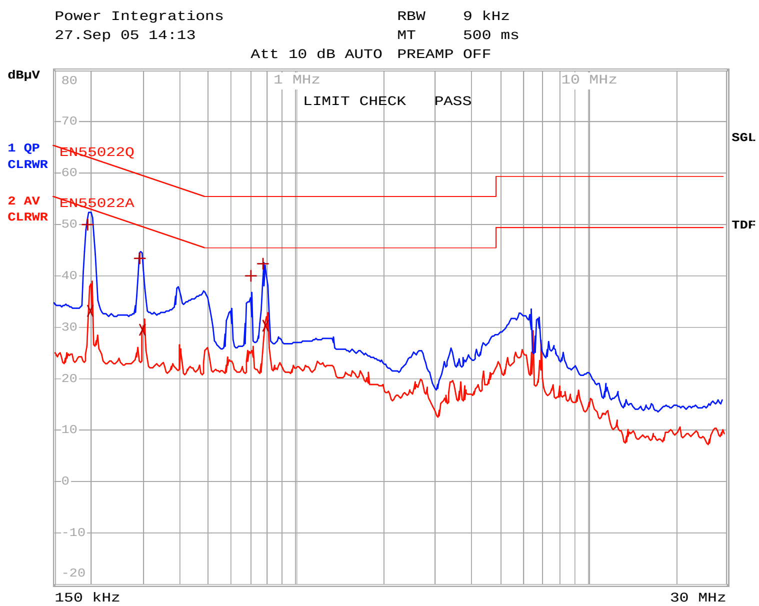

Figure 24 – Conducted Emissions, Line 115 VAC, 17 Ω Load, with Artificial Hand at Output. QP-Dark Blue, AVG-Red.

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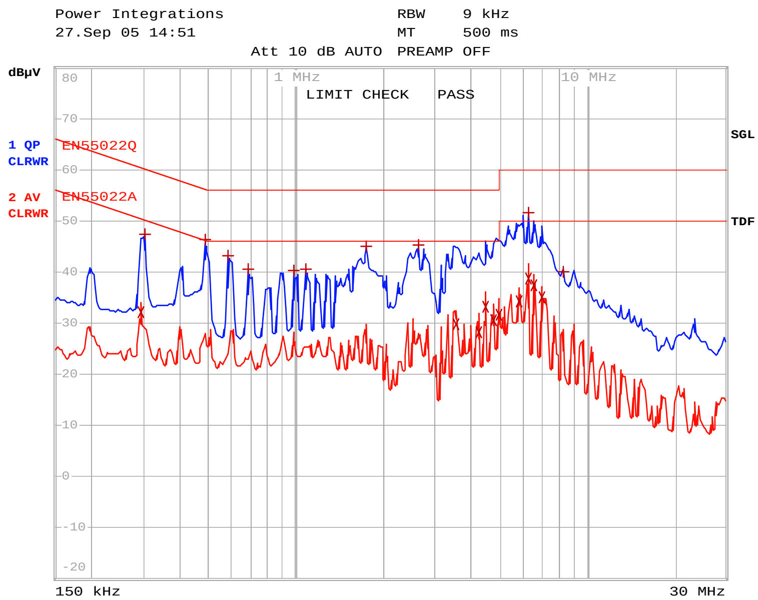

Figure 25 – Conducted Emissions, Neutral 230 VAC, 17 Ω Load, with Artificial Hand at Output. QP-Dark Blue, AVG-Red.

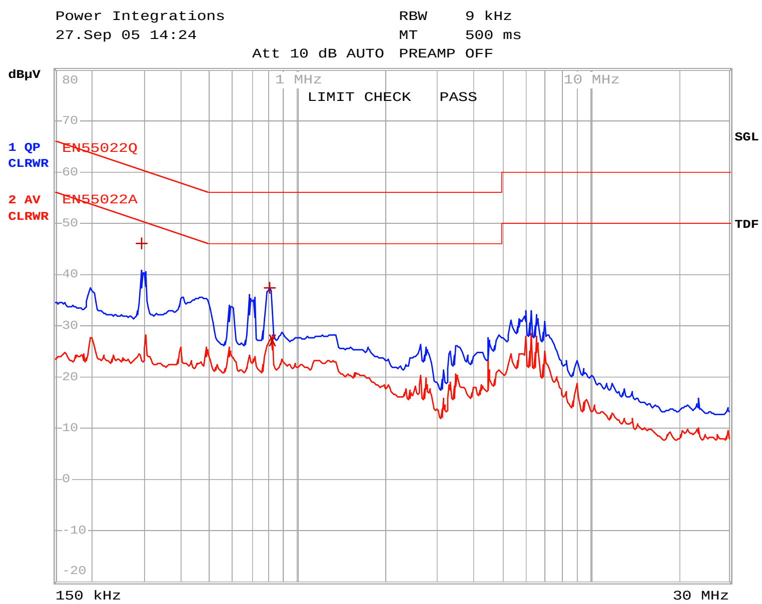

Figure 26 – Conducted Emissions, Line 230 VAC, 17 Ω Load, with Artificial Hand at Output. QP-Dark Blue, AVG-Red

The EMI results show >9 dB margin worst case to quasi-peak and average EN55022B limits.

12 AC Line Surge

Input line 1.2/50 µs differential surge testing (2 Ω generator output impedance) was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load with a 17 Ω resistor and operation was verified during and following each surge event. Neither failures nor output glitches were seen.

Surge Testing Results				
Surge Level (V)	**Input Voltage (VAC)**	**Injection Location**	**Phase Injection (°)**	**Test Result (Pass/Fail)**
+250	230	L N	90	Pass
-250	230	L N	90	Pass
+500	230	L N	90	Pass
-500	230	L N	90	Pass
+750	230	L N	90	Pass
-750	230	L N	90	Pass
+1000	230	L N	90	Pass
-1000	230	L N	90	Pass

Unit passes under all test conditions.

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13 Revision History

Date	Author	Revision	Description & changes
04-Oct-05	SM/SR	1.0	Formatted for Final Release

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