LM48555 Evaluation Board

National Semiconductor
Application Note 1611
Nisha Patel
April 2007

Quick Start Guide

1) Apply power supply voltage to positive terminal of JU4, and source ground to the negative terminal.

2) Short the terminals of JU1 to release the device from shutdown mode.

3) Connect a ceramic speaker, and series resistance load across the output terminals of JU3.

4) Apply a differential audio signal to the positive and negative terminals of JU2.

Introduction

The LM48555 is an audio power amplifier designed to drive ceramic speakers in portable applications. The LM48555 outputs15.5V_{P-P} with less than 1% THD+N while operating from a 3.2V power supply. The LM48555 features differential inputs for improved noise rejection and a low power shutdown mode.

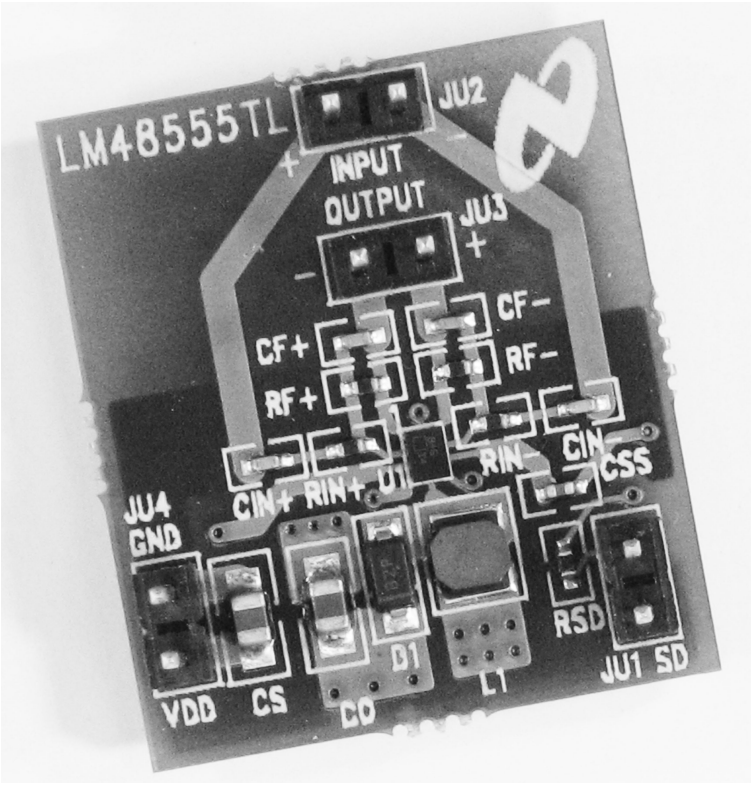
The LM48555 includes advanced click and pop suppression that eliminates audible turn-on and turn-off transients. Additionally, the integrated boost regulator features a soft start function that minimizes transient current during power-up. The LM48555 is unity-gain stable and uses external gain-setting resistors.

The LM48555 Evaluation board (shown in Figure 1) allows the user to easily evaluate the performance and characteristics of the LM48555 device. It provides connectors for audio inputs, audio outputs, power supply, and shutdown control. The ceramic speaker load is not included on the demo board, an external ceramic speaker plus series resistor is needed for evaluation.

Operating Conditions

- Temperature Range
  $-40°C \leq T_A \leq +85°C$
- Supply Voltage
  $2.7V < V_{DD} < 6.5V$

LM48555 Evaluation Board



30014812

FIGURE 1. LM48555 Evaluation Board

Evaluation Board Schematic

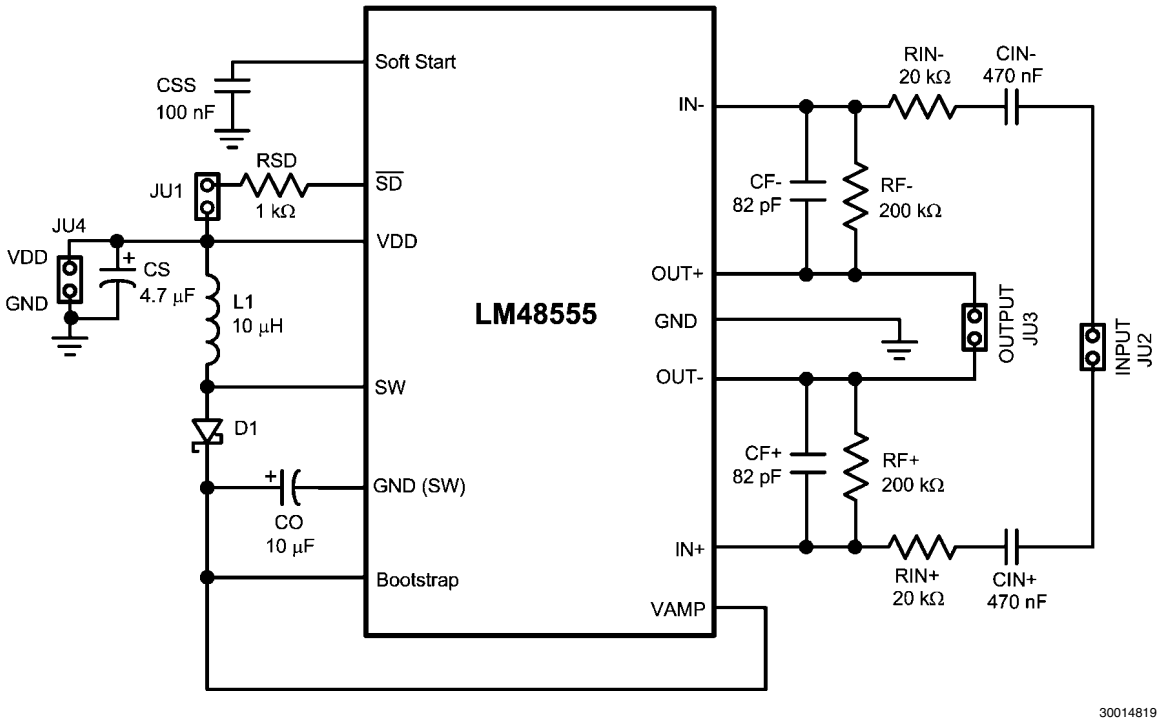


FIGURE 2. Evaluation Board Schematic

Connectors

The LM48555 evaluation boards features connectors for the audio inputs, audio outputs, power supply, and shutdown control. The functionality and designators of each connector are specified in Table 1 below.

TABLE 1. Connectors

Designator	Label	Function
JU1	Shutdown	This connector is used to control the Shutdown function. If JU1 is open, then the LM48555 is in Shutdown. If JU1 is shorted, then the LM48555 is active.
JU2	Audio Input	This connector connects the audio input signal to the device inputs. Apply the positive signal source to the pin labeled "+" and the negative signal source to the pin labeled "-".
JU3	Audio Output	This connector provides a connection to the amplifier outputs. A ceramic speaker load, and series resistors, should be connected across these terminals.
JU4	Power Supply	This connector provides the power supply connection. Apply an external power supply's positive voltage to the pin labeled V_{DD} and the ground source to the pin labeled GND.

Bill of Materials

TABLE 2. Bill of Materials

Designator	Part Description	Manufacturer	Part Number
D2	Diode Schottky 20V 0.5A SOD123	ON Semi	MBR0520LT1G
L1	INDUCTOR 10µH 20% SMD	Taiyo Yuden	NR3010T100M
CIN+, CIN-	Capacitor Ceramic 0.47µF 10V X5R 0402	Murata	GRM155R61A474KE15D
CO	Capacitor Ceramic 10µF 16V X5R 0805	Taiyo Yuden	EMK212BJ106KG-T
CSS	Capacitor Ceramic 0.1µF 25V X5R 0402	Murata	TMK105BJ104KV-F
CF+, CF-	Capacitor Ceramic 82pF 50V 5% C0G 0402	Murata	GRM1555C1H820JZ01D
CS	Capacitor Ceramic 4.7µF 16V X5R 0805	Taiyo Yuden	EMK212BJ475KG-T
RF+, RF-	Resistor 200kΩ 1/16W 1% 0402 SMD	Panasonic	ERJ-2RKF2003X
RIN+, RIN-	Resistor 20kΩ 1/16W 1% 0402 SMD	Panasonic	ERJ-2RKF2002X
RSD	Resistor 1.0kΩ 1/16W 1% 0402 SMD	Panasonic	ERJ-2RKF1001X

Evaluation Board Components

Part number and manufacturer information for the components on the LM48555 evaluation board can be found in the Bill of Materials (Table 2). For more information on component selection refer to the LM48555 datasheet.

PCB Layout Guidelines

High frequency boost converters require very careful layout of components in order to get stable operation and low noise. All components must be as close as possible to the LM4962 device. It is recommended that a four-layer PCB be used so that internal ground planes are available. See Figures 3 through 8 for demo board reference schematic and layout. Some additional guidelines to be observed:

1. Keep the path between L1, D1, and CO extremely short. Parasitic trace inductance in series with D1 and C0 will increase noise and ringing.

2. If internal ground planes are available (recommended) use vias to connect directly to ground at the GND (SW) and GND pins of U1, as well as the negative sides of capacitors CS and CO.

General Layout Recommendations

This section provides practical guidelines for PCB layouts. Designers should note that these are only rule-of-thumb recommendations and the actual results will depend heavily on the final layout.

Power and Ground Circuits

For multi-layer boards, it is important to isolate the switching power and ground trace paths from the amplifier power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major impact on low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will require a greater amount of design time but will not increase the final price of the board.

Avoiding Typical Design / Layout Problems

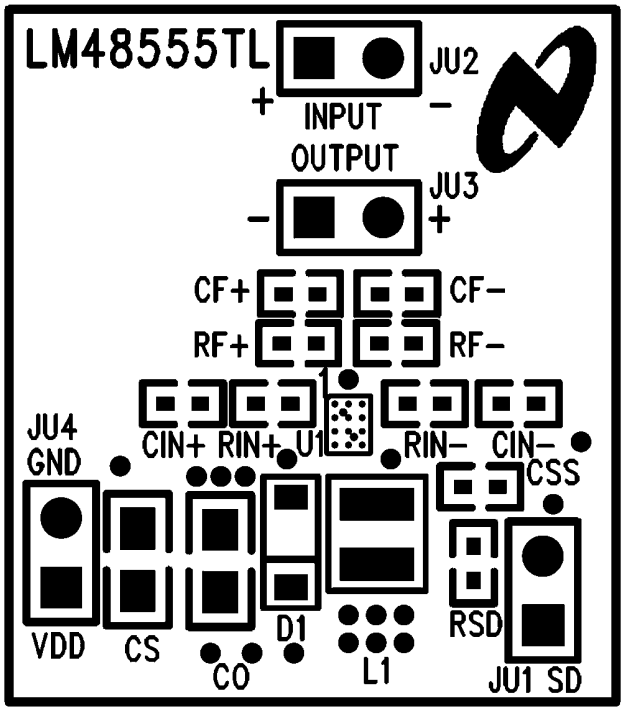
Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other, do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and crosstalk.

Micro SMD Wafer Level Chip Scale Package: PCB, Layout, and Mounting Considerations

Refer to Application Notes (AN-1112) for more information on Micro SMD Wafer Level Chip Scale Package. Since National Semiconductor is constantly pursuing the best package performance possible, please refer to the following web page for possible updates to the µSMD package information:

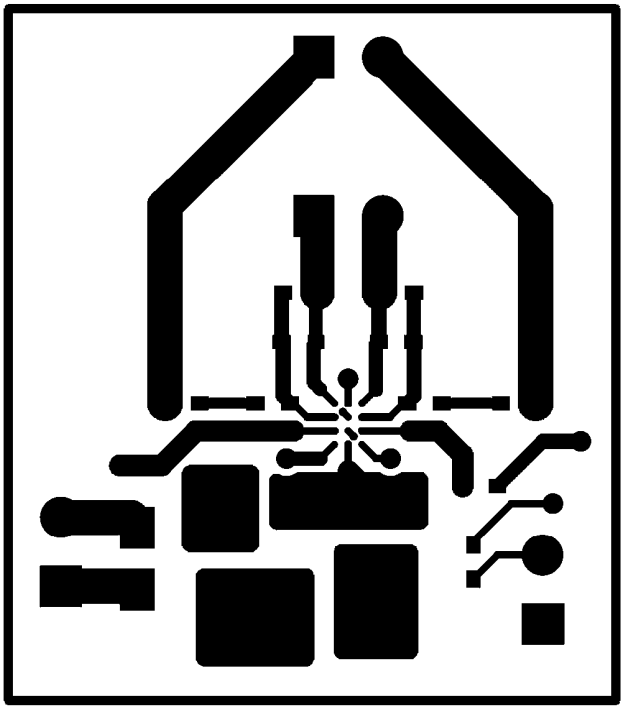
<http://www.national.com/an/AN/AN–1112.pdf.>

PCB Layout



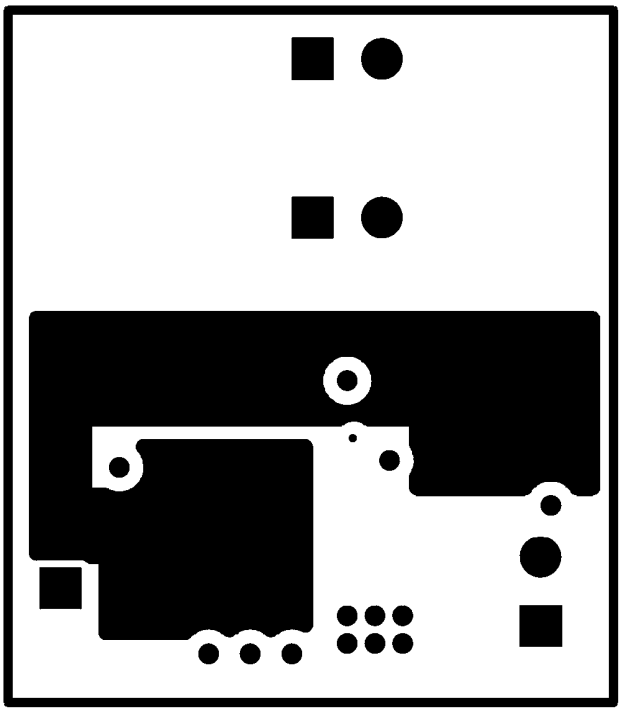
30014813

FIGURE 3. Silkscreen Top



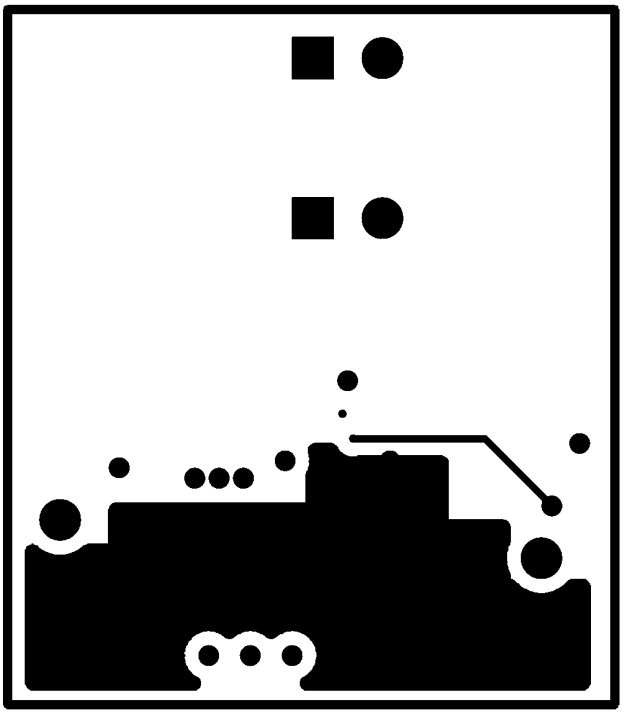
30014814

FIGURE 4. Top Layer



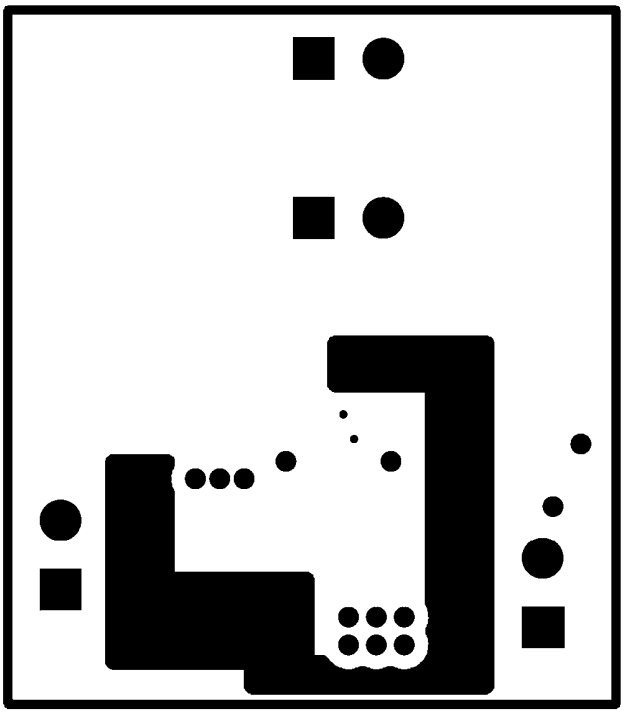
30014815

FIGURE 5. Layer 2



30014816

FIGURE 6. Layer 3



30014817

FIGURE 7. Bottom Layer

30014818

FIGURE 8. Silkscreen Bottom

Revision Table

Rev	Date	Description
1.0	04/03/07	Initial release.

National Semiconductor Americas Customer Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Customer Support Center
Fax: +49 (0) 180-530-85-86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +49 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560