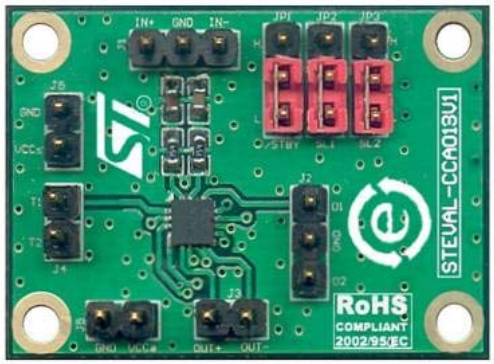
STEVAL-CCA013V1

Mono Class-D audio amplifier with power analog switch demonstration board based on the TS4961T

Data brief

Features

- Power supply range: 2.4 V to 4.3 V
- Audio amplifier standby mode active low
- Ultra high-off-isolation on analog switch: -80 dB typical
- Output power: 1.6 W at 4.2 V into 4 W with 1% THD+N maximum
- Adjustable gain via external resistors
- Low current consumption 2 mA at 3 V
- Efficiency: 88% typical
- Signal-to-noise ratio: 85 dB typical
- PSRR: 63 dB typical at 217 Hz with 6 dB gain
- Thermal shutdown protection
- Break before make delay switching time
- QFN16 package 3mm x 3mm, 450 µm pitch



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Description

This demonstration board is designed to evaluate the TS4961T1, a mono Class-D speaker driver with power audio switch, dedicated to high audio performances and space-constrained applications.

The chip has two functions: the first is an audio Class-D amplifier, and the second is a dual-power analog switch.

Both functions can be used separately (for two different audio channels) or together (to connect two audio sources to one speaker).

Thanks to the output configuration possibilities, the power supply pins, the I/O pins and the standby pins are separated.

It is also possible to control both switches separately.

The TS4961T device is soldered on the two-layer PCB. Both functions previously mentioned can be evaluated separately or together through connectors on the demonstration board.

1 Circuit schematics and BOM list

Figure 1. Schematic diagram

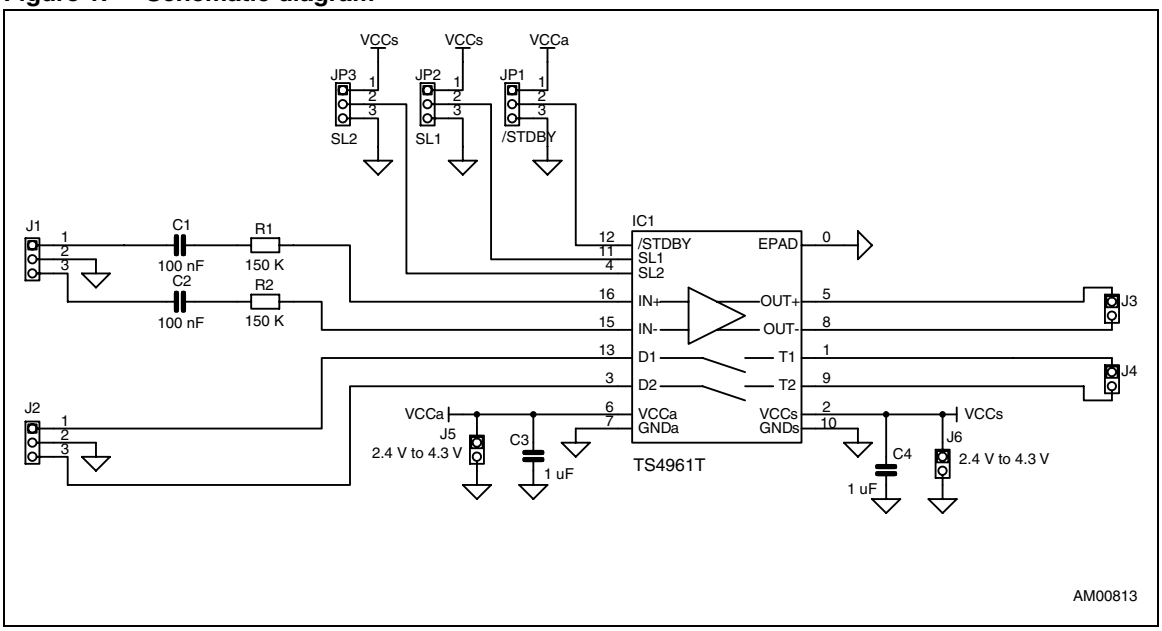


Table 1. Component list for the demonstration board

Name	Quantity	Description
C1, C2	2	100 nF/50 V X7R, +/-10 %, SMD ceramic capacitors, 0603
C3, C4	2	1 µF/10 V X5R, +/-10 %, SMD ceramic capacitors 0603
R1, R2	2	150 K/1 %, 0.063 W, SMD resistors, 0603
J3, J4, J5, J6	4	2-pin header 2.54 mm pitch
J1, J2, JP1, JP2, JP3	5	3-pin header 2.54 mm pitch
IC1	1	TS4961TIQT

2 Demonstration board layout

The following figures show the layers and the top view of the evaluation board.

Figure 2. PCB top overlay

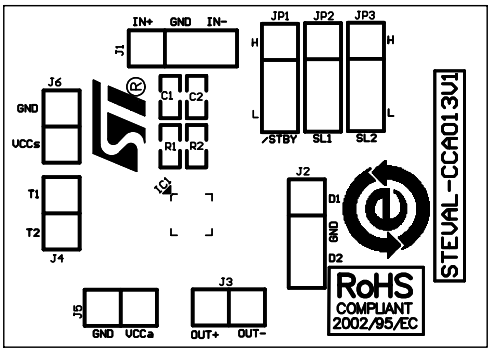


Figure 3. PCB top layer

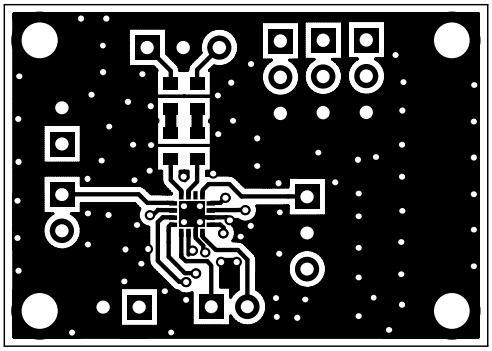


Figure 4. PCB bottom overlay

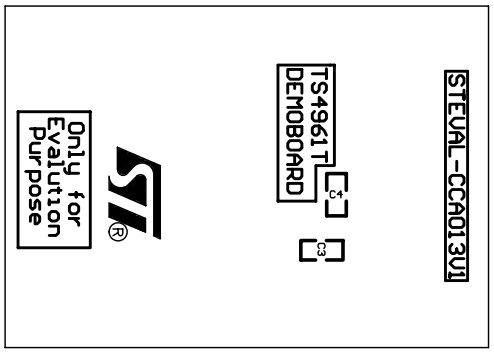
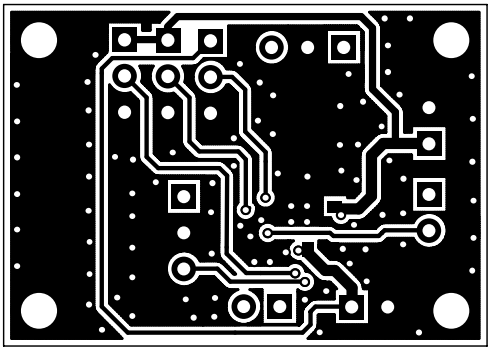


Figure 5. PCB bottom layer



3 Revision history

Table 2. Document revision history

Date	Revision	Changes
04-Jun-2009	1	Initial release.

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