

High IF Receiver Reference Design

National Semiconductor
RD-146
Data Conversions Applications
October 2007



1.0 Design Description

This reference design implements a High IF Receiver circuit that utilizes an LMH6515 DVGA and ADC14V155 Analog to Digital Converter (ADC). The design illustrates variable gain IF amplification and digitization in wireless infrastructure systems and frequency domain analyzers. This flexible subsystem provides excellent sensitivity for input signal frequencies up to 240 MHz. It achieves a small-signal SNR of 72 dBFS and a SFDR greater than 90 dBFS with a 169 MHz input frequency. Large signal performance yields a SNR of 68.3 dBFS and SFDR of 77 dBFS at 169 MHz. In addition to the LMH6515, the design includes National's ADC14V155 14-bit, 155 MSPS ADC with dual data rate, parallel LVDS outputs. The timing is provided by the LMK03001C low-jitter precision clock conditioner with an integrated voltage-controlled oscillator (VCO) that provides 190 femtosecond (fs) jitter over an integration bandwidth of 100 Hz to 20 MHz; as well as several energy-efficient power management ICs.

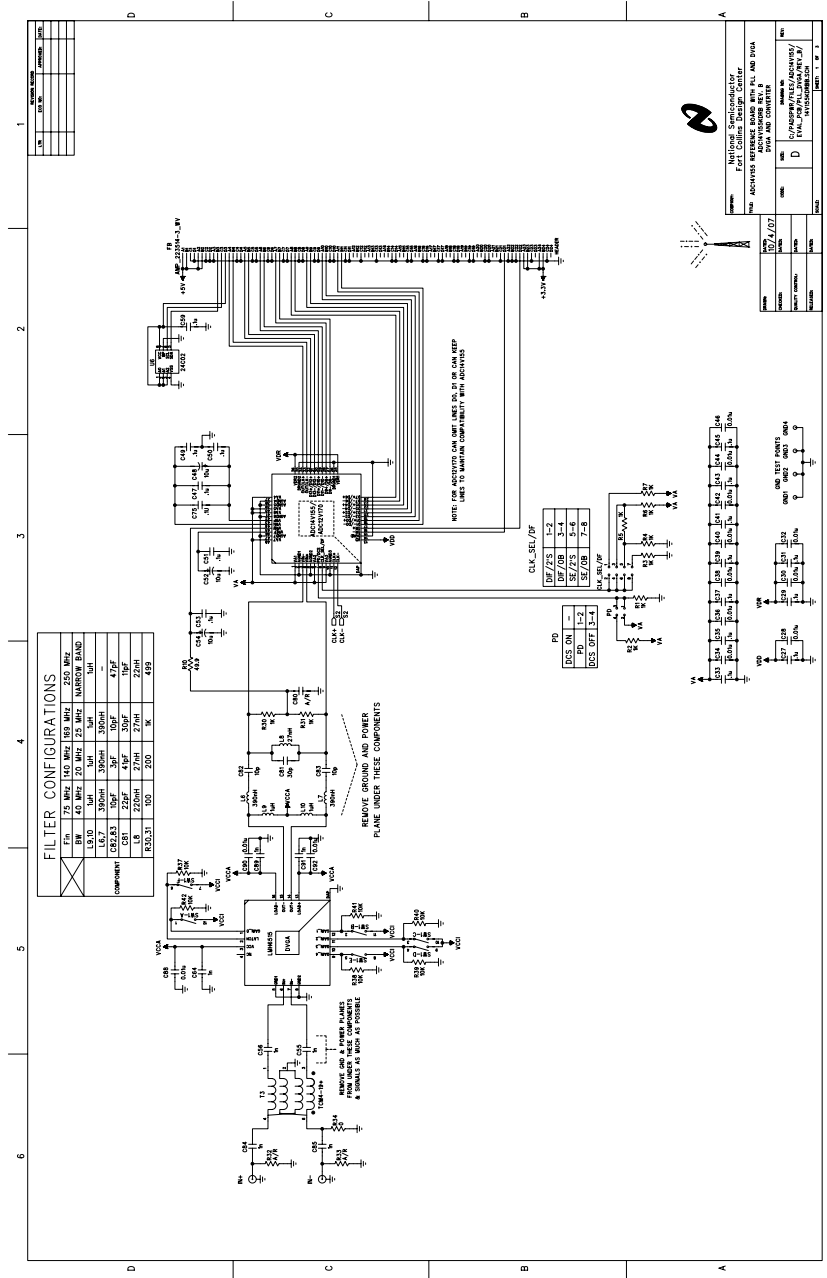
2.0 Features

Key Features of the ADC14V155KDRB High IF Receiver Reference Design Board

- Enables evaluation of a variable gain IF amplification and digitization subsystem with high dynamic range.

- Demonstrates a subsystem architecture used in many wireless infrastructure systems and frequency domain analyzers.
- Configured for an input signal frequency of 169 MHz
- Provides excellent sensitivity for input signal frequencies up to 240 MHz
- **Featured products include :**
 - LMH6515: 450 MHz DVGA with from National Semiconductor's Powerwise® family
 - ADC14V155: 14-bit, 155 MSPS, 1.1 GHz input bandwidth ADC with parallel LVDS outputs from National Semiconductor's Powerwise® family
 - LMK03001C: low-jitter precision clock conditioner with an integrated voltage-controlled oscillator (VCO) from National Semiconductor's Powerwise® family provides 190 fs jitter (100 Hz to 20 MHz integration bandwidth)
 - Several energy-efficient power management ICs from National Semiconductor
- Reference design performance for a 169 MHz input signal
 - Small-signal SNR of 72 dBFS and SFDR greater than 90 dBFS
 - Large signal SNR of 68.3 dBFS and SFDR of 77 dBFS

3.0 Schematic



schematic

FIGURE 1. 14V155KDRBB

schematic 1

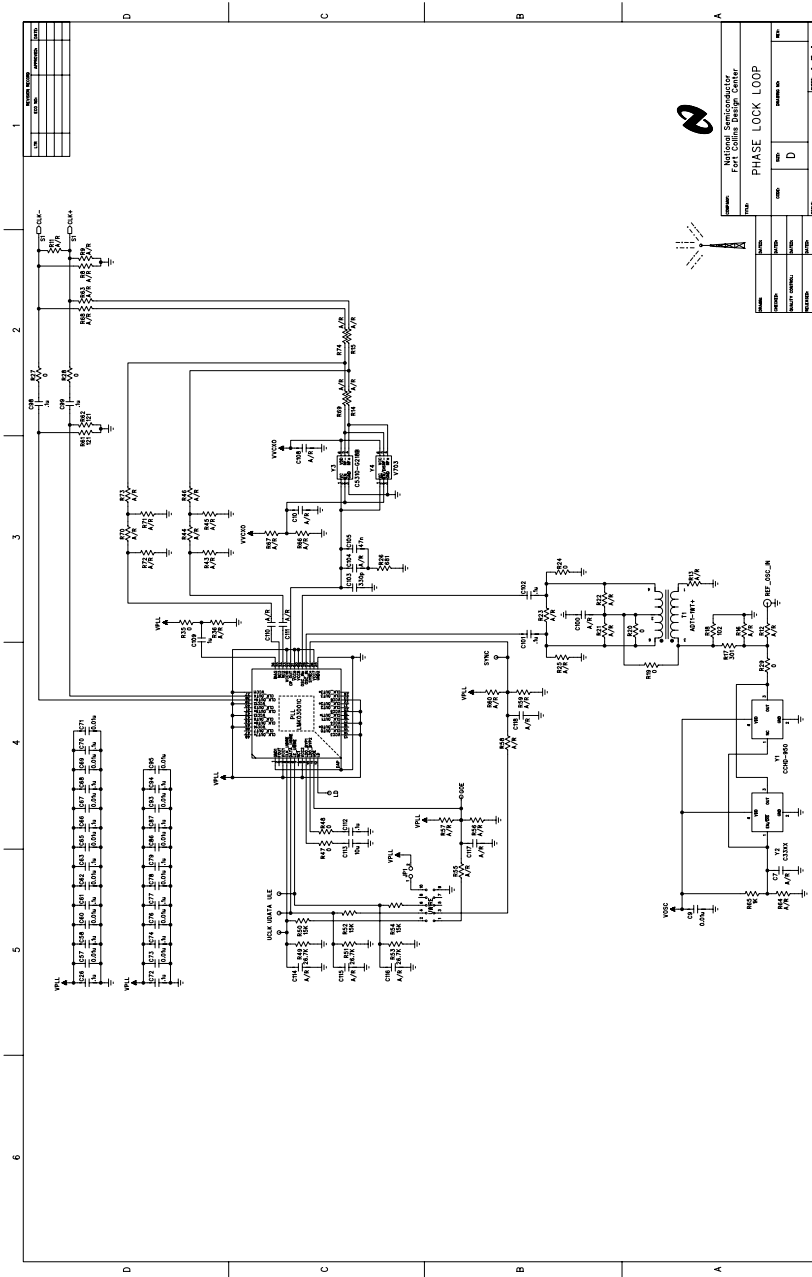


FIGURE 2. 14V155KDRBB

4.0 Bill of Materials

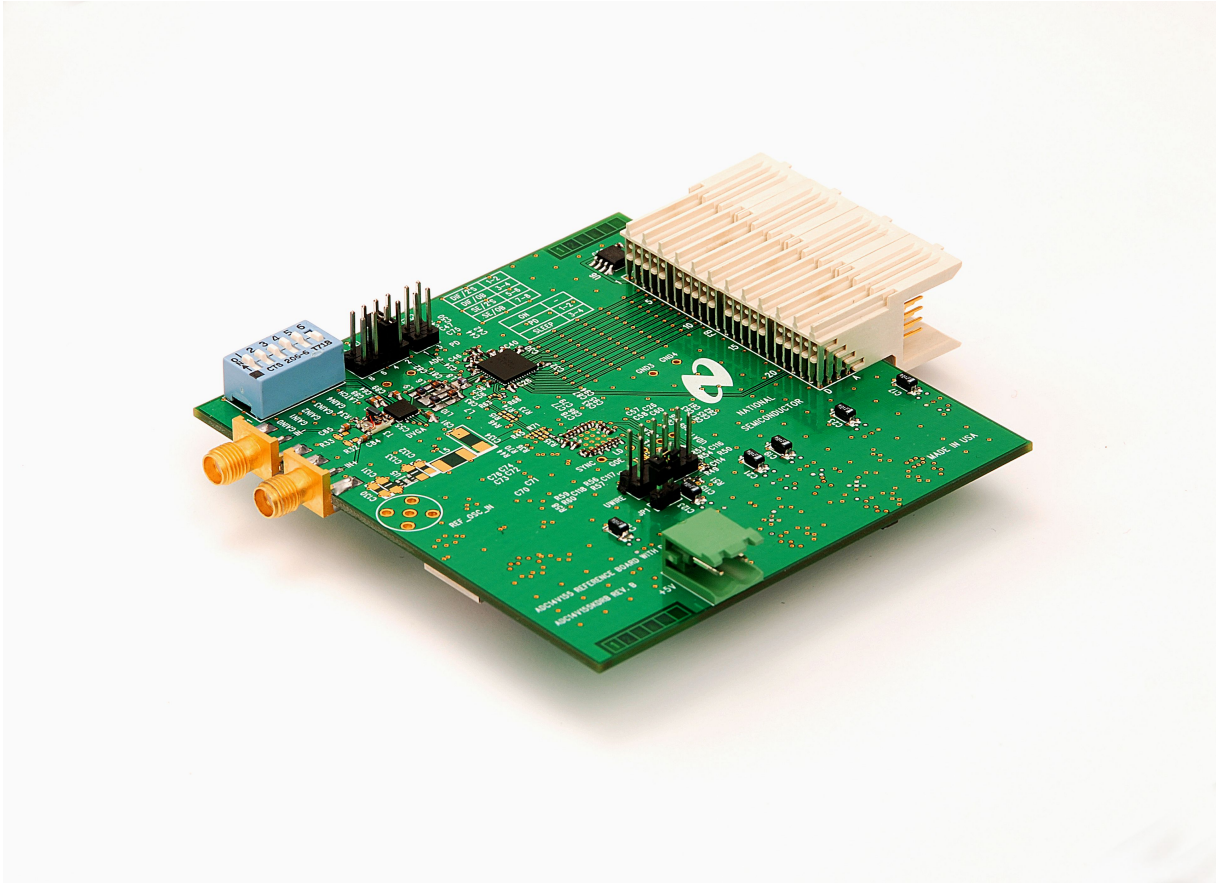
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Item	Quantity	Manufacturer Reference	Manufacturer	Part Description	Manufacturer	Part Number	Notes
1	1	ADC	ATMEL	8-BIT SERIAL EEPROM	ATMEL	24C02	
2	1	CONVERTER	ATMEL	1.44BIT 16-BITS 1.1 GHz BANDWIDTH AD CONVERTER WITH 1.44V REF AND 1.44V REF	ATMEL	AD7124	
3	4	FB	NATIONAL SEMI	2-PACK 2mm (8 Pin) (Pb-Free) 100 Ohm 1% TOLERANCE	NATIONAL SEMI	10000000000	
4	2	FB	TI	100 Ohm 1% TOLERANCE	TI	10000000000	
5	2	CL	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
6	7	CL	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
7	35	CL	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
8	24	CL	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
9	3	CS	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
10	3	CS	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
11	2	CS	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
12	1	CL13	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
13	1	CL13	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
14	1	CL13	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
15	5	CL13	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
16	4	CL13	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
17	4	CL13	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
18	2	CL13	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
19	1	CL13	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
20	1	CL13	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
21	10	CL13	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
22	1	SW1	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
23	1	SW1	TI	0.1 uF 50V 5% TOLERANCE	TI	10000000000	
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FIGURE 4. ADC14155 BOM

boms

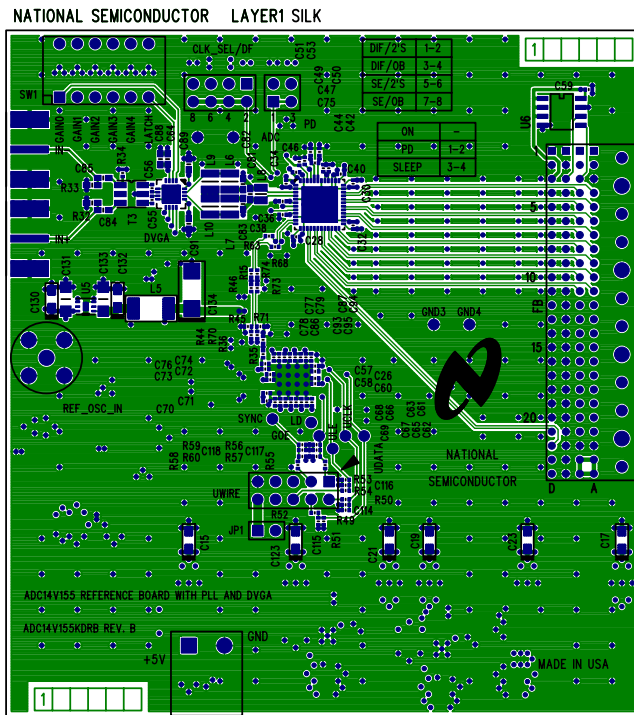
5.0 Board Photos



boardphoto

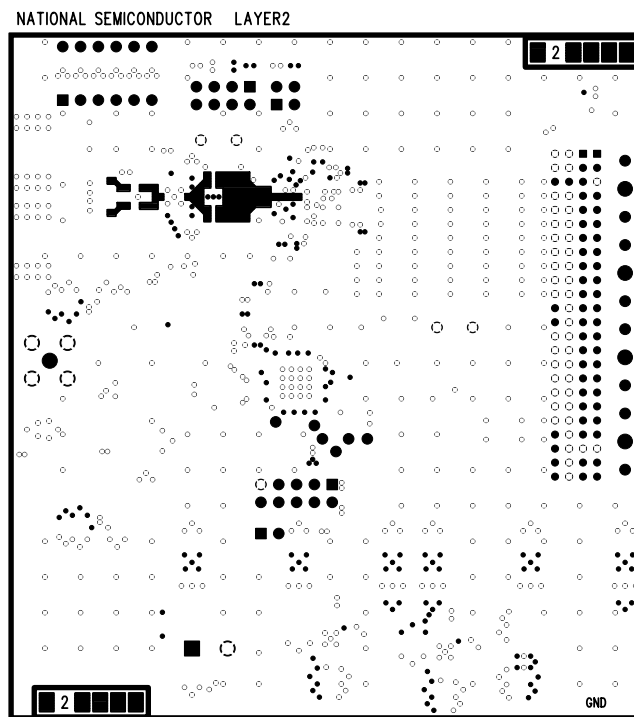
FIGURE 5. ADC14155 Board Photo

6.0 Layouts



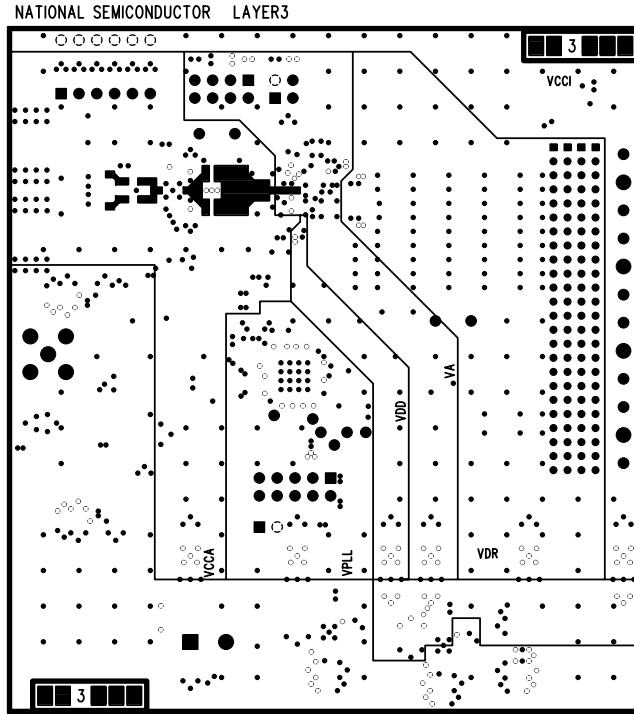
layout21

FIGURE 6. ADC14155 LAYOUT



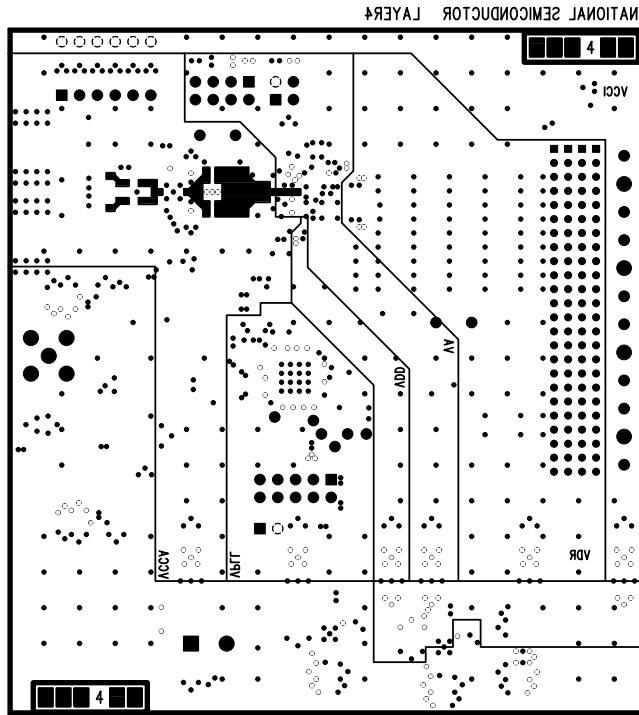
layout22

FIGURE 7. ADC14155 LAYOUT



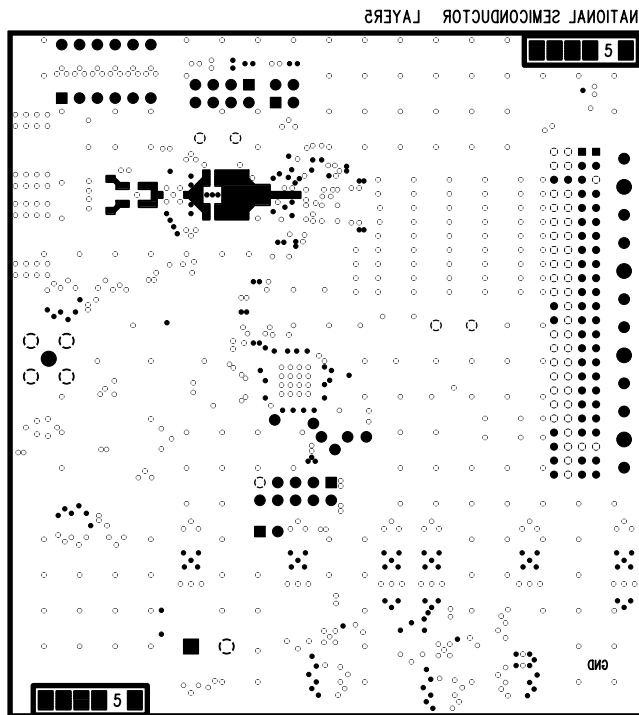
layout23

FIGURE 8. ADC14155 LAYOUT



layout24

FIGURE 9. ADC14155 LAYOUT



layout25

FIGURE 10. ADC14155 LAYOUT

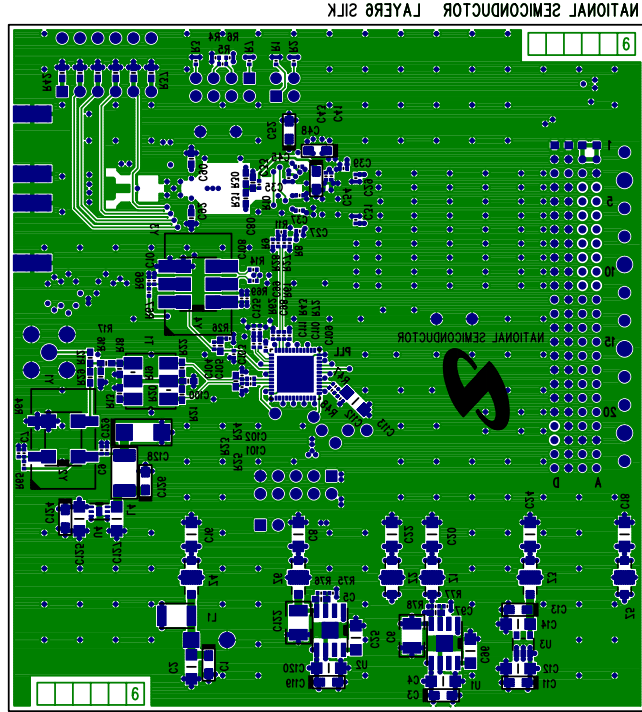


FIGURE 11. ADC14155 LAYOUT

layout26

Notes

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Notes

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