ADC14DS105KARB
Near Zero-IF Receiver Reference Design Board

LMH6552 + ADC14DS105 + LMK02000

User's Guide

National Semiconductor

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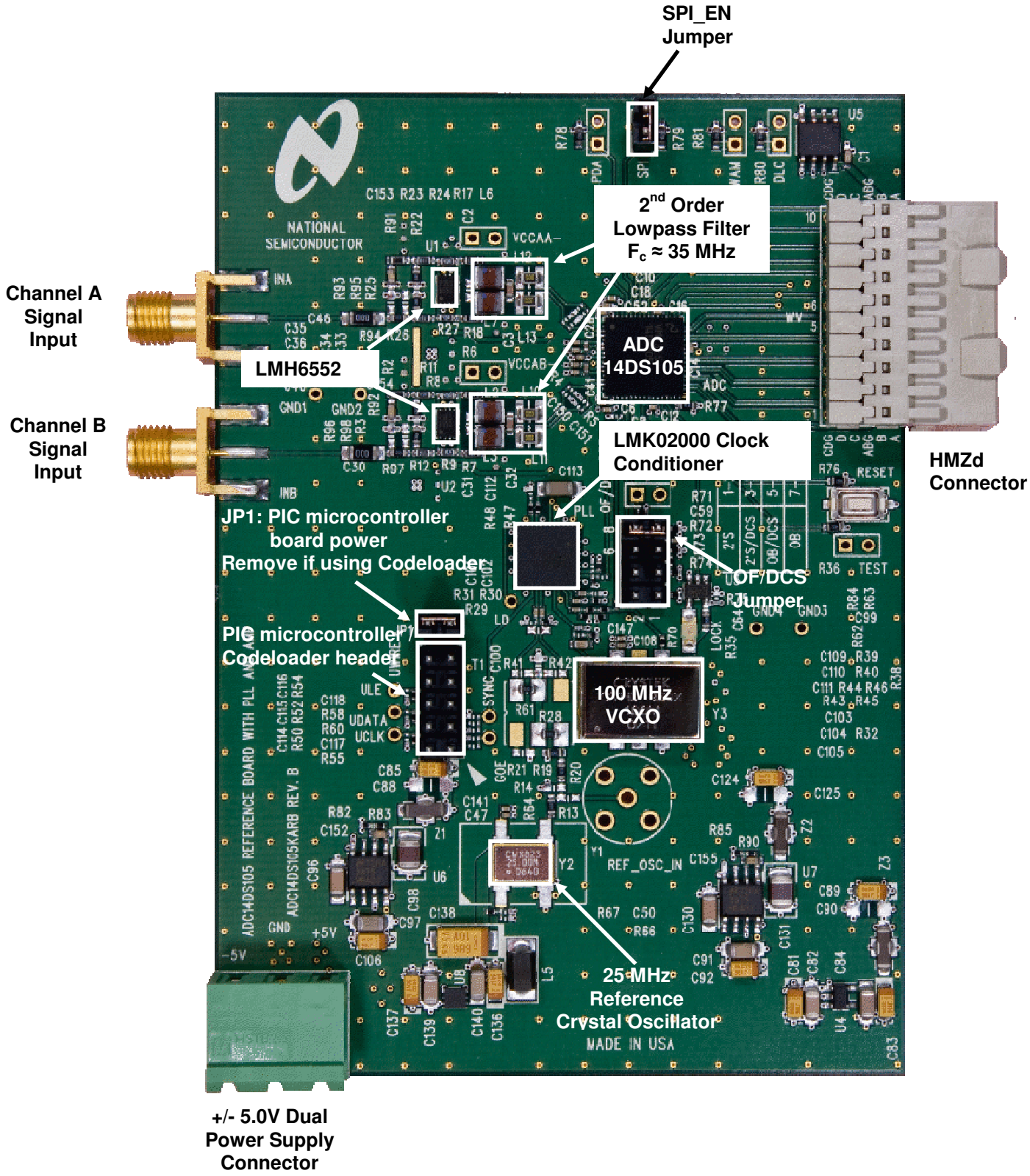

Figure 1. ADC14DS105KARB Component, Connector and Jumper Locations

1.0 Introduction

The ADC14DS105KARB is a near-zero IF receiver reference design board that utilizes the following components from National Semiconductor:

- **Two LMH6552** 1.5 GHz bandwidth differential current feedback amplifiers;
- **ADC14DS105** 14-bit, 1 GHz, Dual 105 MSPS (Megasample per Second) ADC with serial LVDS outputs;
- **LMK02000** low-jitter precision clock conditioner with an integrated phase-locked loop (PLL) that provides 128 femtosecond (fs) jitter over an integration bandwidth of 100 Hz to 20 MHz;
- Several energy-efficient **power management ICs**.

This subsystem reference design utilizes the LMH6552 current feedback amplifier as a differential driver for the ADC14DS105. The sampling clock is provided by a 100 MHz VCXO which is locked to a reference oscillator by the LMK02000.

The 1 GHz input bandwidth of the ADC and the 1.5 GHz differential amplifier gain stage provide excellent performance in this application. The measured performance demonstrates large signal SNR of 73.3 dBFS and SFDR greater than 85 dBFS for input signals up to 25MHz. Figure 2 shows a functional block diagram of the board.

The ADC14DS105KARB uses a dual ADC, demonstrating a quadrature direct conversion or near-zero IF receiver for signal frequencies from DC to 40 MHz. This receiver architecture is commonly used in WiMAX and WCDMA receiver systems.

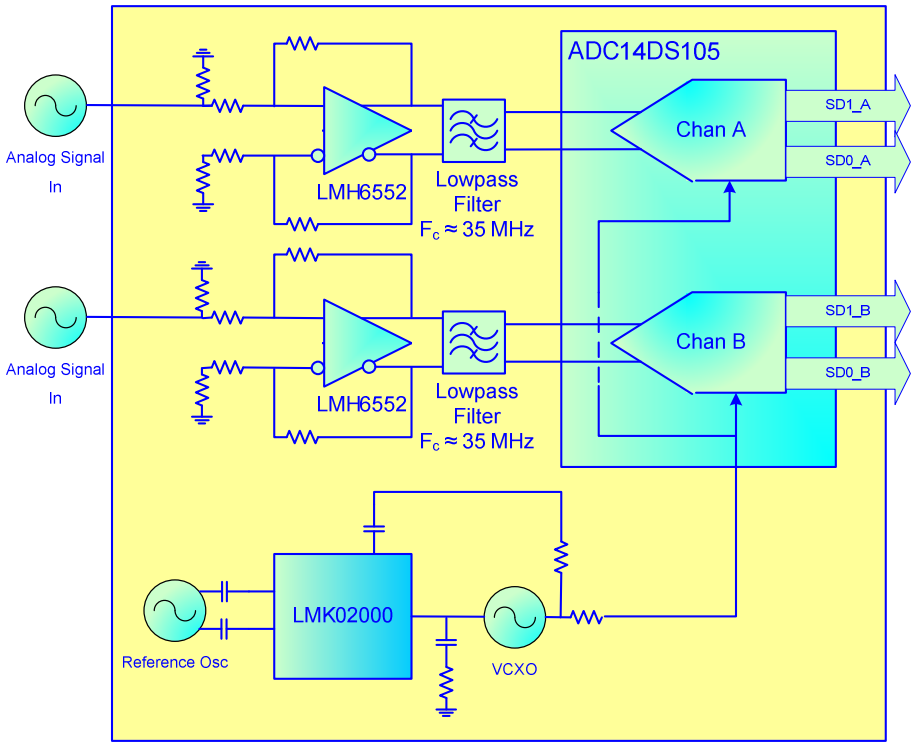

Figure 2. ADC14DS105KARB Block Diagram

2.0 Data Capture

The digital data from the ADC14DS105KARB reference design board can be captured with a suitable instrument, such as a logic analyzer, or with National Semiconductor's WaveVision signal path data acquisition hardware and software platform. The ADC14DS105KARB board can be connected to the data acquisition hardware through the 60-pin connector mounted on the board edge.

The ADC14DS105KARB is compatible with National Semiconductor's WaveVision 5.1 Signal Path Digital Interface Board and associated WaveVision software. Please note that the ADC14DS105KARB board is not compatible with previous versions of the WaveVision hardware (WaveVision 4.x Digital Interface Boards).

The WaveVision hardware and software package allows fast and easy data acquisition and analysis. The WaveVision hardware connects to a host PC via a USB cable and is fully configured and controlled by the latest

WaveVision software. The latest version of the WaveVision software (version 4.3.26) is included in this evaluation kit on a CD-ROM. The WaveVision 5.1 Signal Path Digital Interface hardware is available through the National Semiconductor website (part number: WAVEVSN 5.1).

3.0 Evaluation Kit Contents and Board Assembly

The ADC14DS105KARB evaluation kit includes the following items:

- ADC14DS105KARB reference design board
- PIC microcontroller board (ADC14PIC REV. A)
- CD-ROM with latest WaveVision software (4.3.26)

The ADC14DS105KARB is factory configured for evaluation of input signals up to 35 MHz. Each board is populated with an analog input network which has a lowpass filter with a cutoff frequency of approximately 35 MHz.

The LMK02000, which provides the sample clock for the ADC, must be programmed to correctly configure it for the proper operating frequency. The PIC-microcontroller board (ADC14PIC REV. A) is used to program the registers of the LMK02000 precision clock conditioner chip.

4.0 Quick Start

4.1 WaveVision Software and Hardware Installation

⚠ The WaveVision software must be installed before connecting the WaveVision hardware.

1. Begin by installing the latest version of the WaveVision software (version 4.3.26) which is on the CD-ROM included in this evaluation kit. Do not start the WaveVision software application at this point.
2. Connect the WaveVision 5.1 Digital Interface Board to your PC through the supplied USB cable and apply power to the WaveVision 5.1 board through the +12V AC-DC power adapter included in the WaveVision 5.1 kit. The connection diagram is shown in Figure 3.
3. If this is the first time connecting a WaveVision 5.1 board to your PC, follow the on-screen instructions for installing the drivers for the hardware.
4. Once the WaveVision software and hardware have been installed, the WaveVision software application can be opened.

For more information on installing the WaveVision data acquisition hardware or software, please refer to the Quick Start Guide in the WaveVision User's Guide which can be found on the National Semiconductor website (http://www.national.com/appinfo/adc/evalboards_dataccapture.html).

Please note that the ADC14DS105KARB is only compatible with National Semiconductor's WaveVision 5.1 Digital Interface board.

4.2 Serial Programming Interface (SPI)

The channel and data format modes of the ADC14DS105 can be selected either through the SPI or by direct pin control through the jumpers on the evaluation board. The ADC14DS105KARB evaluation board is delivered with the ADC14DS105 configured for SPI operation.

The serial programming interface enable (**SPI_EN**) pin jumper on the ADC14DS105KARB selects the state of the SPI_EN pin. When the jumper is in place, the pin state is asserted HIGH, the SPI is active and the direct control pins have no effect. When the jumper is removed, the SPI_EN state is LOW, the SPI is deactivated and the ADC modes are pin-controlled through the DLC, WAM, TEST jumpers. The SPI interface is routed through the 60-pin HMZd connector and is controlled through the WaveVision hardware and software when the WaveVision 5.1 data capture hardware is connected and active.

When the ADC14DS105KARB board is connected to the WaveVision 5.1 board, the SPI software control panel shown in Figure 3 will automatically appear. This window should be used to set the modes of the ADC14DS105 when the SPI is enabled. Please ensure that the fields in the window correspond to Figure 3.

⚠ Only the field labeled "Channel" needs to be changed to select between capture from Channel A or Channel B. The other fields in the software control panel should remain unchanged. It is not necessary to click on the "Relock DCMs" button.

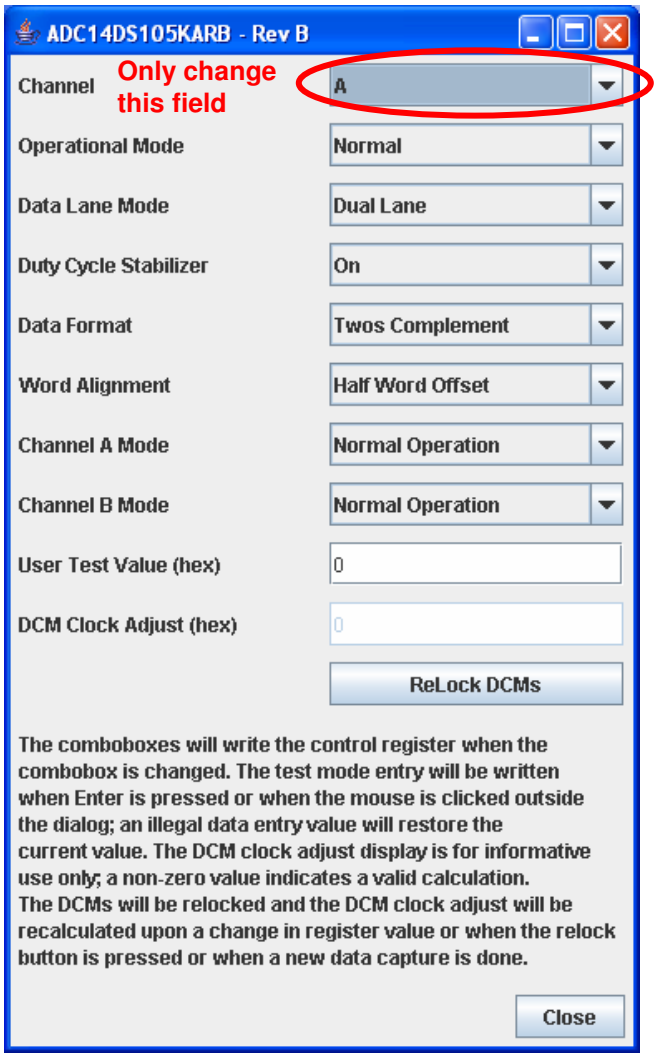

Figure 3. SPI Software Control Panel

4.3 Evaluation Board Jumper Positions

1. **JP1** should have a jumper installed to provide power to the PIC microcontroller board used for programming the LMK02000 registers.

⚠ Remove JP1 if using Codeloader to program the LMK02000 (see Section 5.5 of this guide).

If the SPI_EN jumper is not in place, then the ADC14DS105 is under pin control, and the ADC14DS105KARB board jumpers should be configured as follows. Please refer to Figure 1 for the exact jumper locations.

ADC Control Jumpers

1. The **DLC** pin jumper selects the Dual Lane configuration. When the jumper is in place, the pin is asserted HIGH and all data is sourced on a single lane (SD1_X) for each channel. When the jumper is removed, both channels operate in dual-lane mode and the SD1_X and SD0_X outputs both carry data. This control is disabled when the SPI_EN jumper is installed (SPI is active), as the DLC mode is controlled through the SPI interface.

Jumper position	Description
OPEN	Both ADC LVDS channel outputs operate in dual-lane mode
INSTALLED	ADC LVDS channel outputs operate in single-lane mode

Table 1. DLC Mode Jumper Description (Note: This jumper has no effect when the SPI_EN jumper is installed)

2. The word-alignment-mode (**WAM**) jumper on the front of the board controls the alignment of the sample data words at the ADC outputs. If the DLC mode is single-lane, this jumper must NOT be installed (WAM state is LOW). When the DLC mode is dual-lane (DLC jumper is removed), and the WAM jumper is not installed, the data samples at the SD1_X/SD0_X outputs are offset by one-half sample word. Likewise, when the WAM jumper is installed for dual-lane mode, the data words on SD1_X/SD0_X are time aligned with one another. This pin has no effect when SPI_EN jumper is installed (SPI is active), as the WAM mode is then controlled through the SPI interface.

Jumper position	Description
OPEN	When operating in single lane mode (DLC jumper is installed), this jumper must NOT be installed When operating in dual lane mode, the data samples are offset by one-half word.
INSTALLED	When operating in dual lane mode, the data samples are aligned.

Table 2. WAM Jumper Description (Note: This jumper has no effect when the SPI_EN jumper is installed)

3. The **PDA** and **PDB** jumpers are used to place the ADC14DS105 converters into either power-down or normal operation mode. Table 1 below shows how to select between the power-down modes.

PDx Jumper Settings	Mode
Open	Normal Operation
1-2	Power-down

Table 3. ADC Power-down Jumper Configuration (PDA and PDB)

⚠ If both Channel A and Channel B are powered down at the same time, the ADC14DS105KARB reference board must be power-cycled to recover.

4. The **OF/DCS** pin jumpers select the output data format (2's complement or offset binary) and clock duty cycle correction (active or inactive). Table 2 below shows how to select between the duty cycle correction modes and output data formats. Please note that the ADC14DS105KARB evaluation board is delivered with the ADC14DS105 clock input configured for NO duty cycle correction and Offset Binary output data format (Jumper 7-8).

OF/DCS Jumper Setting	Clock Mode	Output Data Format
1-2	No Duty Cycle Stabilization	2's Complement
3-4	Duty Cycle Stabilization	2's Complement
5-6	Duty Cycle Stabilization	Offset Binary
7-8*	No Duty Cycle Stabilization	Offset Binary

* As assembled from factory. Not observed because ADC14DS105KARB is delivered with the SPI enabled

Table 4. ADC Jumper Settings for ADC Clock Duty Cycle and Output Data Format (OF/DCS)

5. The **TEST** pin jumper selects the state of Test Mode. When the jumper is in place the TEST pin is asserted HIGH and Test Mode is active. A fixed test pattern (10100110001110, msb → lsb) is sourced on all data paths. When the jumper is removed, the ADCs operate in normal mode. This pin has no effect when the SPI_EN jumper is installed (SPI is active), as this the TEST mode is controlled through the SPI interface.

Jumper position	Description
OPEN	The ADC is in normal operation.
INSTALLED	A fixed test pattern is output (10100110001110 msb → lsb)

Table 5. TEST Jumper Description

Amplifier Power Jumpers

1. The **VCCAA-** and **VCCAB-** jumpers are used to select the power supply configuration for the amplifiers. The evaluation board is shipped from the factory in the dual power supply configuration (+/- 5V), so these jumpers are not installed. If single supply operation is desired (+5VDC only), these jumpers should be installed.

Jumper position	Description
OPEN	Dual power supply operation
INSTALLED	Single power supply operation

Table 6. VCCAA- and VCCAB- Jumper Description

ADC Sample Clock Programming

The LMK02000, which provides the sample clock for the ADC, must be programmed to correctly configure it for the proper clock frequency. The programming can be accomplished by either one of two methods.

The first method is to attach a small PIC-based module that is included in this evaluation kit. This module is plugged onto the 10-pin header labeled "UWIRE" as described in Section 4.4 of this user's guide. If this module is used, the JP1 jumper must be installed to provide power from the main board to the PIC module.

The second method for programming the LMK02000 uses the 10-pin "UWIRE" header to connect the LMK02000's serial programming interface (DATA, CLK, LE) to a PC. To use this programming interface, a special parallel port (LPT) cable supplied by National Semiconductor allows the device to be directly programmed with a PC using National Semiconductor's Codeloader software. The serial programming interface can also be programmed over the USB port of the PC. To program the LMK02000 through the USB port, a separate interface board is available from National Semiconductor. See http://www.national.com/appinfo/interface/clk_conditioners.html to download Codeloader, obtain a user's guide and to order any necessary hardware such as programming cables or USB interface boards.

⚠ Remove JP1 if using Codeloader to program the LMK02000.

4.4 Connecting Power and Signal Sources

1. Connect the ADC14DS105KARB reference board to the WaveVision 5.1 board through the FutureBus connector as shown in Figure 4. The ADC14DS105KARB reference board should not be powered up, as the WaveVision hardware does not support hot-swapping of boards.
2. With the WaveVision software running, power-up the WaveVision 5.1 board, and the WaveVision software will automatically load the appropriate firmware to allow data capture from the ADC14DS105KARB. Allow the firmware file to finish downloading before continuing.

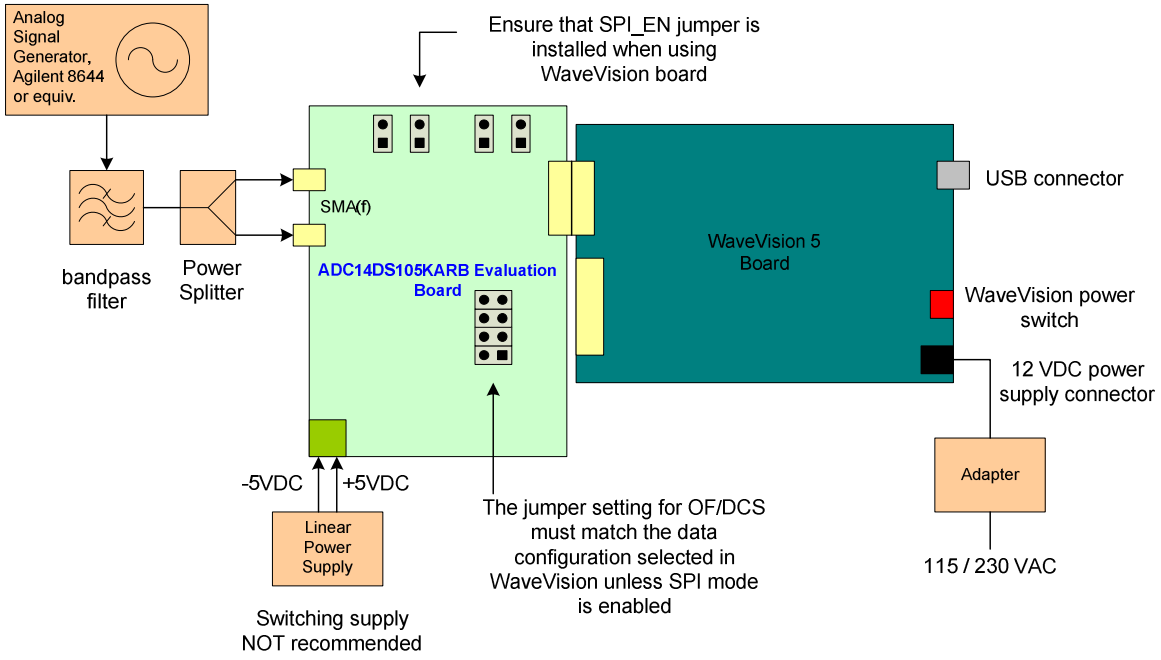

Figure 4. Connection Diagram for ADC14DS105KARB and WaveVision 5.1 Data Capture Hardware

3. Plug the PIC microcontroller board onto the dual-row header labeled "UWIRE" as shown in Figure 5. Align the arrows on the two boards to ensure proper orientation. JP1 should have a jumper installed on the main board to provide power to the PIC microcontroller board. Lastly, flip the switches on the PIC microcontroller board to the following positions: Switch 1 = OFF, Switch 2 = OFF.

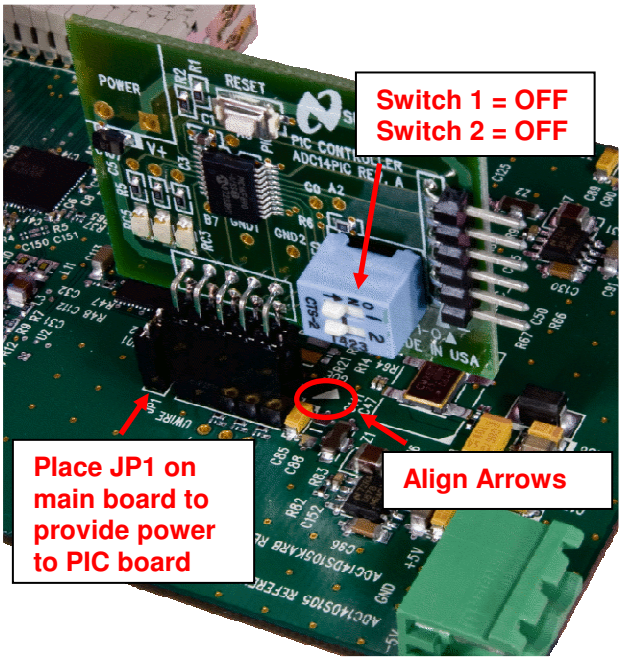

Figure 5. PIC microcontroller Board Connection and Configuration

4. Connect a 5.0V dual power supply (+/- 5.0V) capable of supplying up to 1A to the green power connector which is located along the bottom edge of the ADC14DS105KARB board. This is shown in Figure 3. Ensure that the polarity of the wires going to the green power connector match the "+5V", "-5V" and "GND" labels on the evaluation board. Turn on the +/- 5V supply.
5. The single-ended analog signal inputs are provided by board-edge SMA(f) connectors labeled "INA" and "INB". The input impedances are 50 ohms. The maximum amplitude (Vp-p) for satisfactory performance is 1 Vp-p. The inputs are DC-coupled but the input signal may be either DC or AC coupled. If DC coupled, the DC level of the signal should not exceed 1.2 V. The DC level is set on the ADC14DS105KARB reference board. Connect the signal source through the SMA connector as shown in Figure 1 and Figure 4. Recommended signal generators are the HP8644B (HP/Agilent) or the SMA100A (Rohde & Schwarz). A bandpass filter between the signal generator output and the ADC14DS105KARB SMA connector is required to measure the true performance of the board. See Figure 4.
6. Set the signal source to the desired frequency (up to ~35 MHz) and the input amplitude to 0dBm. The signal generator amplitude will need to be adjusted during evaluation to obtain the desired signal amplitude at the ADC input.
7. Press the "RESET" button on the PIC microcontroller board to load the register settings

into the LMK02000. The three LED's on the PIC microcontroller board will flash to indicate that the register bits have been sent to the LMK02000. At this point, the board should be ready to capture digital data.

8. Capture the data and display the FFT of the captured data with the WaveVision software. A shortcut for capturing data and displaying the FFT plot in WaveVision is to use the "alt-c" key stroke combination.

4.4 ADC14DS105KARB Reference Board Performance

The following plots show the typical (not guarateed) performance of the ADC14DS105KARB reference board at a sample rate of 100 MSPS.

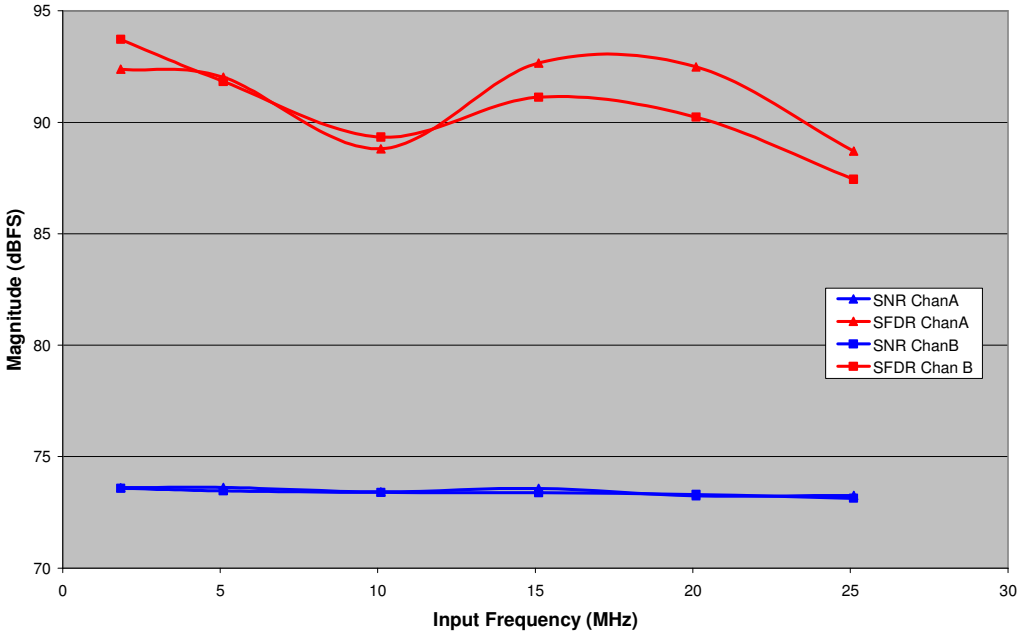

Figure 6. ADC14DS105KARB Typical SFDR and SNR Performance vs. Input Frequency (Amplitude at the ADC input is -1dBFS)

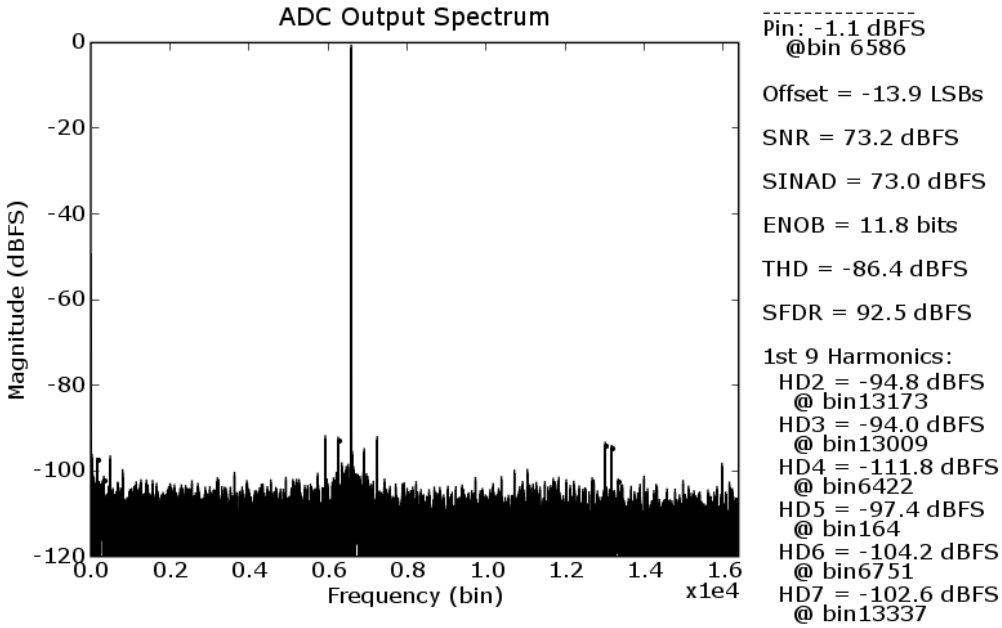

Figure 7. ADC14DS105KARB Typical FFT for Input Frequency of 20 MHz and Amplitude of -1dBFS (at ADC input)

5.0 Functional Description

5.1 Dual Analog Inputs with LMH6552 High Speed Differential Amplifier

This evaluation board is configured to accept dual analog inputs via SMA(f) connectors. Figure 8 illustrates the input configuration for the amplifiers. The inputs are 50 ohms, DC-coupled. Each input drives an LMH6552 differential amplifier that is configured for the single-ended-to-differential mode conversion. The VCOM output of the ADC (ADC14DS105) is used as the common mode input to the amplifier. Each amplifier is configured for 6 dB of gain, so the maximum input signal level is 1 Vp-p, producing 2Vp-p at the output of the amplifier. It is recommended that the amplifiers be powered by dual supply rails (+/- 5VDC), but the board can also be configured to operate in single supply mode by installing jumpers at VCCAA- and VCCAB-. Please refer to the LMH6552 datasheet for a description of operating the LMH6552 with a single supply. To obtain the best distortion results (best SFDR), a low noise signal generator such as the HP8644B (HP/Agilent) or SMA100A (Rohde & Schwarz) is recommended to drive the signal inputs of the evaluation board. The output of the signal generator should be bandpass filtered to suppress any harmonic distortion produced by the signal generator and to allow accurate measurement of the noise and distortion performance. See Figure 4. The low pass filter ($F_c \approx 35$ MHz) following the LMH6552 will further improve the noise performance of the ADC by filtering the broadband noise of the signal generator.

5.2 Bandpass Anti-Aliasing Filter

The output of the LMH6552 amplifier drives a passive 2nd order lowpass filter with $F_c \approx 35$ MHz as shown in Figure 8. The filter output is sampled by the analog to digital converter. The combined channel response of the differential amplifier, bandpass filter and ADC is shown in the Figure 9.

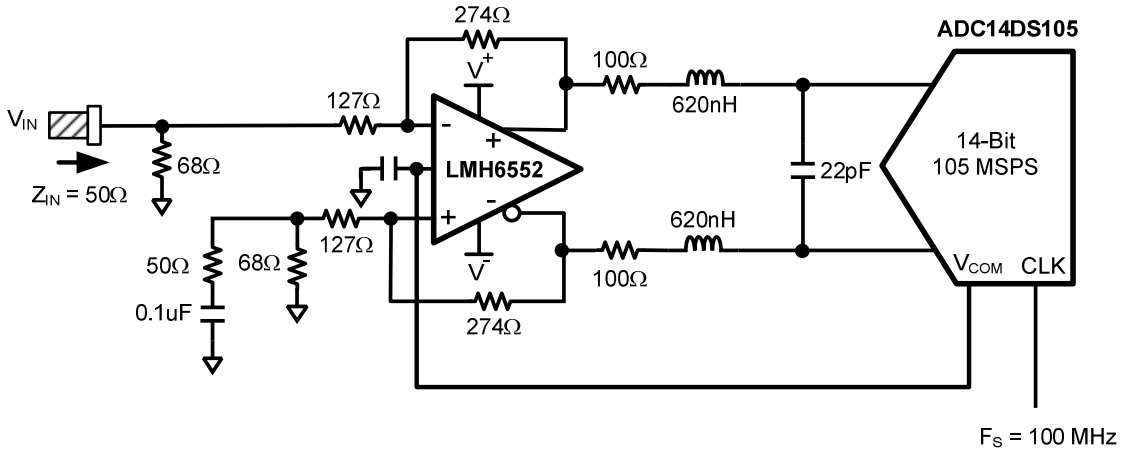

Figure 8. Analog Input Circuit for ADC14DS105KARB

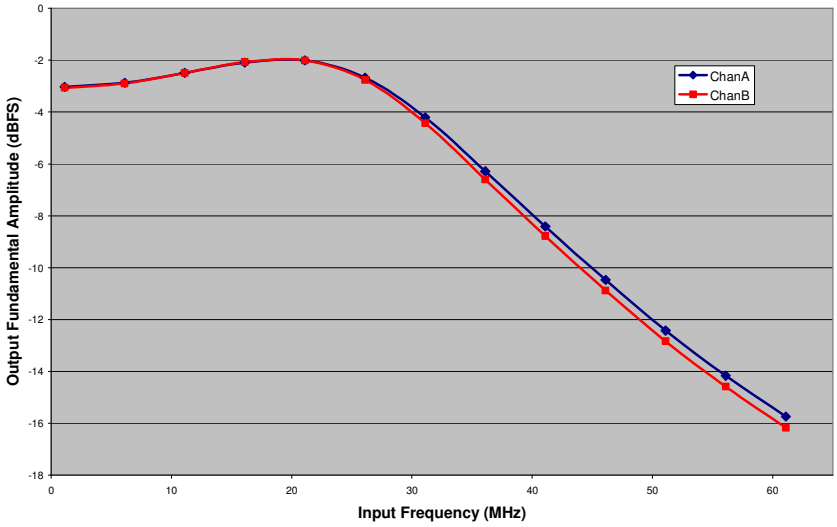

Figure 9. 2nd Order Lowpass Filter Profile for ADC14DS105KARB

5.3 ADC Reference

The internal 1.2V reference on the ADC14DS105 is used in this reference design. This is the recommended reference configuration for the ADC14DS105.

5.4 Clock Input

The ADC clock used to sample the analog inputs is generated using a VCXO controlled by the LMK02000 Precision Clock Conditioner. The LMK02000 is gives the user an ultra-low noise phase-locked loop (PLL) paired with a clock distribution section that provides 5 LVPECL outputs and 3 LVDS outputs (all differential). Though not used in this design, each clock output channel on the LMK02000 contains a divider block and delay adjustment clock. The LMK02000 is typically paired with a low jitter VCXO, in this case the Crystek model CVHD-950X-100.0, which provides a single-ended CMOS clock driving the ADC clock input. On the ADC14DS105KARB evaluation boad, the LMK02000 PLL locks this VCXO to a 25 MHz reference oscillator (Connor-Winfield model CWX823). Figure 10 shows a block diagram of the clocking circuit on the ADC14DS105KARB reference board. The PLL counters, phase detector and charge pump of the LMK02000 are programmed using the PIC microcontroller board as discussed in Section 4.4 of this guide.

The LMK02000 achieves 128 fs RMS jitter (integrated from 100 Hz to 20 MHz). Figure 11 illustrates the phase noise performance of the clock, measured at CLKout4 of the LMK02000.

The single-ended clock signal from the VCXO is applied to the CLK input on the ADC14DS105.

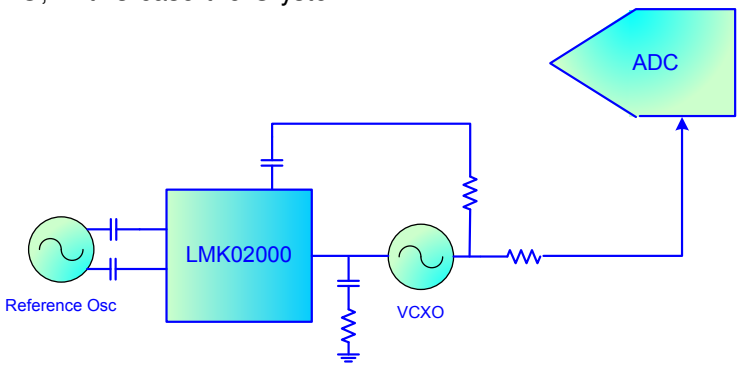

Figure 10. Clocking Circuit for ADC14DS105KARB

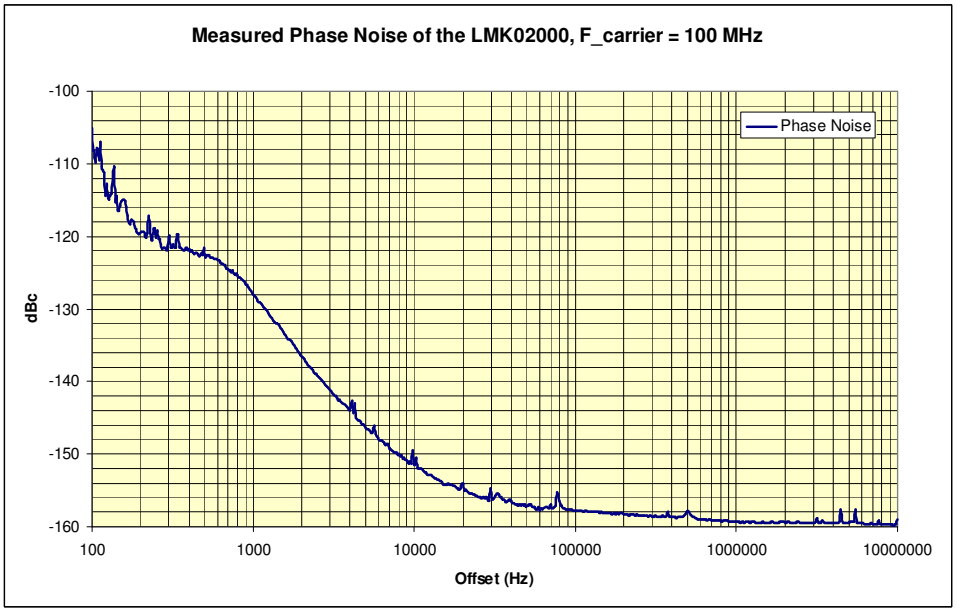

Figure 11. LMK02000 Phase Noise Performance, 100 MHz, Measured at CLKout4

5.5 LMK02000 Programming

The LMK02000, which provides the sample clock for the ADC, must be programmed to correctly configure it for the proper clock frequency. The programming can be accomplished by either one of two methods.

The first method is to attach a small PIC-based module that is included in this evaluation kit. This module is plugged onto the 10-pin header labeled "UWIRE" as described in Section 4.4 of this user's guide. If this module is used, the JP1 jumper must be installed to provide power from the main boad to the PIC module. The PIC module will program the LMK02000 to lock the 100MHz VCXO to a reference of 25 MHz.

The second method for programming the LMK02000 uses the 10-pin "UWIRE" header to connect the LMK02000's serial programming interface (DATA, CLK, LE) to a PC. To use this programming interface, a special parallel port (LPT) cable supplied by National Semiconductor allows the device to be directly programmed with a PC using National Semiconductor's Codeloader software. The serial programming interface can also be programmed over the USB port of the PC. To program the LMK02000 through the USB port, a separate interface board that is available from National Semiconductor is required. See http://www.national.com/appinfo/interface/clk_conditioners.html to download Codeloader, obtain a user's guide and to order any necessary hardware such as programming cables or USB interface boards.

⚠ Remove JP1 if using Codeloader to program the LMK02000.

The procedure for programming the LMK02000 through National's Codeloader software and special parallel port cable is described here if the user intends to program the ADC14DS105KARB reference board for sampling rates other than 100 MSPS. Please note that the VCXO and possibly the loop filter components must be changed to achieve sampling rates other than 100 MSPS.

The following figures illustrate the Codeloader configuration screens and their contents required to properly program the LMK02000 Clock Conditioner using either a parallel port or USB PC interface with appropriate cable. These configuration screens are for programming the LMK02000 to lock a 100 MHz VCXO to a 25 MHz reference, which is the same configuration used on the ADC14DS105KARB reference board. The settings below are programmed using the PIC-module included in this evaluation kit.

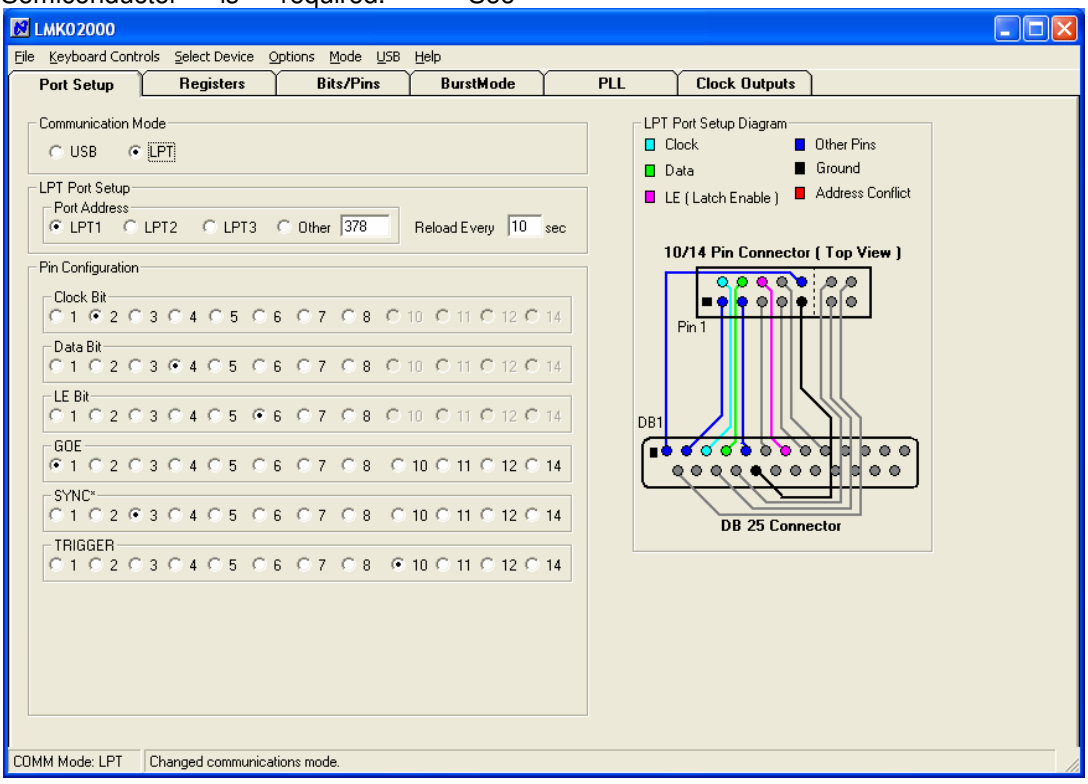

Figure 12. LMK02000 Codeloader software communication port setup for programming

⚠ It should be noted that the user may be required to select a different LPT port that is compatible with the capabilities of the PC being used to program the device. Using the USB port requires a separate interface board, available from National Semiconductor.

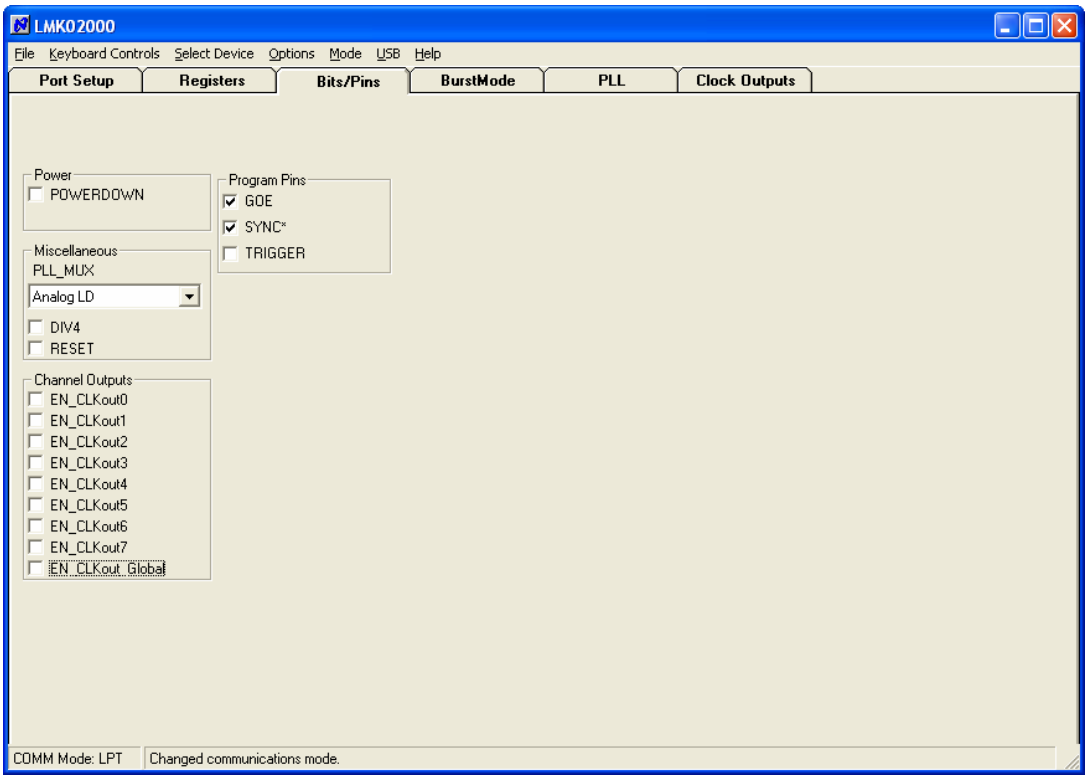

Figure 13. LMK02000 Codeloader configuration, Bits/Pins tab.

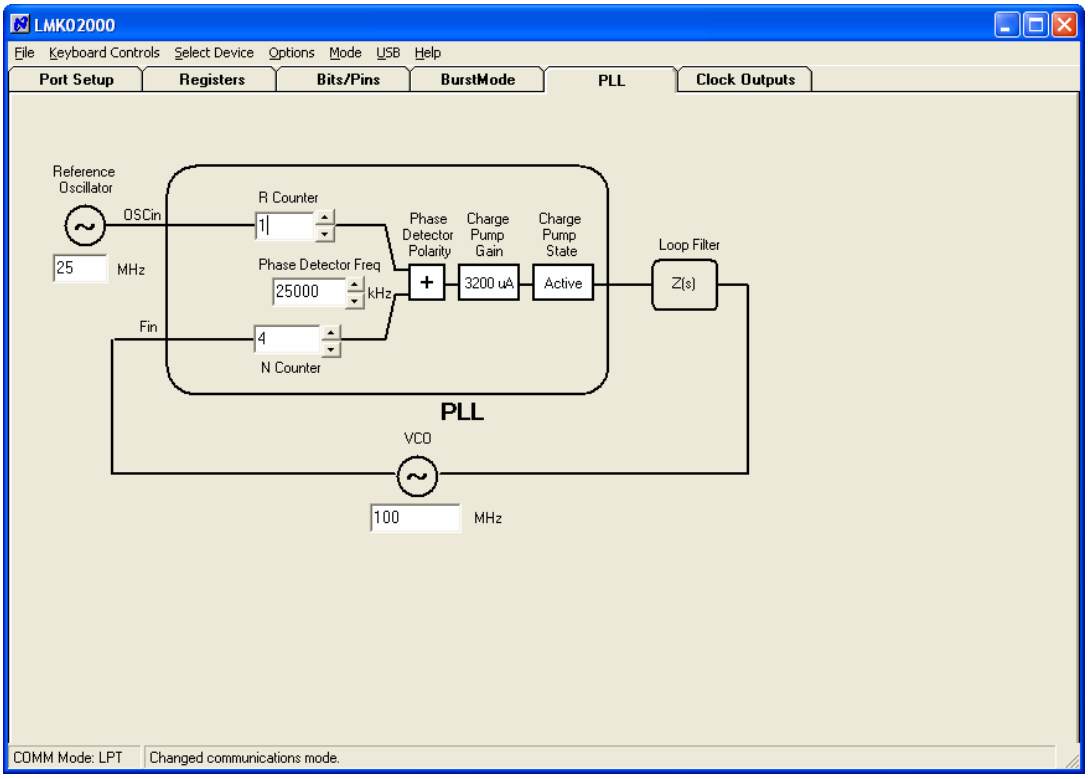

Figure 14. LMK02000 Codeloader configuration, PLL tab.

Note: Using PLL parameter values different from the values shown in Figure 14 may result in degraded performance of the reference board.

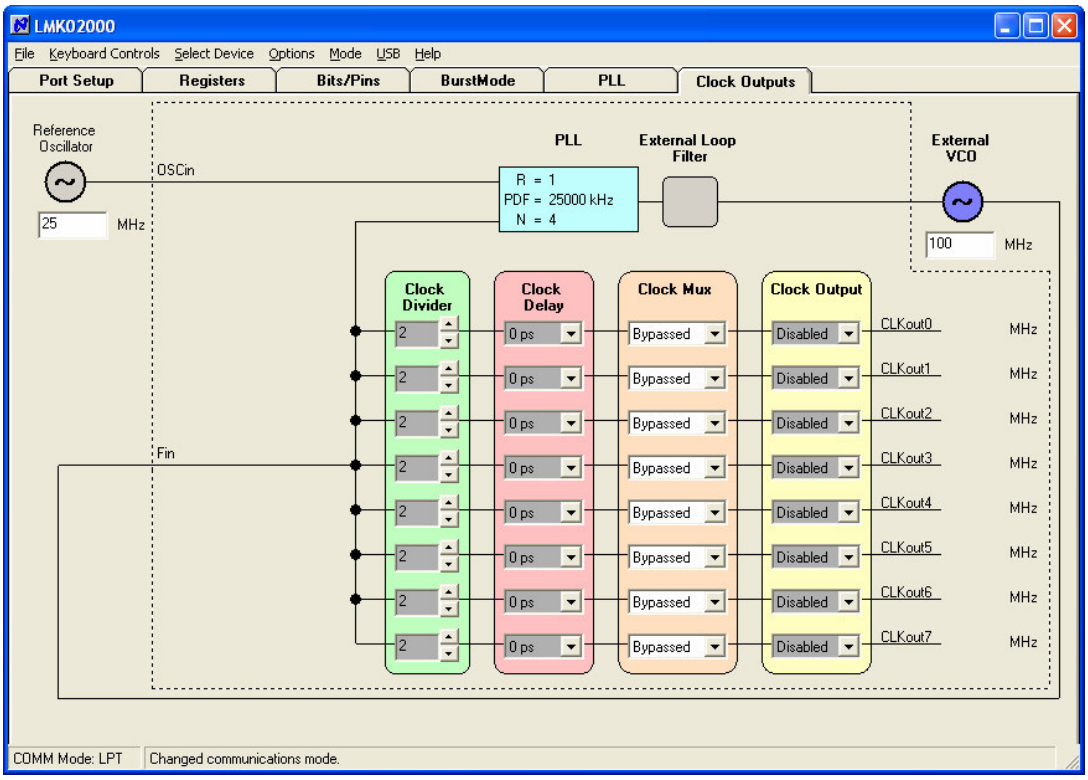

Figure 15. LMK02000 Codeloader configuration, Clock Outputs tab.

Note: The LMK02000 clock outputs are not accessible on the ADC14DS105KARB evaluation board. See http://www.national.com/appinfo/interface/clk_conditioners.html for information on acquiring the LMK02000 Evaluation board, which provides full access to all clock outputs on the LMK02000.

5.6 Board Outputs

Each analog channel is sampled by the dual channel ADC14DS105 analog to digital converter (ADC) on the rising edge of the sample clock. The 14-bit digital samples from each ADC channel are serially clocked out of one (single-lane mode) or two (dual-lane mode) low-voltage-differential-signalling (LVDS) outputs. The samples from converter Channel A appear on SD1_A+/- (single-lane mode) or on both SD1_A+/- and SD0_A+/- (dual –lane mode). Likewise, the samples from Channel B appear on SD1_B+/- (single-lane mode) or on both SD1_B+/- and SD0_B+/- (dual –lane mode). On the evaluation board, these outputs are routed to the 60-pin connector. When the evaluation board is mated with a WaveVision 5 board that is connected to a PC USB port, the samples are buffered on the WaveVision board and then processed by the WaveVision application software running on the PC.

The sample format is configured by the control panel in the WaveVision software or by the jumper on the 8-pin header labeled "OF/DCS". See Section 3.1 for further details.

Please see the ADC14DS105KARB Reference Board schematic in Section 6.0 of this guide and the ADC14DS105 datasheet for further details.

5.7 Power requirements.

Power to the ADC14DS105KARB evaluation board is supplied through the green power connector which is located along the bottom edge of the board. A dual 5V supply (+/- 5.0V) capable of delivering up to 1.0A is required.

6.0 Evaluation Board Schematic

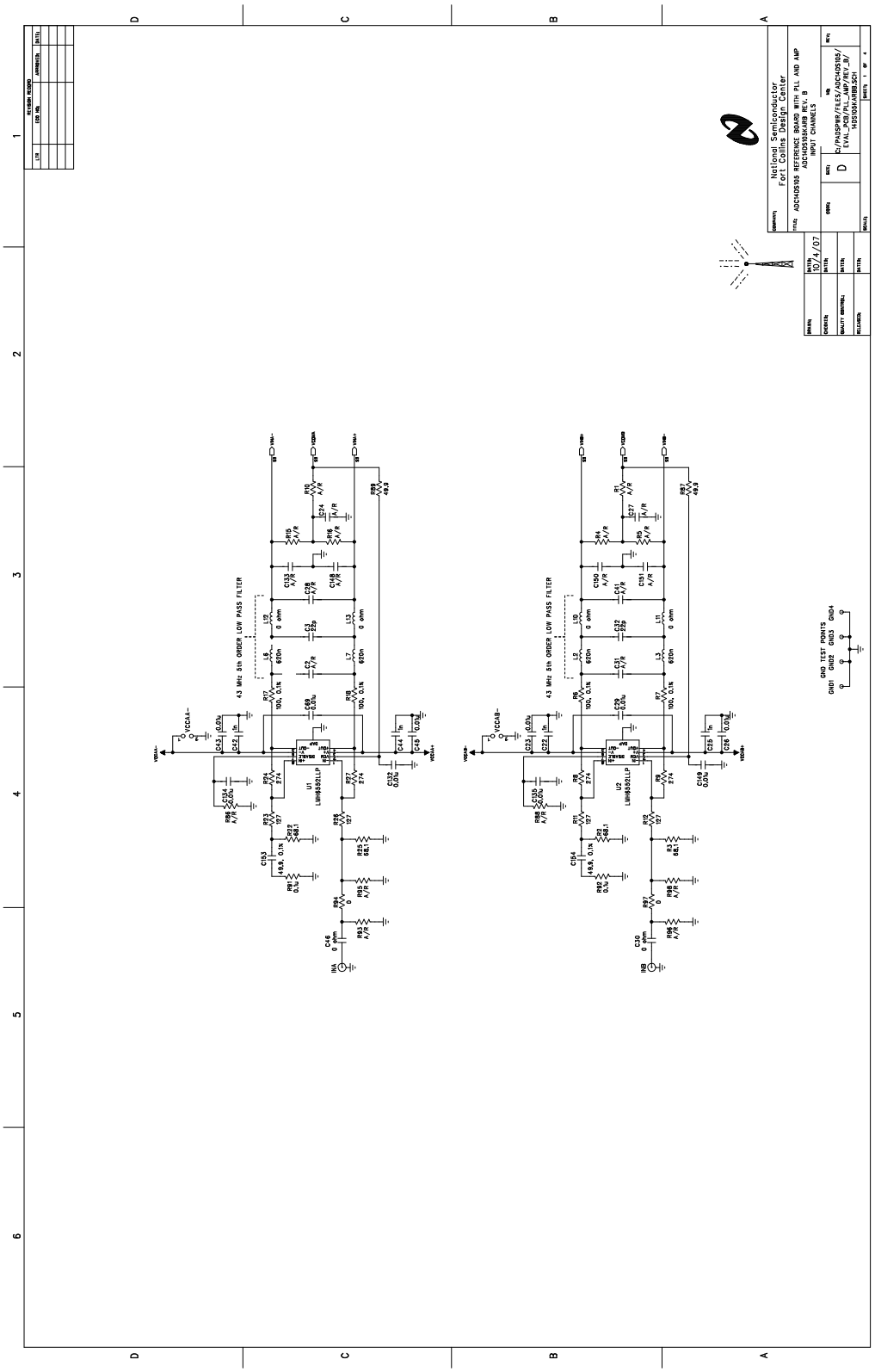

Figure 16. Input Channels With LMH6552

6.0 Schematic (cont.)

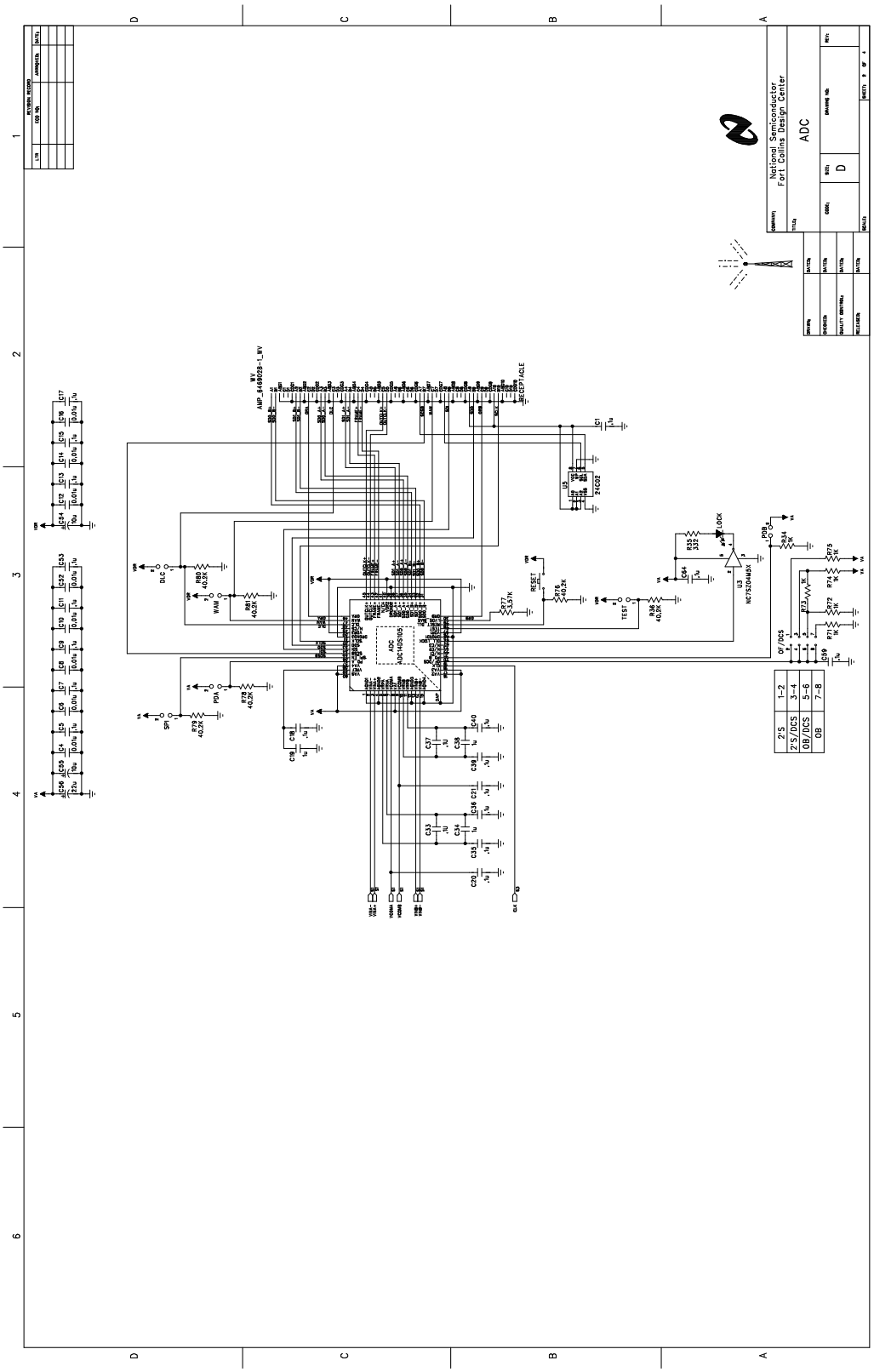

Figure 17. ADC14DS105 Circuit

6.0 Schematic (cont.)

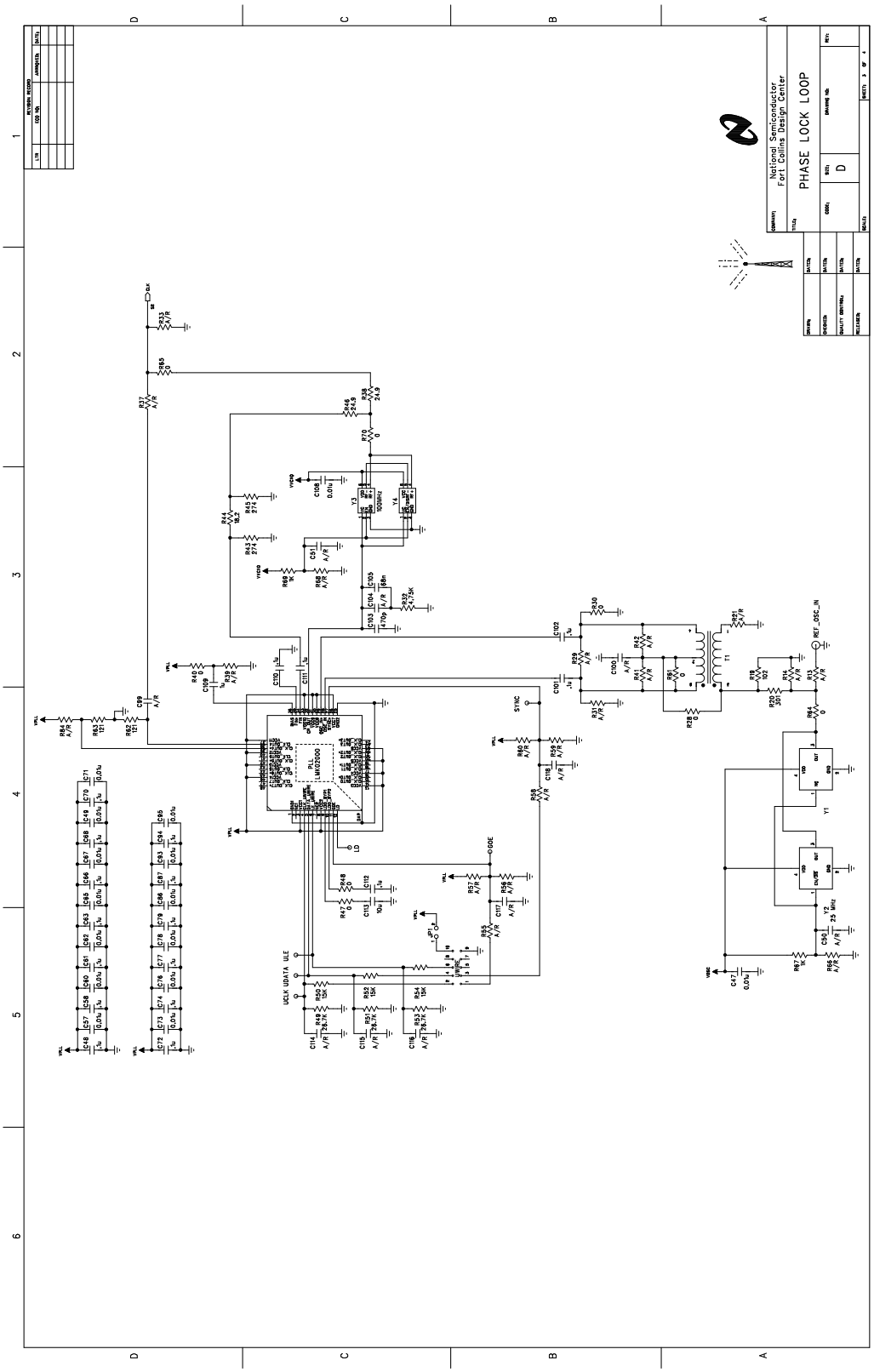

Figure 18. LMK02000 Clock Circuit

6.0 Schematic (cont.)

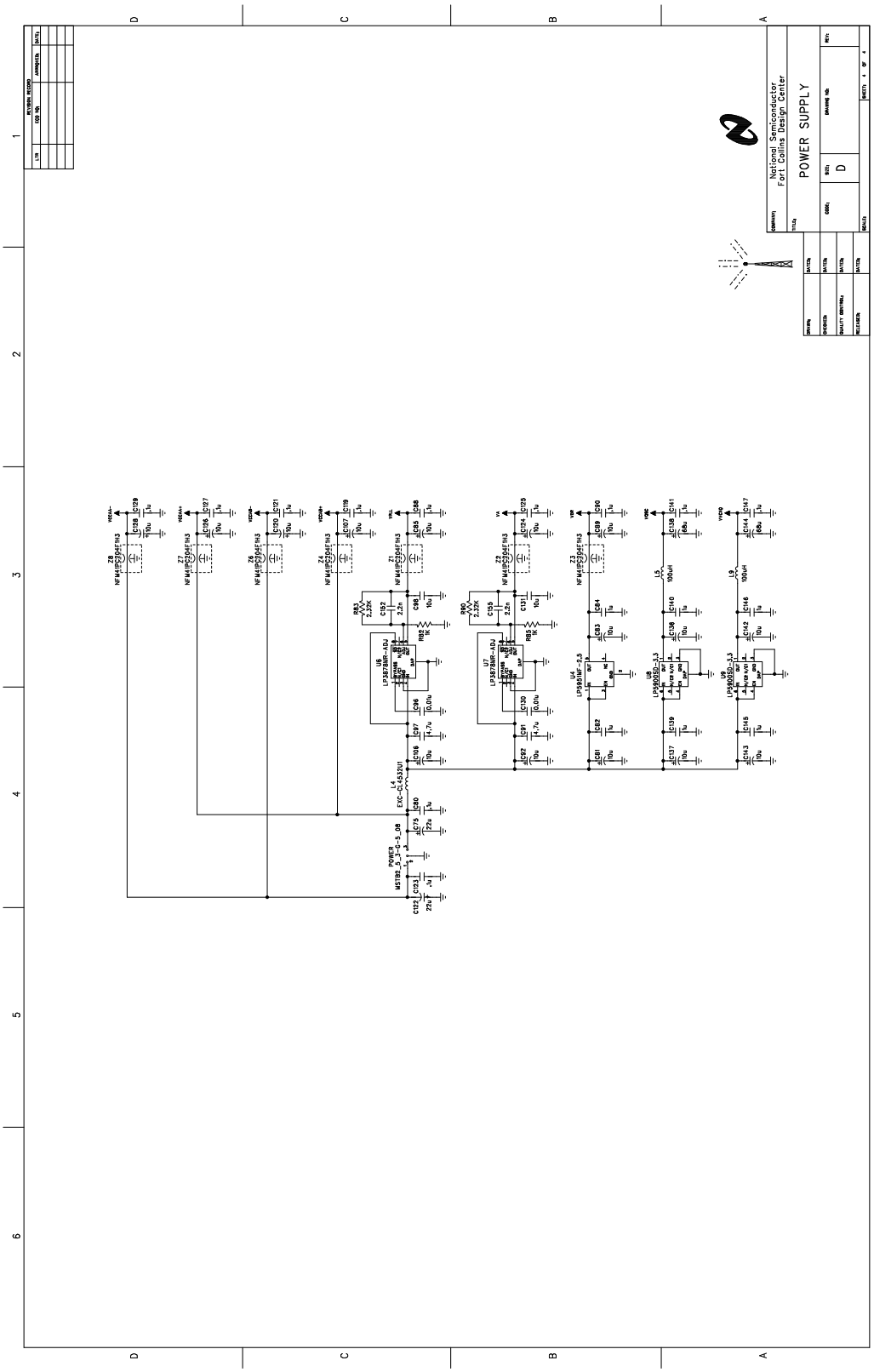

Figure 19. Power Distribution

7.0 Evaluation Board Layout

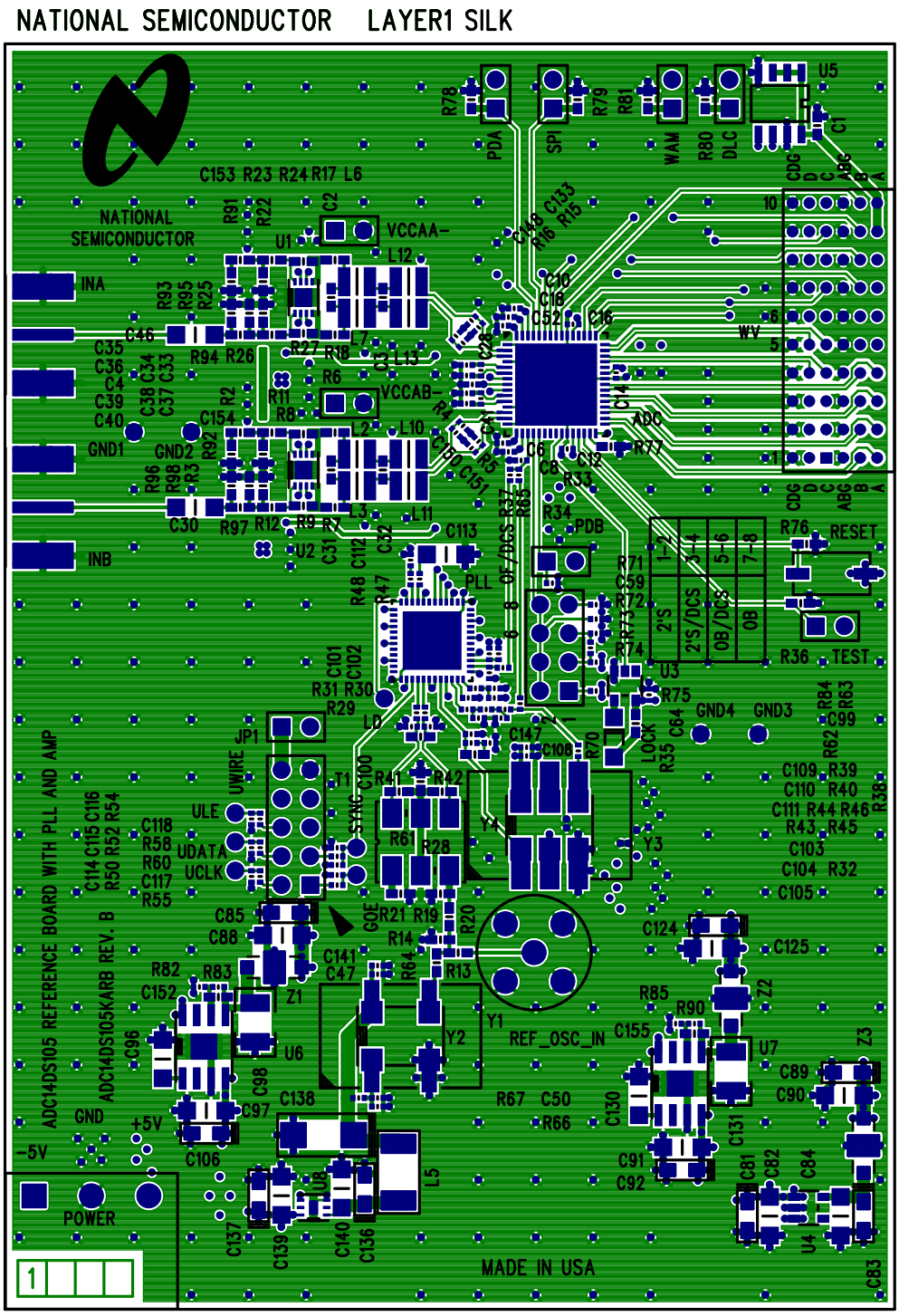

Figure 20. Layer 1 - Signal

7.0 Evaluation Board Layout (cont.)

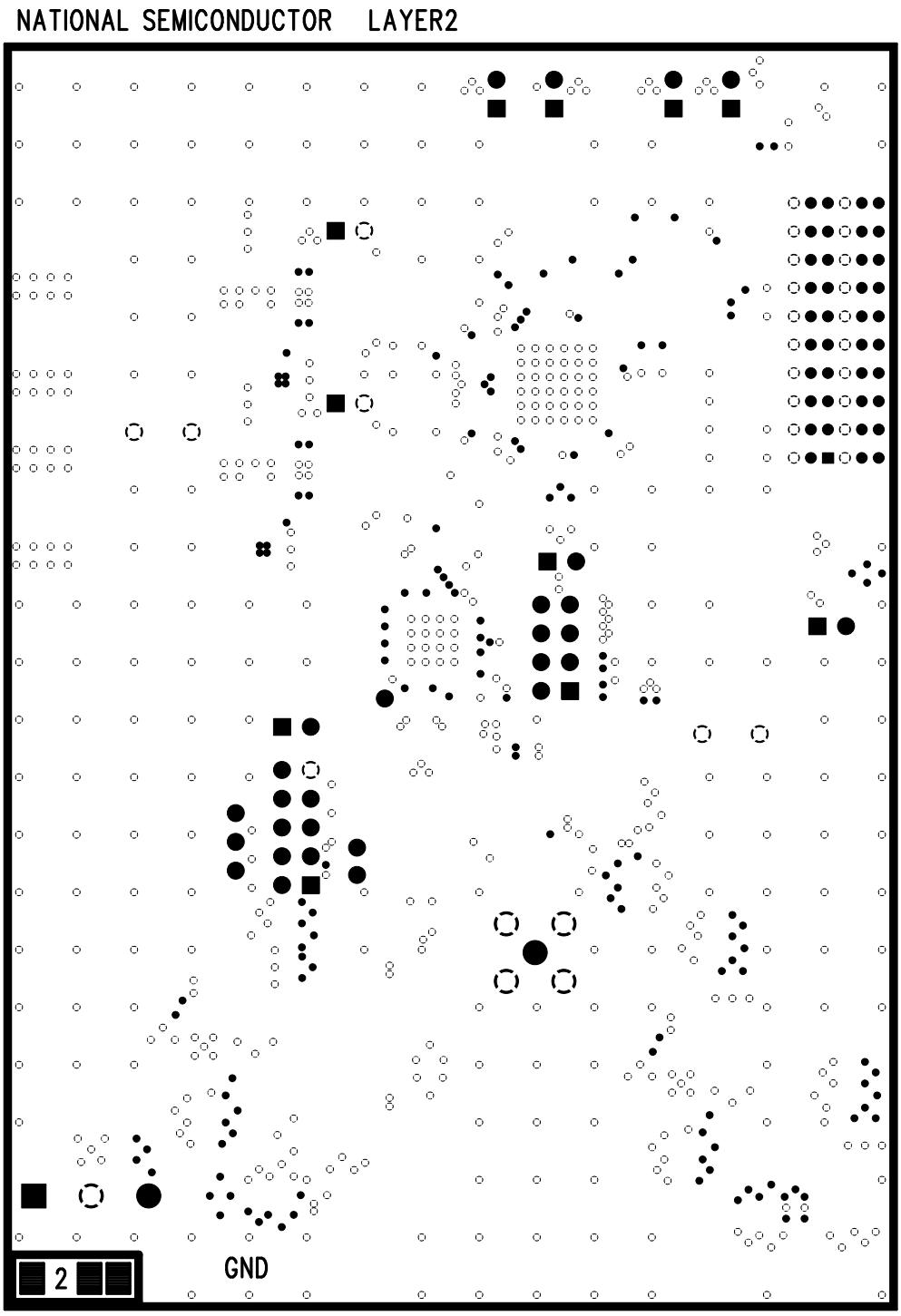

Figure 21. Layer 2 - Ground

7.0 Evaluation Board Layout (cont.)

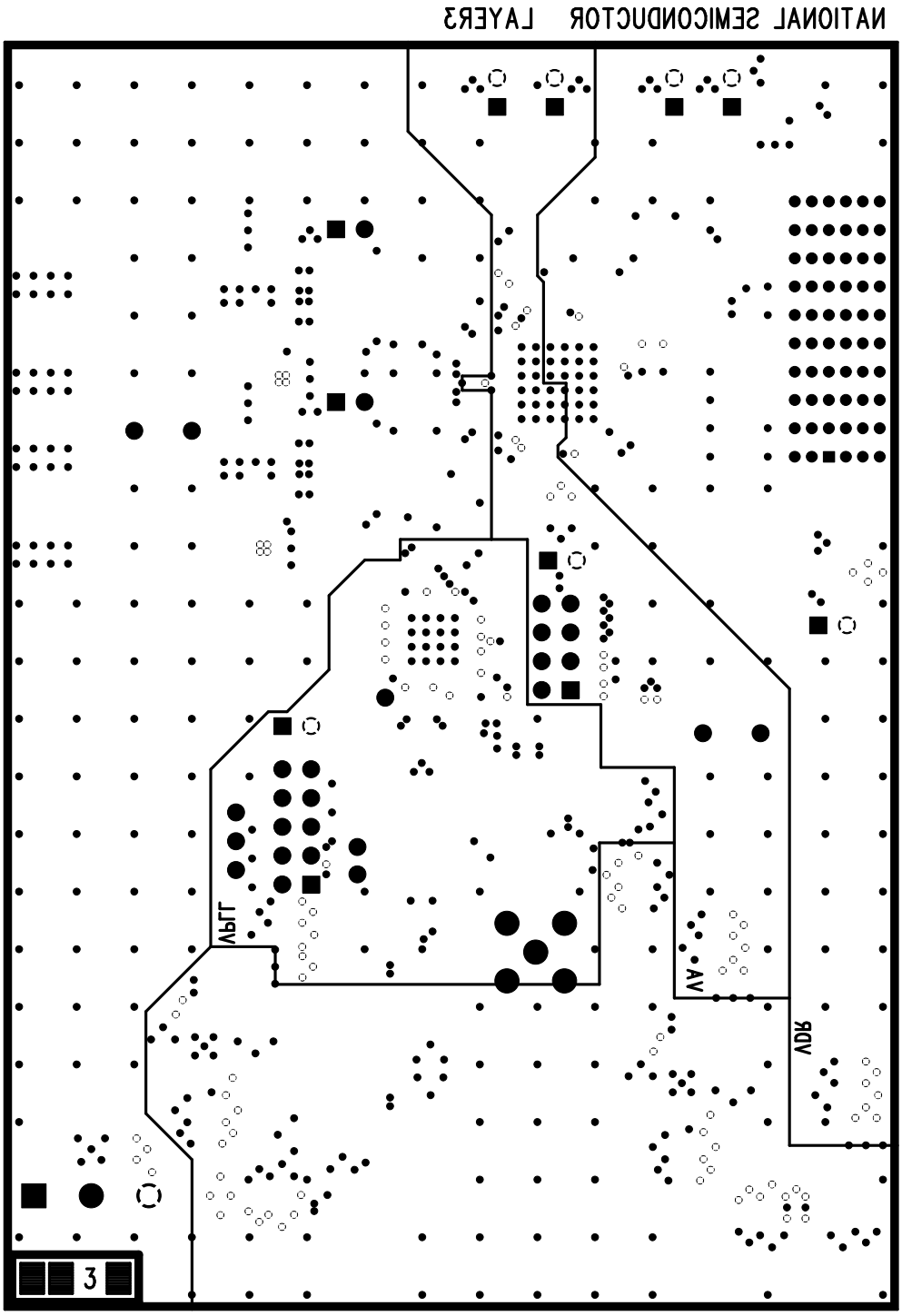

Figure 22. Layer 3 - Power

7.0 Evaluation Board Layout (cont.)

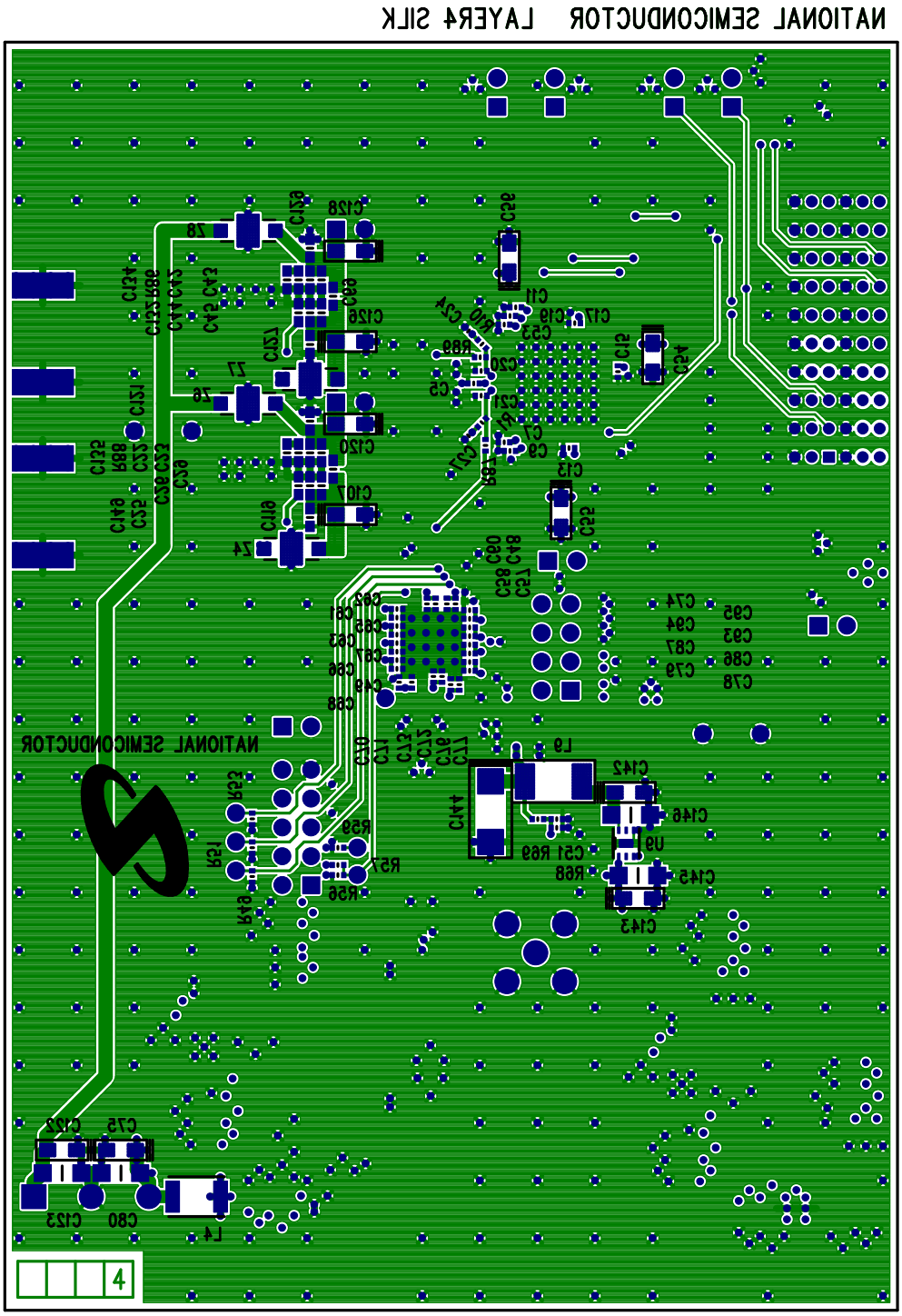

Figure 23. Layer 6 - Signal

8.0 Evaluation Board Bill of Materials

Item	Quantity	Schematic Reference	Part Name	Description	PCB Footprint	Manufacturer
1	1	U5	EEPROM	2K SERIAL EEPROM	8 PIN SOIC	ATMEL
2	1	ADC	CONVERTER	DUAL 14-BIT 105 MSPS A/D CONVERTER WITH SERIAL LVDS OUTPUTS	LLP-60	NATIONAL SEMICONDUCTOR
3	1	WV	WAVEVISION CONNECTOR	HMDz RECEPTACLE	-	TYCO
4	2	C33, C37	0.1uF	0.1uF SMD CAP CERAMIC 6.3V X5R 10%	sm/c_0201	Panasonic - ECG
5	2	C153-154	49.9 ohms	49.9 OHM SMD RESISTOR 1/16W 0.1%	sm/c_0603	Susumu
6	2	C98, C131	10uF	CAP CER 10UF 10V X7R	sm/c_1210	Taiyo Yuden
7	5	C1, C119, C121, C127, C129	0.1uF	0.1uF SMD CAP CERAMIC 25V X5R 10%	sm/c_0603	AVX Corporation
8	37	C5, C7, C9, C11, C13, C15, C17-18, C20-21, C35-36, C39-40, C48, C53, C58-59, C61, C63-64, C66, C68, C70, C72, C74, C77, C79, C87, C94, C101-102, C110-112, C141, C147	0.1uF	0.1uF SMD CAP CERAMIC 10V X5R 10%	sm/c_0402	Panasonic - ECG
9	23	C4, C6, C8, C10, C12, C14, C16, C47, C49, C52, C57, C60, C62, C65, C67, C71, C73, C76, C78, C86, C93, C95, C108	0.01uF	0.01uF SMD CAP CERAMIC 16V X7R 10%	sm/c_0402	AVX Corporation
10	10	C23, C26, C29,C43, C45, C69, C132, C134-135, C149	0.01uF	0.01uF SMD CAP CERAMIC 50V X7R 10%	sm/c_0603	Panasonic - ECG
11	2	C96, C130	0.01uF	0.01uF SMD CAP CERAMIC 50V X7R 5%	sm/c_1206	Kemet
12	2	C30, C46	0 ohms	0 OHM SMD RESISTOR 1/4W 5%	sm/c_1206	Vishay Dale
13	1	C113	10uF	10uF SMD CAP CERAMIC 10V X5R 20%	sm/c_1206	Panasonic - ECG
14	4	C22, C25, C42, C44	1nF	1000PF SMD CAP CERAMIC 50V NPO 5%	sm/c_0603	Panasonic - ECG
15	4	C19, C34, C38, C109	1uF	1uF SMD CAP CERAMIC 6.3V X5R 10%	sm/c_0402	Panasonic - ECG
16	6	C84, C82, C139-140, C145-146	1uF	1uF SMD CAP CERAMIC 25V X7R 10%	sm/c_1206	Panasonic - ECG
17	2	C152, C155	2.2nF	2200pF SMD CAP CERAMIC 100V X7R 5%	sm/c_0603	AVX Corporation
18	2	C3, C32	22pF	22pF SMD CAP CERAMIC 50V NPO 5%	sm/c_0603	Panasonic - ECG
19	2	C91, C97	4.7uF	4.7uF SMD CAP CERAMIC 25V X5R 10%	sm/c_1206	Panasonic - ECG
20	1	C103	470pF	470pF SMD CAP CERAMIC 50V COG 5%	sm/c_0402	TDK Corporation
21	0	-	-	-	-	-
22	1	C105	68nF	68000pF SMD CAP CERAMIC 25V X7R 10%	sm/c_0603	Murata Electronics
23	17	C54-55, C81, C83, C85, C89, C92, C106-107, C120, C124, C126, C128, C136-137, C142-143	10uF	10uF SMD CAP TANTALUM 6.3V 20%	sm/c_3216	Kemet
24	3	C56, C75, C122	22uF	22uF SMD CAP TANTALUM 10V 10%	sm/c_3216	AVX Corporation
25	2	C138, C144	68uF	68uF SMD CAP TANTALUM 10V 20%	sm/c_6032	Kemet
26	1	RESET	RESET SWITCH	LIGHT TOUCH SWITCH 240GF SMD	-	Panasonic - ECG
27	1	L4	Ferrite Bead Core	SMD FERRITE BEAD CORE 4.5X3.2X1.8	-	Panasonic - ECG
28	1	LOCK	LOCK LED	RED LIGHT EMITTING DIODE	-	AVAGO
29	2	L5, L9	Inductor	100UH SMD INDUCTOR UNSHIELDED	sm/i_1812	API Delevan
30	4	L2-3, L6-7	620nH	620nH Series 1008CS (2520) Ceramic Chip Inductor	sm/l_1008	Coilcraft
31	4	L10-13	0 ohms	0 OHM SMD RESISTOR 1/8W 5%	sm/l_1008	ROHM
32	2	JP1, SPI	Jumper 1X2	1X2 JUMPER BLOCK HEADER	-	Samtec
33	3	JP1, SPI, OF/DCS	Shunt	PLACE SHUNT SO IT IS ON ONE OF JP1 CONNECTOR PINS BUT DOES NOT CONNECTOR TO THE OTHER PIN, PLACE SHUNT FROM PINS 1-2 ON SPI, PLACE SHUNT FROM PINS 7-8 ON OF/DCS	-	FCI Electronic
34	1	OF/DCS	Jumper 2X4	2X4 JUMPER BLOCK HEADER	-	Samtec
35	1	UWIRE	Jumper 2X5	2X5 JUMPER BLOCK HEADER	-	Samtec
36	2	U1-2	DIFF AMP	1 GHz Fully Differential Amplifier	LLP-8	NATIONAL SEMICONDUCTOR
37	1	PLL	Phase Lock Loop	PRECISION CLOCK DISTRIBUTOR WITH INTERGRATED PLL	LLP-48	NATIONAL SEMICONDUCTOR
38	2	U6-7	Voltage Regulator	ADJUSTABLE VOLTAGE REGULATOR	PSOP-8	NATIONAL SEMICONDUCTOR
39	2	U8-9	Voltage Regulator	LINEAR REGULATOR FOR RF/ANALOG CIRCUITS	LLP-6	NATIONAL SEMICONDUCTOR
40	1	U4	Voltage Regulator	LOW-DROPOUT CMOS VOLTAGE REGULATOR	SOT23-5	NATIONAL SEMICONDUCTOR
41	1	POWER	Power Connector Terminal Block	TERMINAL BLOCK 3POS 5.08mm	-	Phoenix Contact
42	1	-	Power Connector Plug	TERMINAL BLOCK PLUG 2POS 5.08mm	-	Phoenix Contact
43	1	U3	Inverter	INVERTER SGL TINYLOGIC	SOT23-5	FAIRCHILD
44	7	Z1-4, Z6-8	Noise Suppression Filter	FILTER LC HIGH FREQ .2UF	1806	Murata Electronics
45	5	R28, R61, R64, R94, R97	0 ohms	0 OHM SMD RESISTOR 1/10W 5%	sm/l_0603	Vishay Dale
46	6	R30, R40, R65, R70, R47-48	0 ohms	0 OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Vishay Dale
47	1	R19	102 ohms	102 OHM SMD RESISTOR 1/10W 1%	sm/r_0603	Vishay Dale
48	2	R62-63	121 ohms	121 OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Panasonic - ECG
49	3	R50, R52, R54	15K ohms	15K OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Vishay Dale
50	1	R44	18.2 ohms	18.2 OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Vishay Dale
51	10	R34, R67, R69, R71-75, R82, R85	1K ohms	1K OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Vishay Dale
52	2	R83, R90	2.32K ohms	2.32K OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Vishay Dale
53	2	R38, R46	24.9 ohms	24.9 OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Vishay Dale
54	3	R49, R51, R53	26.7K ohms	26.7K OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Vishay Dale
55	2	R43 R45	274 ohms	274 OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Vishay Dale
56	1	R77	3.57K ohms	3.57K OHM SMD RESISTOR 1/10W 1%	sm/r_0603	Vishay Dale
57	1	R20	301 ohms	301 OHM SMD RESISTOR 1/10W 1%	sm/r_0603	Vishay Dale
58	1	R35	332 ohms	332 OHM SMD RESISTOR 1/10W 1%	sm/r_0603	Vishay Dale
59	1	R32	4.75K ohms	4.75K OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Vishay Dale
60	6	R36, R76, R78-81	40.2K ohms	40.2K OHM SMD RESISTOR 1/10W 1%	sm/r_0603	Vishay Dale
61	4	R8-9, R24, R27	274 ohms	274 OHM SMD RESISTOR 1/10W 1%	sm/r_0603	ROHM
62	4	R6-7, R17-18,	100 ohms	100 OHM SMD RESISTOR 1/16W 0.1%	sm/r_0603	Panasonic - ECG
63	2	R87, R89	49.9 ohms	49.9 OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Yageo Corporation
64	2	INA, INB	SMA Input	PCB MOUNTABLE SMA CONNECTOR	-	Molex/Waldom Electronics Corp
65	1	Y2	OSC	25 MHz Oscillator	-	Connor-Winfield
66	1	Y3	VCXO	100 MHz Voltage Controlled Oscillator	-	Crystek Crystal Corpotation
67	4	MT1-4	Bump-on Rubber Feet	PLACE BUMP ONS AT THE 4 CORNERS, ON BOTTOM OF BOARD	-	3M
68	2	R91-92	0.1uF	0.1uF SMD CAP CERAMIC 25V X5R 10%	sm/r_0603	AVX Corporation
69	0	-	-	-	-	-
70	4	R11-R12, R23, R26	127 ohms	127 OHM SMD RESISTOR 1/10W 1%	sm/r_0603	ROHM
71	4	R2-3, R22, R25	68.1 ohms	68.1 OHM SMD RESISTOR 1/10W 1%	sm/r_0603	Vishay Dale

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