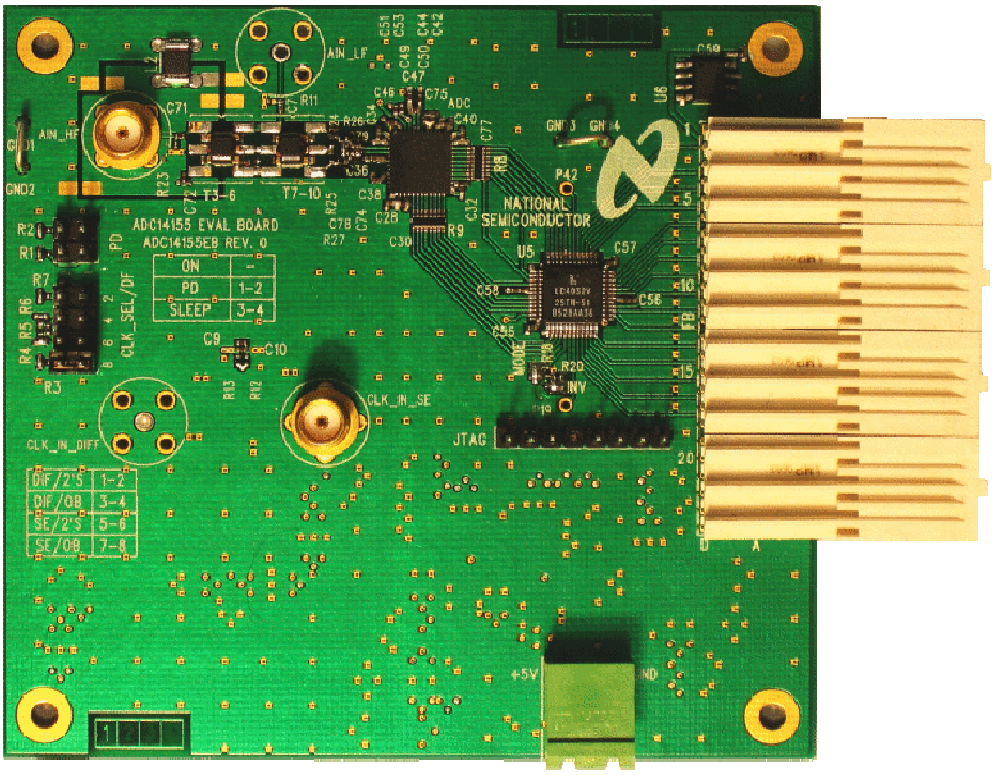
Evaluation Board User's Guide for
ADC14155: 14-Bit, 155 MSPS Analog to Digital Converter



National Semiconductor

www.national.com
Rev 0.0
September 2007

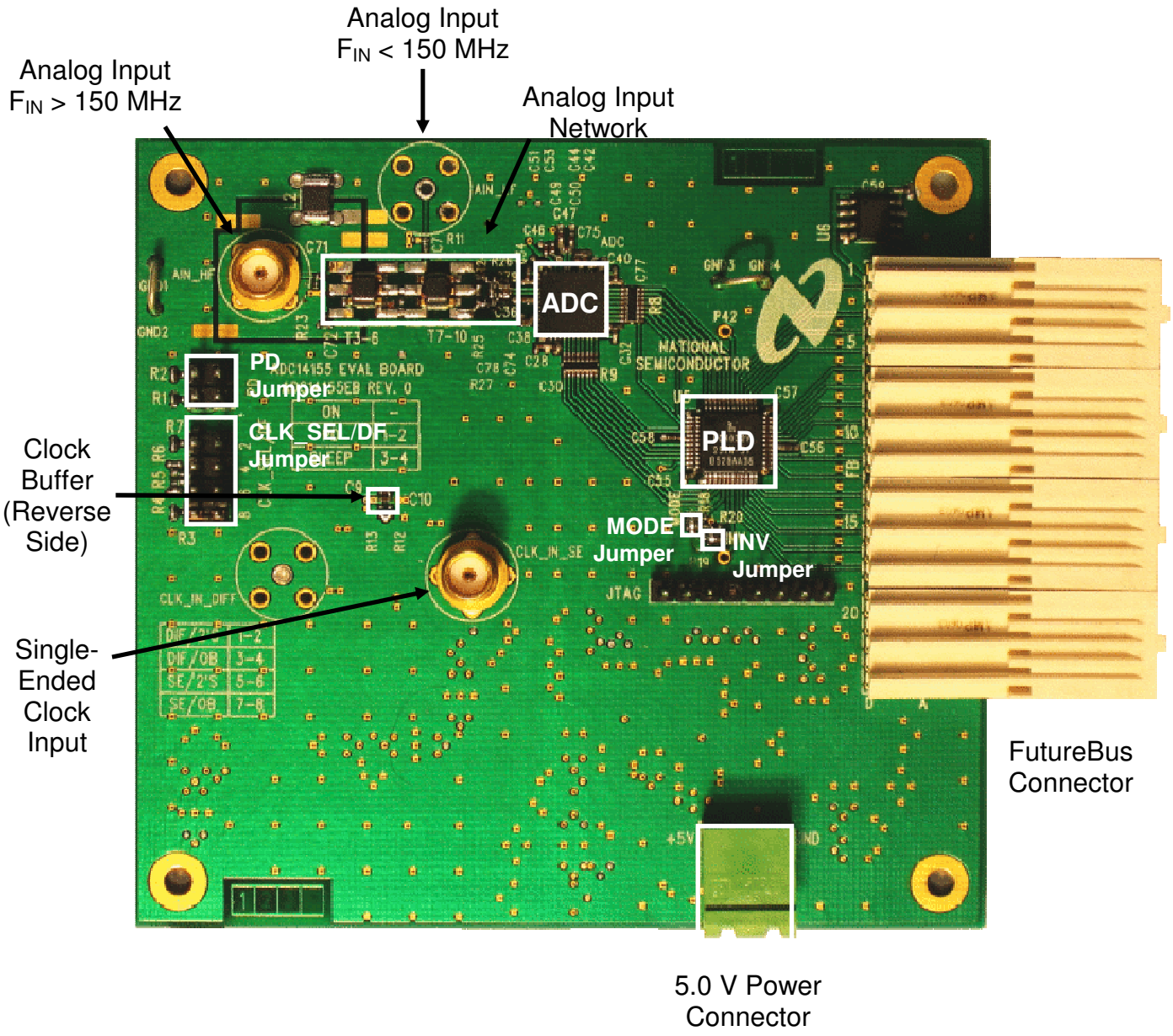


Figure 1. ADC14155 Evaluation Board Connector and Jumper Locations

1.0 Introduction

The ADC14155 Evaluation Board is designed to support the ADC14155 14-bit 155 Mega Sample Per Second (MSPS) Analog to Digital Converter.

The ADC14155 Evaluation Board comes in two versions:

1. **ADC14155HFEB** (high frequency version) for input frequencies greater than 150 MHz.

2. **ADC14155LFEB** (low frequency version) for input frequencies less than 150 MHz.

The digital data from the ADC14155 evaluation board can be captured with a suitable instrument, such as a logic analyzer, or with National Semiconductor's WaveVision data acquisition hardware and software platform. The ADC14155 evaluation board can be connected to the data acquisition hardware through the FutureBus connector (schematic reference designator FB).

The ADC14155 evaluation board is compatible with National Semiconductor's WaveVision 4.4 and higher Digital Interface Board and associated WaveVision software. Please note that the ADC14155 evaluation board is not compatible with the WaveVision 4.0 or 4.1 Digital Interface Boards.

The WaveVision hardware and software package allows fast and easy data acquisition and analysis. The WaveVision hardware connects to a host PC via a USB cable and is fully configured and controlled by the latest WaveVision software. The latest WaveVision software is provided with the ADC14155 evaluation kit. The WaveVision data acquisition hardware is available through the National Semiconductor website (http://www.national.com/appinfo/adc/wv4.html).

2.0 Board Assembly

Each evaluation board from the factory is configured for single-ended clock operation and is populated with an analog input network which has been optimized for one of two analog input frequencies ranges:

1. **ADC14155HFEB** (high frequency version) for input frequencies greater than 150 MHz.

2. **ADC14155LFEB** (low frequency version) for input frequencies less than 150 MHz.

Please refer to the input circuit configurations described in the Analog Input Section (4.2) of this guide.

The location and description of the components on the ADC14155 evaluation board can be found in Figure 1 as well as Section 5.0 (Schematic) and Section 7.0 (Bill of Materials) of this user's guide.

3.0 Quick Start

The ADC14155 evaluation board enables easy set up for evaluating the performance of the ADC14155.

If the WaveVision data acquisition and data analysis system is to be used for capturing data, please follow the Quick Start Guide in the WaveVision User's Guide to install the required software and to connect the WaveVision Digital Interface Board to the PC. Please note that the ADC14155 evaluation board is only compatible with National Semiconductor's WaveVision 4.4 and higher Digital Interface boards.

3.1 Evaluation Board Jumper Positions

The ADC14155 evaluation board jumpers should be configured as follows. Please refer to Figure 1 for the exact jumper locations.

1. J1 on the reverse of the board should be shorted.
2. The MODE jumper on the front of the board should be shorted and the INV jumper should be left open. See Section 4.4 for more detailed information regarding the function of the MODE and INV jumpers.
3. The PD jumper places the ADC14155 into either power-down or sleep mode. Table 1 below shows how to select between the power-down modes.

PD Jumper Setting	Mode
Open	Normal Operation
1-2	Power-down
3-4	Sleep

Table 1. PD/Sleep Selection Table

4. CLK_SEL/DF pin jumpers select the output data format (2's complement or offset binary) and clock mode (single-ended or differential). Table 2 below shows how to select between the clock modes and output data formats. Please note that the ADC14155 evaluation board is delivered with the ADC14155 clock input configured for single-ended operation and Offset Binary output data format (Jumper 7-8).

CLK_SEL/DF Jumper Setting	Clock Mode	Output Data Format
1-2	Differential	2's Complement
3-4	Differential	Offset Binary
5-6	Single-Ended	2's Complement
7-8*	Single-Ended	Offset Binary

* As assembled from factory.

Table 2. CLK_SEL/DF Selection Table

3.2 Connecting Power and Signal Sources

1. To power the ADC14155 evaluation board, connect a 5.0V power supply capable of supplying up to 500mA to the green power connector labeled "+5V" which is located along the bottom edge of the ADC14155 evaluation board.
2. Use the FutureBus connector (FB) to connect the ADC14155 evaluation board to the instrument being used to capture the data from the evaluation board. If the WaveVision Digital Interface Board is being used for data capture, please consult the WaveVision User's Guide for details on installing and operating the WaveVision hardware and software system.
3. Connect the clock and signal inputs to the SMA connectors labeled CLK_IN_SE (for clock) and AIN_LF (for the ADC14155LFEB) or AIN_HF (for the ADC14155HFEB).

4.0 Functional Description

4.1 Clock Input

The clock used to sample the analog input should be applied to the CLK_IN_SE SMA connector (if using the single-ended clock mode as provided from the factory).

To achieve the best noise performance (best SNR), a low jitter clock source with total additive jitter less than 150 fs should be used. A low jitter crystal oscillator is recommended, but a sinusoidal signal generator with low phase noise, such as the SMA100A from Rohde & Schwarz or the HP8644B (discontinued) from Agilent / HP, can also be used with a slight degradation in the noise performance. The SNR is primarily degraded by the broadband noise of the signal generator. The clock signal generator amplitude is typically set to +19.9 dBm to produce the highest possible slew rate, but the SNR performance will be impacted minimally by slightly lowering the signal generator amplitude. Placing a bandpass filter between the clock source and the CLK_IN_SE SMA connector will further improve the noise performance of the ADC by filtering out the broadband noise of the clock source. All results in the ADC14155 datasheet are obtained with a tunable bandpass filter made by Trilithic, Inc. (Indianapolis, IN) in the clock signal path.

The noise performance of the ADC14155 can be improved further by making the edge transitions of the clock signal entering the ADC clock input (pin 11, CLK+) very sharp. The ADC14155 evaluation board is assembled with a high speed buffer gate (NC7WV125K8X, schematic reference designator U2) in the clock input path to provide a sharp clock edge to the clock inputs and improve the noise performance of the ADC. The amplitude of the clock signal from the NC7WV125K8X high speed buffer is 3.3V.

4.2 Analog Input

To obtain the best distortion results (best SFDR), the analog input network on the evaluation board must be optimized for the signal frequency being applied.

For analog input frequencies up to 150 MHz, the circuit in Figure 2 is recommended. This is the configuration of the assembled ADC14155LFEB as it is delivered from the factory. For input frequencies above 150 MHz, the circuit in Figure 3 is recommended. This is the configuration of the assembled ADC14155HFEB as it is delivered from the factory.

A low noise signal generator such as the SMA100A from Rohde & Schwarz or the HP8644B (discontinued) from Agilent / HP is recommended to drive the signal input of the ADC14155 evaluation board. The output of the signal generator must be filtered to suppress the harmonic distortion produced by the signal generator and to allow accurate measurement of the ADC14155 distortion performance. A low pass or a bandpass filter is recommended to filter the analog input signal. In some cases, a second low pass filter may be necessary. The bandpass filter on the analog input will further improve the noise performance of the ADC by filtering the broadband noise of the signal generator. Data shown in the ADC14155 datasheet was taken with a tunable bandpass filter made by Trilithic (Indianapolis, IN) in the analog signal path.

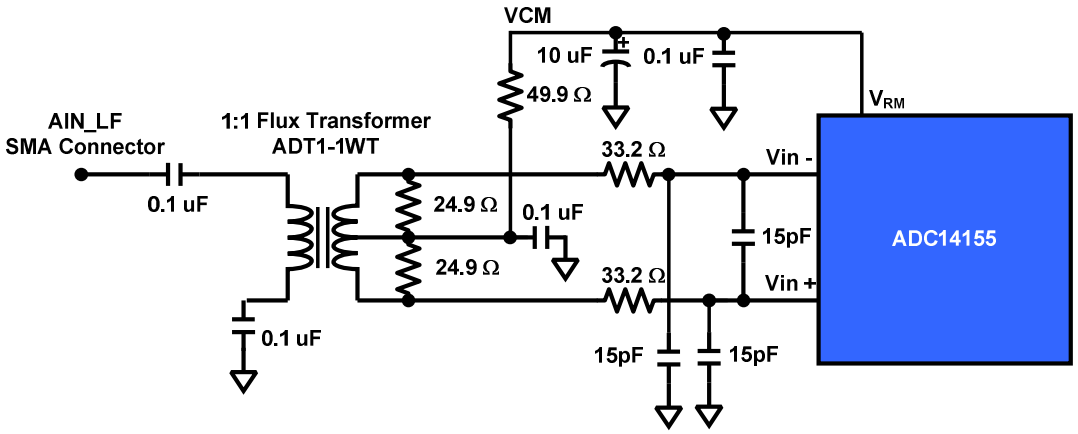


Figure 2. Analog Input Network of ADC14155LFEB: F_{IN} < 150 MHz

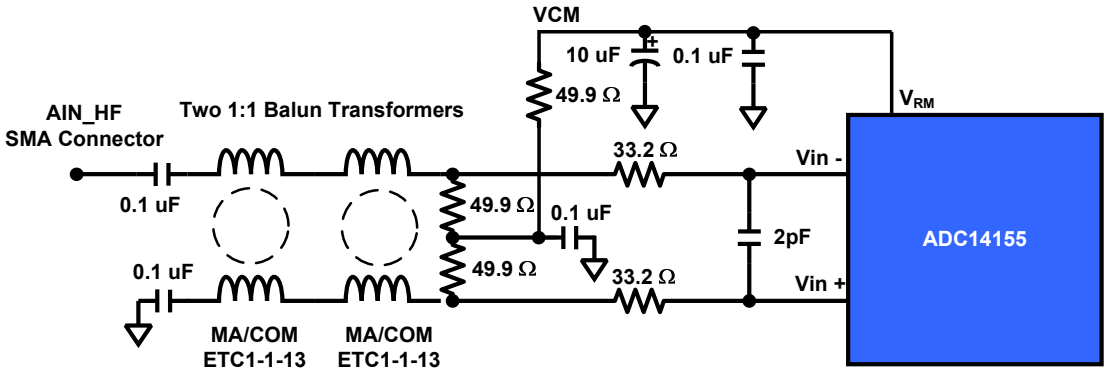


Figure 3. Analog Input Network of ADC14155HFEB: F_{IN} > 150 MHz

4.3 ADC Reference and Input Common Mode

The internal 1.0V reference on the ADC14155 is used to acquire all of the results in the ADC14155 datasheet. It is recommended to use the internal reference on the ADC14155. However, if an external reference is required, the ADC14155 is capable of accepting an external reference voltage between 0.9V and 1.1V (1.0V recommended). The input impedance of the ADC14155 V_{REF} pin (pin 46) is 9 kΩ. Therefore, to overdrive this pin, the output impedance of the exernal reference source should be << 9 kΩ.

It is recommended to use the voltage at the V_{RM} pin (pin 45) of the ADC14155 to provide the 1.5V common mode voltage required for the differential analog inputs V_{IN+} and V_{IN-}. The ADC14155 evaluation board is factory-assembled with V_{RM} connected to the transformer center-tap through a 49.9Ω resistor to provide the necessary common mode voltage to the differential analog input.

4.4 Board Outputs

The digitized 14-bit output word from the ADC14155 evaluation board is available at pins B4 (MSB) through B17 (LSB) on the FutureBus connector (schematic reference designator FB). The rising edge of the data ready (DRDY) signal should be used to capture the output data. The DRDY signal is available at pin D2 of the FutureBus connector and the over-range (OVR) bit which indicates that the input signal to the ADC has exceeded the maximum digitizable signal amplitude is available at pin B18 on the FutureBus connector. See the Evaluation Board schematic in Section 5.0 for details.

The ADC14155 evaluation board uses a PLD device from Lattice Semiconductor (LC4032V-25TN48C, schematic reference designator U5) to translate the ADC output from 1.8V CMOS to 3.3V CMOS, which is compatible with the WaveVision Digital Interface Board and other data capture instruments which the user may choose.

The ADC14155 evaluation board has been designed to give the user the flexibility to choose between passing the data from the ADC to the capture instrument either with or without latching the data in the PLD. Tables 3 and 4 show how to configure the PLD device through the MODE and INV jumpers on the evaluation board to enable the latching function. The ADC14155 evaluation board is factory assembled with the MODE jumper shorted and the INV jumper open.

MODE Jumper	**Data Transfer Through PLD**
Short*	Latch data with DRDY signal
Open	Pass data transparently without latching

* As assembled from factory.

Table 3. PLD Data Transfer Selection Table

The data from the ADC14155 in the PLD can be latched either on the rising or falling edge of DRDY. Table 4 shows how to choose which edge of DRDY will be used to latch the ADC data into the PLD.

INV Jumper	**DRDY Latching Edge**
Short	Falling
Open*	Rising

* As assembled from factory.

Table 4. PLD Latch Edge Selection Table

4.5 Power requirements.

Power to the ADC14155 evaluation board is supplied through the green power connector labeled "+5V" which is located along the bottom edge of the board. Voltage and current requirements are:

- +5V capable of delivering up to 500mA (ADC14155 evaluation board only)

5.0 Evaluation Board Schematic

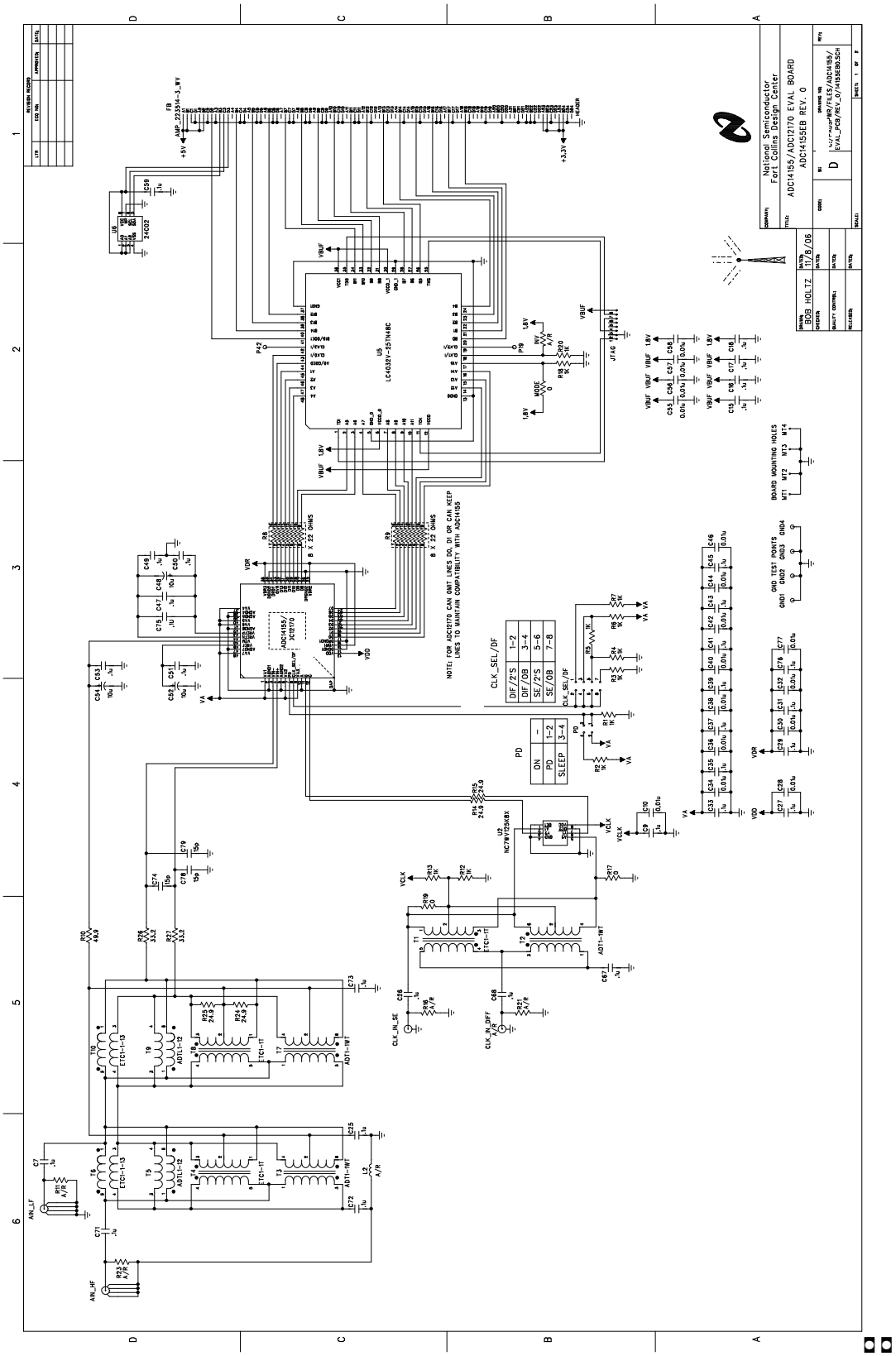


Figure 4. Signals

5.0 Schematic (cont.)

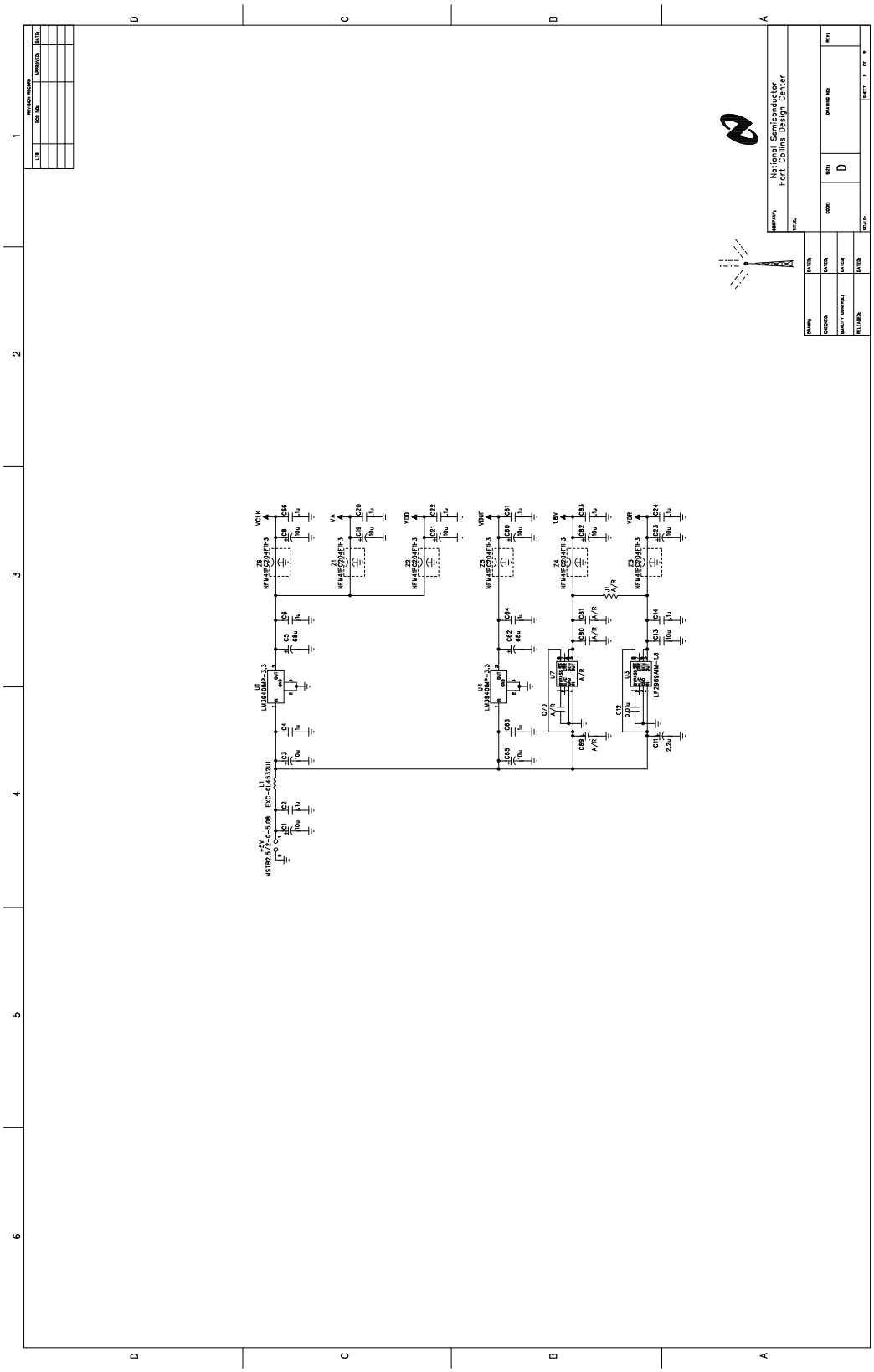


Figure 5. Power Distribution

6.0 Evaluation Board Layout

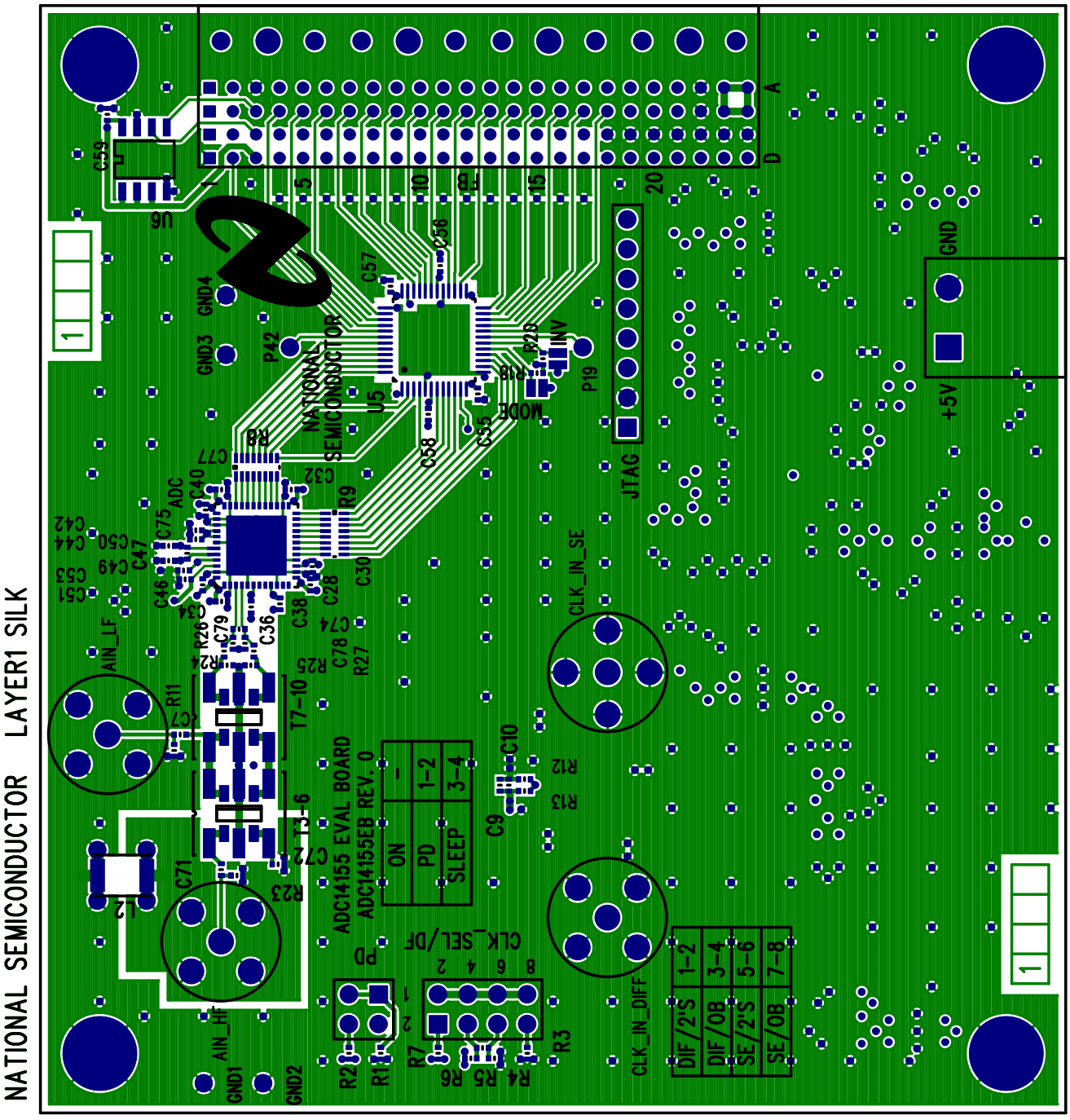


Figure 6. Layer 1 - Signal

6.0 Evaluation Board Layout (cont.)

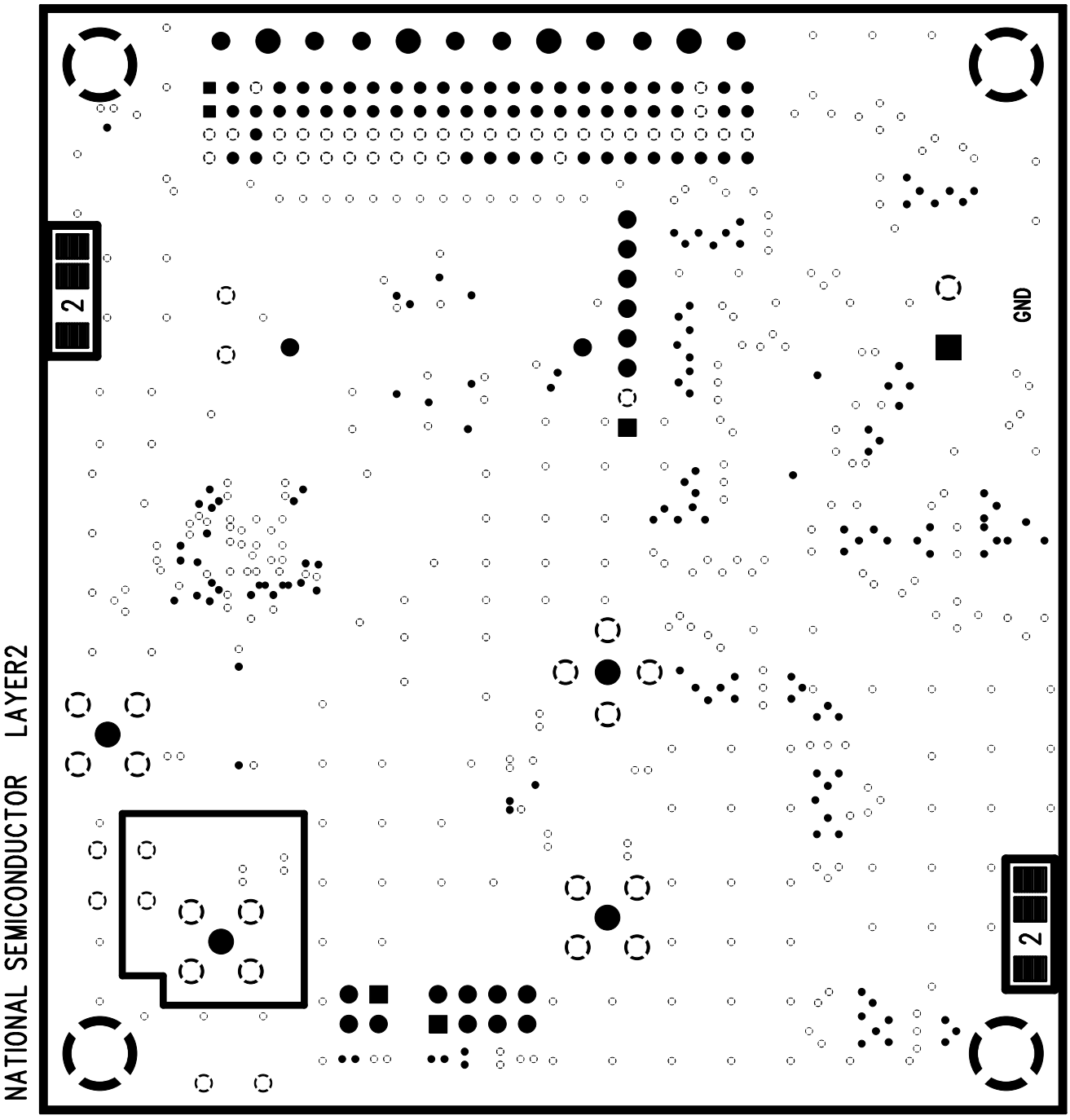


Figure 7. Layer 2 - Ground

6.0 Evaluation Board Layout (cont.)

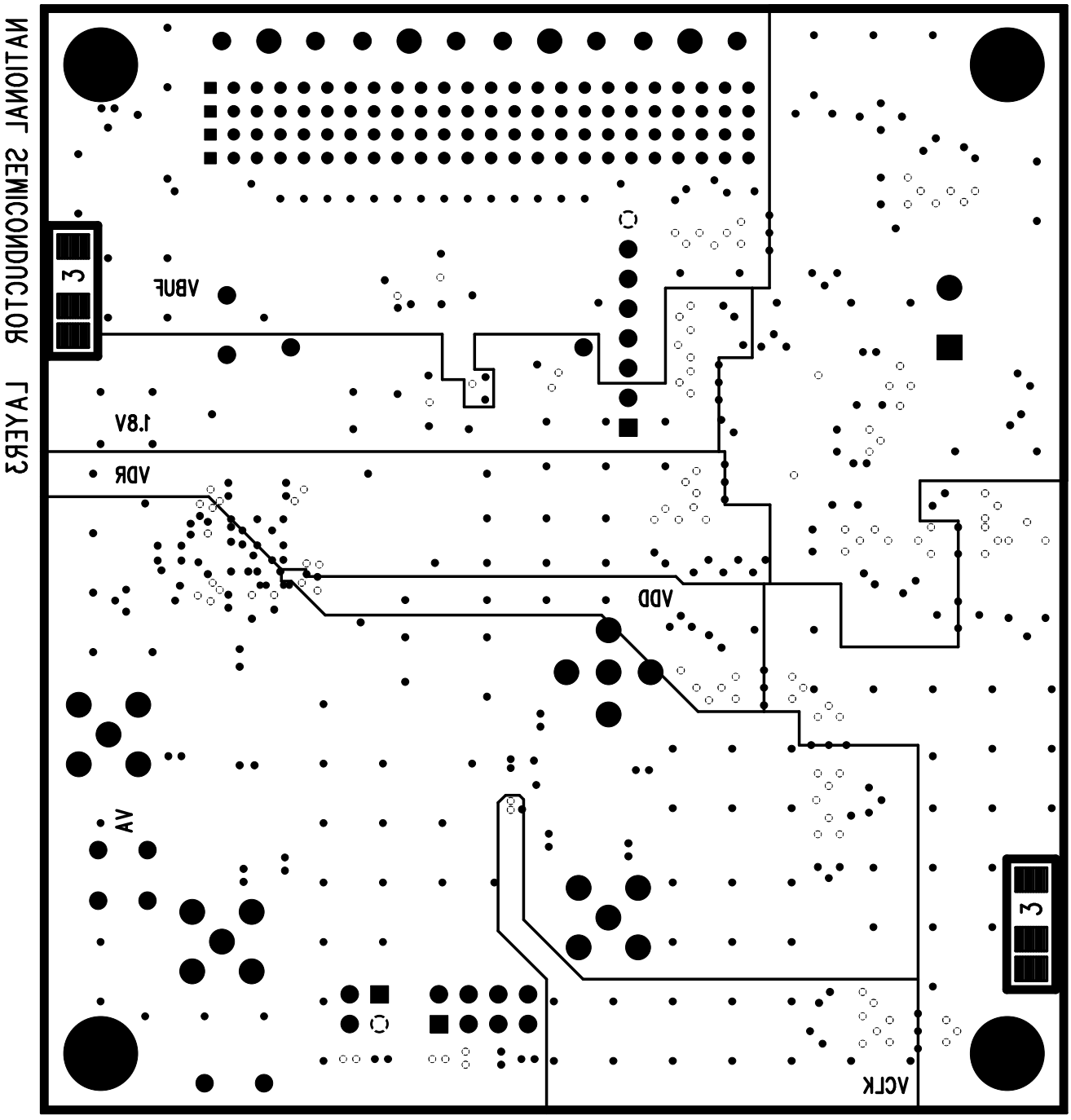


Figure 8. Layer 3 - Power

6.0 Evaluation Board Layout (cont.)

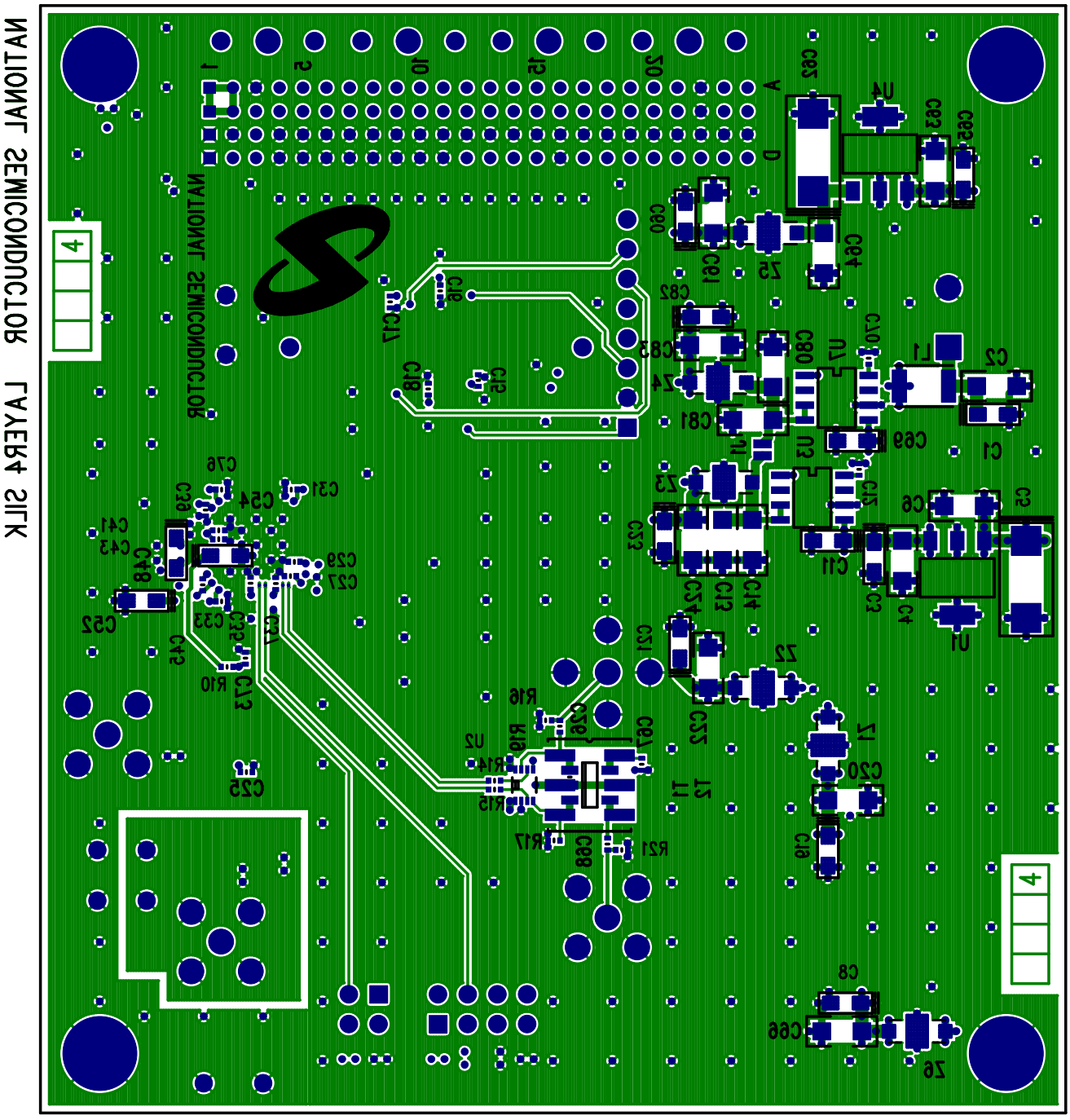


Figure 9. Layer 4 - Signal

7.0 Evaluation Board Bill of Materials

7.1 ADC14155HFEB (For Fin > 150 MHz)

Item	Quantity	Schematic Reference	Part Name	Description	PCB Footprint	Manufacturer
1	1	U6	24C02	2K SERIAL EEPROM 1.8V	SOIC-8	Atmel
2	1	ADC	ADC14155	14-Bit, 155 MSPS Analog/Digital Converter	48-LLP	National Semiconductor
3	2	T6, T10	ETC1-1-13	BALUN TRANSFORMER		MA/COM
4	4	FB	AMP_5223514-1	Z-PACK 2mm FB (Futurebus+) RIGHT ANGLE HEADER CONNECTOR	-	AMP
5	1	C75	0.1uF	0.1uF SMD CAP CERAMIC 6.3V X5R 10%	sm/c_0201	Panasonic - ECG
6	8	C2, C14, C20, C22, C24, C61, C66, C83	0.1uF	0.1uF SMD CAP CERAMIC 25V X7R 10%	sm/c_1206	Panasonic - ECG
7	26	C9, C15-18, C26-27, C29, C31, C33, C35, C37, C39, C41, C43, C45, C47, C49-51, C53, C59, C71, C72, C73, C76	0.1uF	0.1uF SMD CAP CERAMIC 10V X5R 10%	sm/c_0402	Panasonic - ECG
8	17	C10, C12, C28, C30, C32, C34, C36, C38, C40, C42 C44, C46, C55-58, C77	0.01uF	0.01uF SMD CAP CERAMIC 16V X7R 10%	sm/c_0402	AVX Corporation
9	1	C13	10uF	10uF SMD CAP CERAMIC 10V X5R 20%	sm/c_1206	Panasonic - ECG
10	1	C74	2pF	2pF SMD CAP CERAMIC 50v +/-0.25pF	sm/c_0402	Murata Electronics
11	4	C4, C6, C63-64	1uF	1uF SMD CAP CERAMIC 25V X7R 10%	sm/c_1206	Panasonic - ECG
12	12	C1, C3, C8, C19, C21, C23, C48, C52, C54, C60, C65, C82	10uF	10uF SMD CAP TANTALUM 6.3V 20%	sm/c_3216	Kemet
13	1	C11	2.2uF	2.2uF SMD CAP TANTALUM 16V 10%	sm/c_3216	Kemet
14	2	C5, C62	68uF	68uF SMD CAP TANTALUM 6.3V 10%	sm/c_7343	Kemet
15	2	R8-9	8x22 ohm	22 OHM SMD 8 RES ARRAY 5%	sm/r_0402 x 8	Panasonic -ECG
16	2	L1, L2	Ferrite Bead Core	SMD FERRITE BEAD CORE 4.5X3.2X1.8	-	Panasonic -ECG
17	1	JTAG	Jumper 1x8	JUMPER BLOCK USING 8 PIN SIP HEADER	-	Samtec
18	1	PD	Jumper 2X2	2X2 JUMPER BLOCK HEADER CUT TO SIZE FROM 2X6 HEADER	-	Samtec
19	1	CLK_SEL/DF	Jumper 2X4	2X4 JUMPER BLOCK HEADER CUT TO SIZE FROM 2X6 HEADER	-	Samtec
20	1	-	Shunt	PLACE SHUNT ACROSS PINS 7-8 ON CLK_SEL/DF JUMPER	-	FCI Electronic
21	1	U5	PLD	ispMACH PLD, 3.3V core	48-TQFP	Lattice Semiconductor
22	2	U1, U4	3.3V Regulator	1A LOW DROPOUT REGULATOR FOR 5V TO 3.3 V CONVERSION	SOT-223	National Semiconductor
23	1	U3	1.8V Regulator	MICROPOWER/LOW NOISE, 500 mA ULTRA LOW-DROPOUT REGULAT	SOIC NARROW -8	National Semiconductor
24	1	+5V	Power Connector Terminal Block	TERMINAL BLOCK 2POS 5.08mm	-	Phoenix Contact
25	1	-	Power Connector Plug	TERMINAL BLOCK PLUG 2POS 5.08mm	-	Phoenix Contact
26	4	MT1-4	Bump-on Rubber Feet	PLACE BUMP ONS AT THE 4 CORNERS, ON BOTTOM OF BOARD	-	3M
27	1	U2	Tinylogic Buffer	TINYLOGIC ULP-A BUFFER WITH 3-STATE OUTPUT 8-LEAD US8, JEDEC MO-187, CA 3.1 mm WIDE	-	Fairchild Semiconductor
28	6	Z1-6	Noise Suppression Filter	FILTER LC HIGH FREQ .2UF	1806	Murata Electronics
29	2	J1, MODE	Solder Short	SOLDER SHORT ACROSS THE PADS OF "J1" AND ACROSS PADS OF "MODE"	-	-
30	2	R17, R19	0 ohms	0 OHM SMD RESISTOR	sm/r_0402	Vishay Dale
31	11	R1-7, R12-13, R18, R20	1 kOHM	1 kOHM SMD RESISTOR 1/16W 1%	sm/r_0402	Panasonic - ECG
32	2	R14-15	24.9 ohms	24.9 OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Yageo Corporation
33	2	R26-27	33.2 ohms	33.2 OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Vishay Dale
34	3	R10, R24-25	49.9 ohms	49.9 OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Yageo Corporation
35	2	AIN_HF, CLK_IN_SE	SMA Input	PCB MOUNTABLE SMA CONNECTOR	-	Emerson Network Power Connectivity

7.0 Evaluation Board Bill of Materials (cont.)

7.2 ADC14155LFEB (For Fin < 150 MHz)

Item	Quantity	Schematic Reference	Part Name	Description	PCB Footprint	Manufacturer
1	1	U6	24C02	2K SERIAL EEPROM 1.8V	SOIC-8	Atmel
2	1	ADC	ADC14155	14-Bit, 155 MSPS Analog/Digital Converter	48-LLP	National Semiconductor
3	1	T7	ADT1-1WT+	WIDEBAND RF TRANSFORMER 0.4MHz - 800 MHz	CD542	MINI CIRCUITS
4	4	FB	AMP_5223514-1	Z-PACK 2mm FB (Futurebus+) RIGHT ANGLE HEADER CONNECTOR	-	AMP
5	1	C75	0.1uF	0.1uF SMD CAP CERAMIC 6.3V X5R 10%	sm/c_0201	Panasonic - ECG
6	8	C2, C14, C20, C22, C24, C61, C66, C83	0.1uF	0.1uF SMD CAP CERAMIC 25V X7R 10%	sm/c_1206	Panasonic - ECG
7	26	C7, C9, C15-18, C25, C26-27, C29, C31, C33, C35, C37, C39, C41, C43, C45, C47, C49-51, C53, C59, C73, C76	0.1uF	0.1uF SMD CAP CERAMIC 10V X5R 10%	sm/c_0402	Panasonic - ECG
8	17	C10, C12, C28, C30, C32, C34, C36, C38, C40, C42 C44, C46, C55-58, C77	0.01uF	0.01uF SMD CAP CERAMIC 16V X7R 10%	sm/c_0402	AVX Corporation
9	1	C13	10uF	10uF SMD CAP CERAMIC 10V X5R 20%	sm/c_1206	Panasonic - ECG
10	3	C74, C78-79	15pF	15pF SMD CAP CERAMIC 50v NP0 5%	sm/c_0402	Panasonic - ECG
11	4	C4, C6, C63-64	1uF	1uF SMD CAP CERAMIC 25V X7R 10%	sm/c_1206	Panasonic - ECG
12	12	C1, C3, C8, C19, C21, C23, C48, C52, C54, C60, C65, C82	10uF	10uF SMD CAP TANTALUM 6.3V 20%	sm/c_3216	Kemet
13	1	C11	2.2uF	2.2uF SMD CAP TANTALUM 16V 10%	sm/c_3216	Kemet
14	2	C5, C62	68uF	68uF SMD CAP TANTALUM 6.3V 10%	sm/c_7343	Kemet
15	2	R8-9	8x22 ohm	22 OHM SMD 8 RES ARRAY 5%	sm/r_0402 x 8	Panasonic -ECG
16	1	L1	Ferrite Bead Core	SMD FERRITE BEAD CORE 4.5X3.2X1.8	-	Panasonic -ECG
17	1	JTAG	Jumper 1x8	JUMPER BLOCK USING 8 PIN SIP HEADER	-	Samtec
18	1	PD	Jumper 2X2	2X2 JUMPER BLOCK HEADER CUT TO SIZE FROM 2X6 HEADER	-	Samtec
19	1	CLK_SEL/DF	Jumper 2X4	2X4 JUMPER BLOCK HEADER CUT TO SIZE FROM 2X6 HEADER	-	Samtec
20	1	-	Shunt	PLACE SHUNT ACROSS PINS 7-8 ON CLK_SEL/DF JUMPER	-	FCI Electronic
21	1	U5	PLD	ispMACH PLD, 3.3V core	48-TQFP	Lattice Semiconductor
22	2	U1, U4	3.3V Regulator	1A LOW DROPOUT REGULATOR FOR 5V TO 3.3 V CONVERSION	SOT-223	National Semiconductor
23	1	U3	1.8V Regulator	MICROPOWER/LOW NOISE, 500 mA ULTRA LOW-DROPOUT REGULAT	SOIC NARROW -8	National Semiconductor
24	1	+5V	Power Connector Terminal Block	TERMINAL BLOCK 2POS 5.08mm	-	Phoenix Contact
25	1	-	Power Connector Plug	TERMINAL BLOCK PLUG 2POS 5.08mm	-	Phoenix Contact
26	4	MT1-4	Bump-on Rubber Feet	PLACE BUMP ONS AT THE 4 CORNERS, ON BOTTOM OF BOARD	-	3M
27	1	U2	Tinylogic Buffer	TINYLOGIC ULP-A BUFFER WITH 3-STATE OUTPUT 8-LEAD US8, JEDEC MO-187, CA 3.1 mm WIDE	-	Fairchild Semiconductor
28	6	Z1-6	Noise Suppression Filter	FILTER LC HIGH FREQ .2UF	1806	Murata Electronics
29	2	J1, MODE	Solder Short	SOLDER SHORT ACROSS THE PADS OF "J1" AND ACROSS PADS OF "MODE"	-	-
30	2	R17, R19	0 ohms	0 OHM SMD RESISTOR	sm/r_0402	Vishay Dale
31	11	R1-7, R12-13, R18, R20	1 kOHM	1 kOHM SMD RESISTOR 1/16W 1%	sm/r_0402	Panasonic - ECG
32	4	R14-15, R24-25	24.9 ohms	24.9 OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Yageo Corporation
33	2	R26-27	33.2 ohms	33.2 OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Vishay Dale
34	1	R10	49.9 ohms	49.9 OHM SMD RESISTOR 1/16W 1%	sm/r_0402	Yageo Corporation
35	2	AIN_LF, CLK_IN_SE	SMA Input	PCB MOUNTABLE SMA CONNECTOR	-	Emerson Network Power Connectivity

The ADC14155 Evaluation Board is intended for product evaluation purposes only and is not intended for resale to end consumers, is not authorized for such use and is not designed for compliance with European EMC Directive 89/336/EEC.

WaveVision is a trademark of National Semiconductor Corporation. National does not assume any responsibility for use of any circuitry or software supplied or described. No circuit patent licenses are implied.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80 532 78 32

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507