Errata: CS5571 - Silicon revision: B0

Reference CS5571 Data Sheet revision DS768PP1 dated March 2008.

Pin 12 (DITHER) Logic Level vs. Pin 13 ($\overline{\text{RST}}$) Logic Level

Description

The $\overline{\text{RST}}$ pin does not initialize the device correctly if pin 12 (DITHER) is held low as pin 13 ($\overline{\text{RST}}$) is driven high.

Workaround

Pin 12 (DITHER) should be driven high (to VL) until after $\overline{\text{RST}}$ is driven high.

The pin can then be used as described in the data sheet for the dither function.

Determining the Silicon Revision of the Integrated Circuit

On the front of the integrated circuit, directly under the part number, is an alpha-numeric line. Characters 5 and 6 in this line represent the silicon revision of the chip. For example, this line indicates that the chip is a “B0” revision chip:

FF AA **B0** LL YY WW

This Errata is applicable only to the B0 revision of the chip.