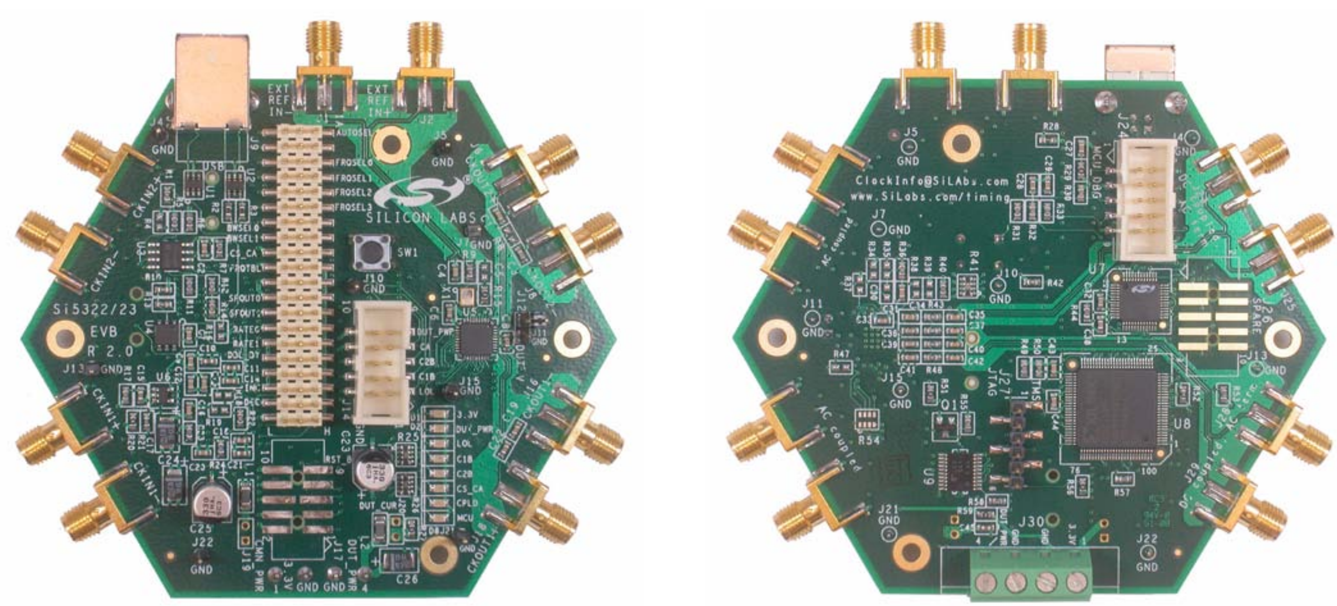
Si5316-EVB Si5319-EVB Si5322/23-EVB Si5324-EVB Si5325/26-EVB

Si5316, Si5319, Si5322/23, Si5324, and Si5325/26 EVB User's Guide

1. Introduction

The Si5316-EVB, Si5319-EVB, Si5322/23-EVB, Si5324-EVB, and Si5325/26-EVB provide platforms for evaluating Silicon Laboratories' Si5316, Si5319, Si5322/Si5323, Si5324, and Si5325/Si5326 Any-Rate Precision Clocks. The Si5316, Si5322, and Si5323 are controlled directly using configuration pins on the devices, while the Si5324, Si5325, and Si5326 are controlled by a microprocessor or MCU (micro-controller unit) via an I^2C or SPI interface. The Si5316 is a jitter attenuator with a loop bandwidth ranging from 60 Hz to 8.4 kHz. The Si5322 and Si5325 are low jitter clock multipliers with a loop bandwidth ranging from 30 kHz to 1.3 MHz. The Si5319, Si5323, and Si5326 are jitter-attenuating clock multipliers, with a loop bandwidth ranging from 60 Hz to 8.4 kHz. The Si5324 has features and capabilities very similar to the Si5326, but has much lower loop bandwidths that range from 4 to 525 Hz. The Si5326 device can optionally be configured to operate as a Si5325, so a single evaluation board is available to evaluate both devices. Likewise, the Si5323 can be configured to operate as a Si5322, so the two devices share a single evaluation board.

The Si5316/19/22/23/25/26 Any-Rate Precision Clocks are based on Silicon Laboratories' third-generation DSPLL® technology, which provides any-rate frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The devices have excellent phase noise and jitter performance. The Si5316 is a jitter attenuator that supports jitter generation of 0.3 ps RMS (typ) across the 12 kHz –20 MHz and 50 kHz–80 MHz jitter filter bandwidths. The Si5319, Si5323, and Si5326 jitter attenuating clock multipliers support jitter generation of 0.3 ps RMS (typ) across the 12 kHz–20 MHz and 50 kHz–80 MHz jitter filter bandwidths. The Si5322 and Si5325 support jitter generation of 0.6 ps RMS (typ) across the 12 kHz–20 MHz and 50 kHz–80 MHz jitter filter bandwidths. For all devices, the DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. These devices are ideal for providing clock multiplication/clock division, jitter attenuation, and clock distribution in mid-range and high-performance timing applications.



Top Bottom

Figure 1. Si532x QFN EVB

Table 1. Features by Part Number

Device PN	# Clock Inputs	# Clock Outputs	Control	Input Freq (MHz)	Output Freq (MHz)	Jitter Generation (12 kHz–20 MHz)	Prog. Loop BW	Clock Mult.	Hitless Switching	Alarms	Package
Any-Rate Precision Clock Multipliers											
Si5322	2	2	Pin	15 to 707	19 to 1050	0.6 ps rms typ	30 kHz–1.3 MHz	Y	N	LOS	6 x 6 36-QFN
Si5325	2	2	I^2C or SPI	10 to 710	10 to 1400	0.6 ps rms typ	30 kHz–1.3 MHz	Y	N	LOS, FOS	6 x 6 36-QFN
Any-Rate Precision Clock Multipliers with Jitter Attenuation											
Si5316	2	1	Pin	19 to 710	19 to 710	0.3 ps rms typ	60 Hz–8.4 kHz	N	N	LOL, LOS	6 x 6 36-QFN
Si5319	1	1	I^2C or SPI	.002 to 710	.002 to 1400	0.3 ps rms typ	60 Hz–8.4 kHz	Y	N	LOL, LOS	6 x 6 36-QFN
Si5323	2	2	Pin	.008 to 707	.008 to 1050	0.3 ps rms typ	60 Hz–8.4 kHz	Y	Y	LOL, LOS	6 x 6 36-QFN
Si5324	2	2	I^2C or SPI	.002 to 710	.002 to 1400	0.3 ps rms typ	4–525 Hz	Y	Y	LOL, LOS, FOS	6 x 6 36-QFN
Si5326	2	2	I^2C or SPI	.002 to 710	.002 to 1400	0.3 ps rms typ	60 Hz–8.4 kHz	Y	Y	LOL, LOS, FOS	6 x 6 36-QFN

2. Applications

The Si5316/19/22/23/25/26 Any-Rate Precision Clocks have a comprehensive feature set, including any-rate frequency synthesis, multiple clock inputs, multiple clock outputs, alarm and status outputs, hitless switching between input clocks, programmable output clock signal format (LVPECL, LVDS, CML, CMOS), output phase adjustment between output clocks, and output phase adjustment between all output clocks and the selected reference input clock (phase increment/decrement). For more details, consult the Silicon Laboratories timing products website at www.silabs.com/timing.

All five evaluation boards (EVBs) have an MCU (C8051F340) that support USB communications with a PC host. For the pin controlled parts (Si5316, Si5322, Si5324, and Si5323), the pin settings of the devices are determined by the MCU and the PC resident software that is provided with the EVB. For the MCU controlled parts (Si5319, Si5324, Si5325, and Si5326), the devices are controlled and monitored through the serial port (either SPI or I^2C). A CPLD sits between the MCU and the Any-Rate Precision Clock device that performs voltage level translation and stores the pin configuration data for the pin controlled devices. Jumper plugs are provided so that the user can bypass the MCU/CPLD to manually control the pin controlled devices. Ribbon headers and SMA connectors are included so that external clock in, clock out, and status pins can be easily accessed by the user. For the MCU controlled devices (Si5319, Si5324, Si5325, and Si5326), the user also has the option of bypassing the MCU and controlling the parts from an external serial device. On-board termination is included so that the user can evaluate single-ended or differential as well as ac or dc coupled clock inputs and outputs. A separate DUT (Device Under Test) power supply connector is included so that the Any-Rate Precision Clocks can be run at either 1.8, 2.5 or 3.3 V, while the USB MCU remains at 3.3 V. LEDs are provided for convenient monitoring of key status signals.

3. Features

The Si5316-EVB, Si5319-EVB, Si5322/23-EVB, Si5324-EVB, and Si5325/26-EVB each include the following:

- CD with documentation and EVB software including the DSPLL*sim* configuration software utility
- USB cable
- EVB circuit board including an Si5316 (Si5316-EVB), Si5319 (Si5319-EVB), Si5323 (Si5322/23-EVB), Si5324 (Si5324-EVB), or Si5326 (Si5325/26-EVB)
- User's Guide (this document)

4. Si5316-EVB, Si5319-EVB, Si5322/23-EVB, Si5324-EVB, and Si5325/26-EVB Quick Start

1. A CD-ROM is included with the evaluation board. On this CD, there is a file named "install_instructions.PDF". This file gives the detailed instructions on how to install the drivers and software that control the evaluation board.
2. Connect the two power supplies to the EVB. One is 3.3 V and the other is 1.8, 2.5, or 3.3 V. The DUT is powered by the 1.8/2.5/3.3 V supply.
3. Turn on the power supplies.
4. Connect a USB cable from the EVB to the PC where the software was installed.
5. Install USB driver.
6. Launch software by clicking on **Start**→**Programs**→**Silicon Laboratories**→**Precision Clock EVB Software** and selecting one of the programs.

5. Functional Description

The Si5316-EVB, Si5319-EVB, Si5322/23-EVB, Si5324-EVB, Si5325/26-EVB, and software allow for a complete and simple evaluation of the functions, features, and performance of the Si5316, Si5319, Si5322, Si5323, Si5325, and Si5326 Any-Rate Precision Clocks.

5.1. Narrowband versus Wideband Operation

This document describes five evaluation boards: Si5316, Si5319, Si5322/23, Si5324, and Si5325/26. The Si5316 and Si5322/23 evaluation boards are for pin controlled clock parts and the Si5319, Si5324, and Si5325/26 are for clock parts that are to be controlled by an MCU over a serial port. The Si5316-EVB, Si5319-EVB, and Si5324-EVB support only one part, while the two other boards each support two parts: one that is wideband (the Si5322 and the Si5325) and one that is narrowband (the Si5323 and the Si5326). The narrowband parts are both capable of operating in the wideband mode, so evaluation of the wideband parts can be done by using a narrowband part in wideband mode. As such, these evaluation boards are only populated with narrowband parts.

The Si5324-EVB is a special case because the Si5324 has a lower loop bandwidth and does not support wideband operation. Because of the lower loop bandwidth, the lock times are significantly increased and the Si5324 will be more sensitive to XA-XB reference crystal temperature changes. For this reason, a 20 ppm crystal is used on the SI5324-EVB. It should be noted that the 20 ppm crystal is used for its temperature stability, not its absolute accuracy. If the crystal will undergo significant changes in temperature, it is suggested that the crystal be thermally insulated by covering it with foam tape or some other means.

To evaluate Si5322 device operation using the Si5322/23-EVB, the RATE[1:0] pins must be set to LL using the jumpers provided. To evaluate Si5325 device operation using the Si5325/26-EVB, the Precision Clock EVB Software should be configured for wideband mode. For details, see the Precision Clock EVB Software documentation.

5.2. Block Diagram

Figure 2 is a block diagram of the evaluation board and it is helpful to refer to this diagram. The MCU communicates to the host PC over a USB connection. The MCU controls and monitors the Si532x through the CPLD. The CPLD, among other tasks, translates the signals at the MCU voltage level of 3.3 V to the Si532x's voltage level, which is nominally 3.3, 2.5, or 1.8 V. The user has access to all of the Si532x's pins using the various jumper settings as well as through the host PC via the MCU and CPLD.

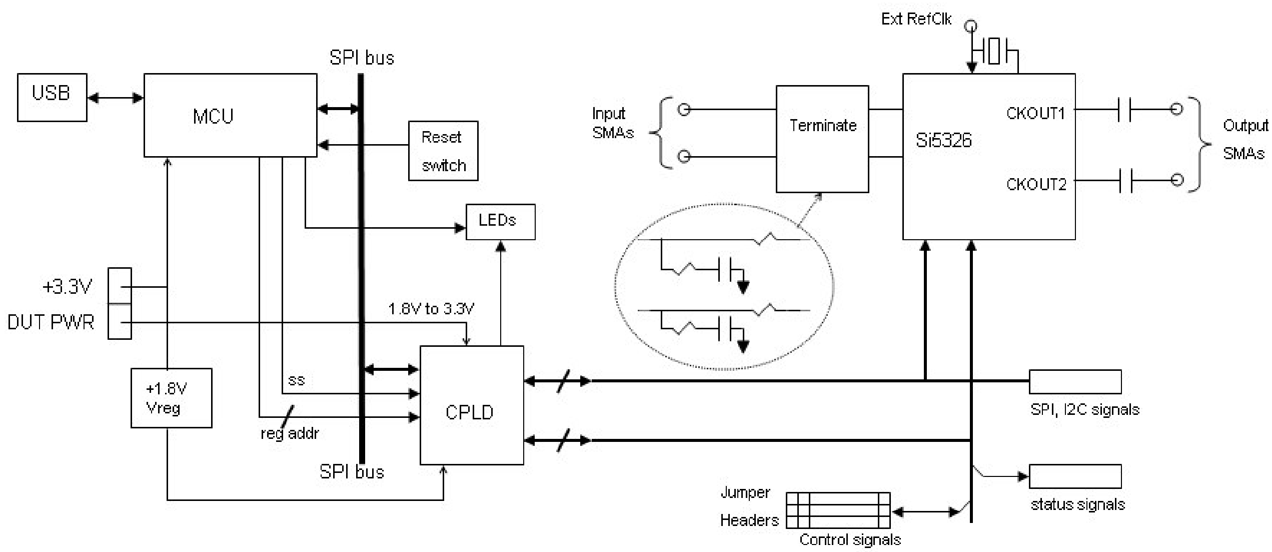


Figure 2. Si532x QFN Block Diagram

5.3. Si532x Input and Output Clocks

The Si532x has two differential inputs that are ac terminated to 50 Ω and then ac coupled to the part. Single-ended operation can be implemented by simply not connecting to one of the two of the differential pairs bypassing the unused input to ground with a capacitor. When operating with clock inputs of 1 MHz or less in frequency, the appropriate dc blocking capacitors (C39, C41, C34 and C36) located on the bottom of the board should be replaced with zero ohm resistors. The reason for this is that the capacitive reactance of the ac coupling capacitors becomes significant at low frequencies. It is also important that the CKIN signal meet the minumum rise time of 11 ns (CKNtrf) even though the input frequency is low.

The two clock outputs (one for the Si5316-EVB and Si5319-EVB) are all differential, AC coupled and configured for driving 50 ohm transmission lines. **When using single ended outputs, it is important that the unused half of the output be terminated**.

Two jumpers are provided to assist in monitoring the Si532x power: When R27 is removed, J20 can be used to measure the device current. J12 can be used at any time to monitor the supply voltage at the device.

The Si5319, Si5323 and Si5326 require that an external reference clock be provided to enable the devices to operate as narrowband jitter attenuators with loop bandwidths as low as 60 Hz (4 Hz for the Si5324). The external reference clock can be either a crystal, a standalone oscillator or some other clock source. The range of acceptable reference frequencies is described in the Any-Rate Precision Clocks Family Reference Manual (Si53xxRM.pdf). The EVBs are shipped with a 3rd overtone 114.285 MHz crystal that is used in the majority of applications. J1 and J2 are used when the Si532x is to be configured in narrowband mode with an external reference oscillator (i.e. without using the 114.285 MHz crystal).

The RATE pins should also be configured for the desired mode, using the jumper plugs at J9 (see Table 6).

For unused inputs and outputs, please refer to the Any-Rate Precision Clocks Family Reference Manual (Si53xxRM.pdf).

Table 2 shows how the various components should be configured for the three modes of operation.

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Table 2. Reference Input Mode

	Mode		
	Xtal[1]	Ext Ref[2]	Wide Band
Input 1	NC[3]	J1	NC
Input 2	NC	J2	NC
C30	NOPOP[4]	install	install
C5	NOPOP	install	NOPOP
R34	NOPOP	NOPOP	install
R15	install	NOPOP	NOPOP
RATE0	M	—	H
RATE1	M	—	H

Notes:
1. Xtal is 114.285 MHz 3rd overtone.
2. For external reference frequencies and RATE pin settings, see the Si53xx-RM Any-Rate Precision Clock Family Reference Manual.
3. NC—no connect.
4. NOPOP—do not install this component.

For a differential external reference, connect the balanced input signals to J1 and J2. For single-ended operation, connect the input signal to J2 and disconnect J1.

R35 is provided so that a different termination scheme can be used. If R35 is populated, then remove R9 and R36.

5.4. Two and Three Level Inputs

The two-level and three-level inputs can all be manually configured by installing jumper plugs at J9. The two level inputs are either H or L. For the three-level inputs, the M level is achieved by not installing a jumper plug at a given location. J9 can also be used as a connection to an external circuit that controls these pins. J17 is a ten pin ribbon header that is provided so that an external processor can control the Si532x over either the SPI or I^2C bus.

J14 is another ten pin ribbon header that brings out all of the status outputs from the Si532x. Note that some pins are shared and serve as both inputs and outputs, depending on how the device is configured. For users that wish to remotely access the input and output pins settings as well as serial ports with external hardware, all three of these headers can be connected to ribbon cables.

5.5. CPLD and Power

This CPLD is required for the MCU to control the Si532x. The CPLD provides two main functions: it translates the voltage level from 3.3 V (the MCU voltage) to the Si532x voltage (either 1.8, 2.5, or 3.3 V). The MCU communicates to the CPLD with the SPI signals SS_CPLD_B (slave select), MISO (master in, slave out), MOSI (master out, slave in), and SCLK. The MCU can talk to CPLD-resident registers that are connected to pins that control the Si532x's pins, mainly for pin control mode. When the MCU wishes to access a Si532x register, the SPI signals are passed through the CPLD, while being level translated, to the Si532x. The CPLD is an EE device that retains its code and is loaded through the JTAG port (J27). The core of the CPLD runs at 1.8 V, which is provided by voltage regulator U6. The CPLD also logically connects many of the LEDs to the appropriate Si532x pins.

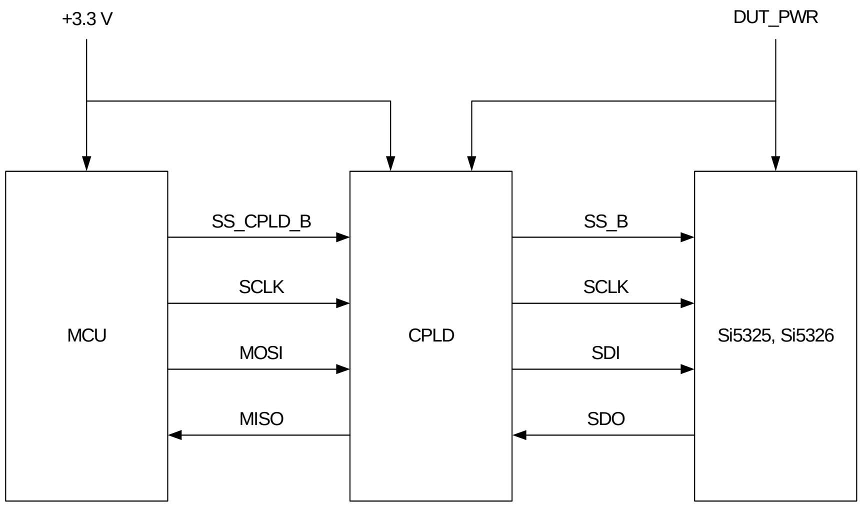


Figure 3. SPI Mode Serial Data Flow

This evaluation board requires two power inputs +3.3 V for the MCU and either 1.8, 2.5, or 3.3 V for the Any-Rate Precision Clock part. The power connector is J30. The grounds for the two supplies are tied together on the EVB. There are eight LEDs, as described in Table 3.

The Evaluation board has a serial port connector (J17) that supports the following:

- Control by the MCU/CPLD of an Any-Rate part on an external target board.
- Control of the Any-Rate part that is on the Eval board through an external SPI or I^2C port.

For details, see J17 (Table 5).

Though they are not needed on this Evaluation Board because the CPLD has low output leakage current, some applications will require the use of external pullup and pulldown resistors when three level pins are being driven by external logic drivers. This is particularly true for the pin-controlled parts: the Si5316, Si5322 and Si5323. Consult the Si53xx-RM Any-Rate Precision Clock Family Reference Manual for details.

5.6. MCU

The MCU is responsible for connecting the evaluation board to the PC so that PC resident software can be used to control and monitor the Si532x. The USB connector is J3 and the debug port, by which the MCU is flashed, is J24. The reset switch, SW1, resets the MCU, but not the CPLD. The MCU is a self-contained USB master and runs all of the code required to control and monitor the Si532x, both in the MCU mode and in the pin-controlled modes.

U4 contains a unique serial number for each board and U3 is an EEPROM that is used to store configuration information for the board. The board powers up in free run mode with a configuration that is outlined in "Appendix—Powerup and Factory Default Settings" on page 23.

For the pin controlled parts (Si5316-EVB and Si5322/23-EVB), the contents of U3 configure the board on powerup so that jumper plugs may be used.

If DSPLLsim is subsequently run, the jumper plugs should be removed before DSPLLsim downloads the configuration to the EVB so that the jumpers do not conflict with the CPLD outputs.

For microprocessor parts, U3 configures the EVB for a specific frequency plan as described in "Appendix—Powerup and Factory Default Settings" on page 23.

LVPECL outputs will not function at 1.8 V. If the Si532x part is to be operate at 1.8 V, the output format needs to be changed by altering either the SFOUT pins (Si5316/22/23) or the SFOUT register bits (Si5319/25/26).

6. Connectors and LEDs

6.1. LEDs

There are eight LEDs on the board which provide a quick and convenient means of determining board status.

Table 3. LED Status and Description

LED	Color	Label
D1	Green	3.3 V
D2	Green	DUT_PWR
D5	Red	LOL
D4	Red	C1B
D6	Red	C2B
D3	Green	CA
D7	Yellow	CPLD
D8	Yellow	MCU

6.2. User Jumpers and Headers.

Use the following to locate the jumpers described below:

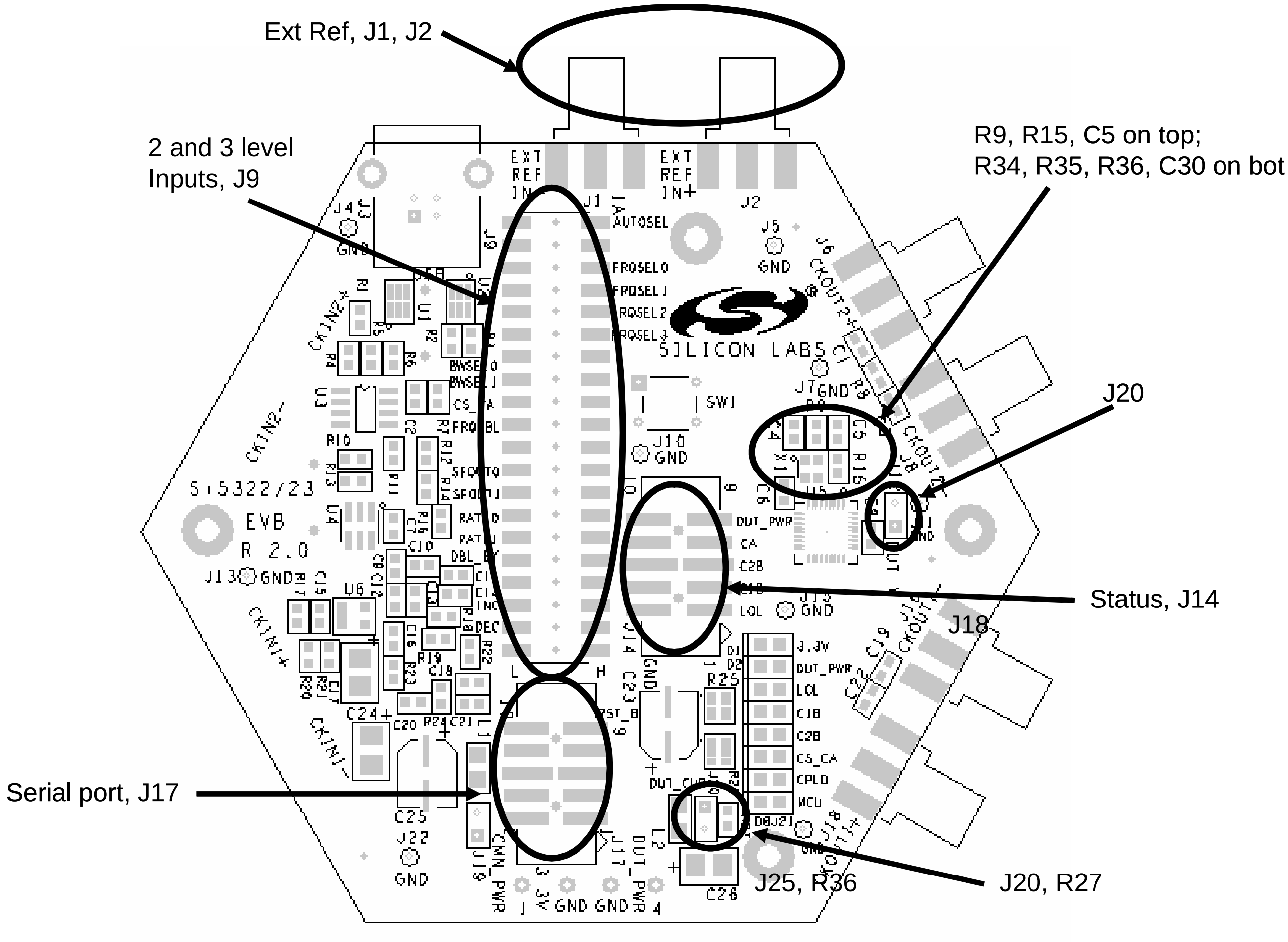


Figure 4. Connectors, Jumper Header Locations

J20 assists in measuring the Any-Rate Precision Clock current draw. If J20 is to be used, R27 should be removed.

J14 is a 10 pin ribbon header that provides an external path to monitor the status pins.

Table 4. Status Header, J14

J14	Pin	Comment
J14.1	LOL	
J14.3	C1B	
J14.5	C2B	
J14.7	CS_CA	clock active
J14.9	DUT_PWR	

J17 is a 10 pin ribbon header that provides an external path to serially communicate with the Any-Rate Precision Clock.

To control the Any-Rate part that is on the Evaluation Board from an external serial port, open the Register Programmer, connect to the Evaluation Board, go to Options in the top toolbar, and select "Switch To External Control Mode."

To control an Any-Rate part that is on an external target board from the Evaluation Board using its serial port, tie pin 9 of J17 low so that the on-board Any-Rate part is constantly being held in reset. This will force it to disable its SDA_SDO output buffer. This will work only for Evaluation Boards that have Rev C or higher Any-Rate parts.

Table 5. External Serial Port Connector, J17

J17	Pin	Comment
J17.1	SDA_SDO	
J17.3	SCL_SCLK	
J17.5	SDI	
J17.7	A2_SS	
J17.9	DUT_RST_B	not reset

J9 is a three-pin by twenty header that is used to establish input levels for the pin controlled two and three-level inputs using jumper plugs. It also provides a means of externally driving the two and three-level input signals.

Table 6. Two and Three Level Input Jumper Headers, J9

J9	Pin
J9.1B	AUTOSEL
J9.2B	CMODE
J9.3B	A0_FRQSEL0
J9.4B	A1_FRQSEL1
J9.5B	A2_SS_FRQSEL2
J9.6B	SDI_FRQSEL3
J9.7B	SCL_SCLK_BWSEL0
J9.8B	SDA_SDO_BWSEL1
J9.9B	CS_CA
J9.10B	FRQTBL

J9	Pin	Comment
J9.11B	—	not used
J9.12B	SFOUT0	
J9.13B	SFOUT1	
J9.14B	RATE0	
J9.15B	RATE1	
J9.16B	DBL2_BY	
J9.17B	—	not used
J9.18B	INC	
J9.19B	DEC	
J9.20B	—	not used

J12 is used to monitor the Any-Rate Precision Clock voltage.

J1 and J2 are edge mount SMA connectors that are used, if so configured, to supply an external single-ended or differential 38.88 MHz reference oscillator.

7. EVB Software Installation

The following sections describe how to install the EVB software.

Note: These programs can control any of the Any-Rate Precision Clock devices including the Si5316, Si532x, and Si536x devices. This software can be installed once per PC and used for all available Precision Clock EVBs.

7.1. PC System Requirements

- Microsoft Windows 2000 or Windows XP
- USB 1.1 or USB 2.0
- 3 MB of hard drive space
- 1024 x 768 screen resolution or greater (1280 x 1024 recommended)
- Microsoft .NET Framework 1.1
- Precision Clock EVB Driver (**Note**: The Precision Clock EVB driver is provided with the installation files.)

7.2. Microsoft .NET Framework Installation

The Microsoft .NET Framework is required before installing and running the Precision Clock EVB software. Details and installation information about the .NET Framework are available via a shortcut in the NETFramework directory on the installation CD or at the following web site:

http://www.microsoft.com/downloads/details.aspx?FamilyId=262D25E3-F589-4842-8157-034D1E7CF3A3&displaylang=en

Contact your system administrator for more details.

7.3. Precision Clock EVB Driver

The EVB requires a driver to be controlled by the software. The following section lists the steps for installing and uninstalling the driver.

7.3.1. Install

The driver files must be installed before the EVB is connected to the PC via the USB cable. This installation usually only needs to be completed once per PC.

1. Navigate to the "EVBDriver" directory on the CD.
2. Double-click on the PreInstaller.exe file to run the installation program for the driver.
3. Click Install in the dialog box. Be sure to select a location on the PC's hard drive for the files, if necessary.
4. If the PC is running Windows XP, click **Continue Anyway** when the wizard warns that the driver does not pass the Windows Logo verification for XP.

After the above files are installed, the operating system will be able to identify the EVB's USB controller when the EVB is connected to the PC. The following steps occur when the EVB is connected to the PC for the first time.

- For Windows 2000, when the EVB is connected to the PC, the operating system will display a dialog box indicating that it found new hardware. No other action is required. The driver installation can be verified in the Device Manager under the USB section; look for "Precision Clock EVB" in the list.
- For Windows XP:
    1. When the EVB is connected to the PC, the **Found New Hardware** wizard will appear. Use the default settings that will tell the PC to look for the driver.
    2. Again, ignore the warning about the driver not passing verification by clicking **Continue Anyway**.
    3. Click **Finish** to complete the install.

7.3.2. Uninstall

In the Control Panel, select Add/Remove Programs. Then select "Precision Clock EVB Driver Set" and click **Change/ Remove**. The wizard will remove the associated files.

7.4. Precision Clock EVB Software Installation

To install:

1. Navigate to the "PrecisionClockEVBSoftware" directory.
2. Double-click on the **Setup.exe** file
3. Follow the steps in the wizard to install the program. Note: Use the default installation location for best results.
4. After the installation is complete, click on **Start→Programs→Silicon Laboratories→Precision Clock EVB Software**. Select one of the programs to control the EVB.
5. Refer to the online help in each program by clicking **Help→Help**.

To uninstall:

1. Open Add/Remove Programs in the Control Panel.
2. Select the Precision Clock EVB Software, and click **Remove**.
3. Follow the steps in the wizard to complete the removal.

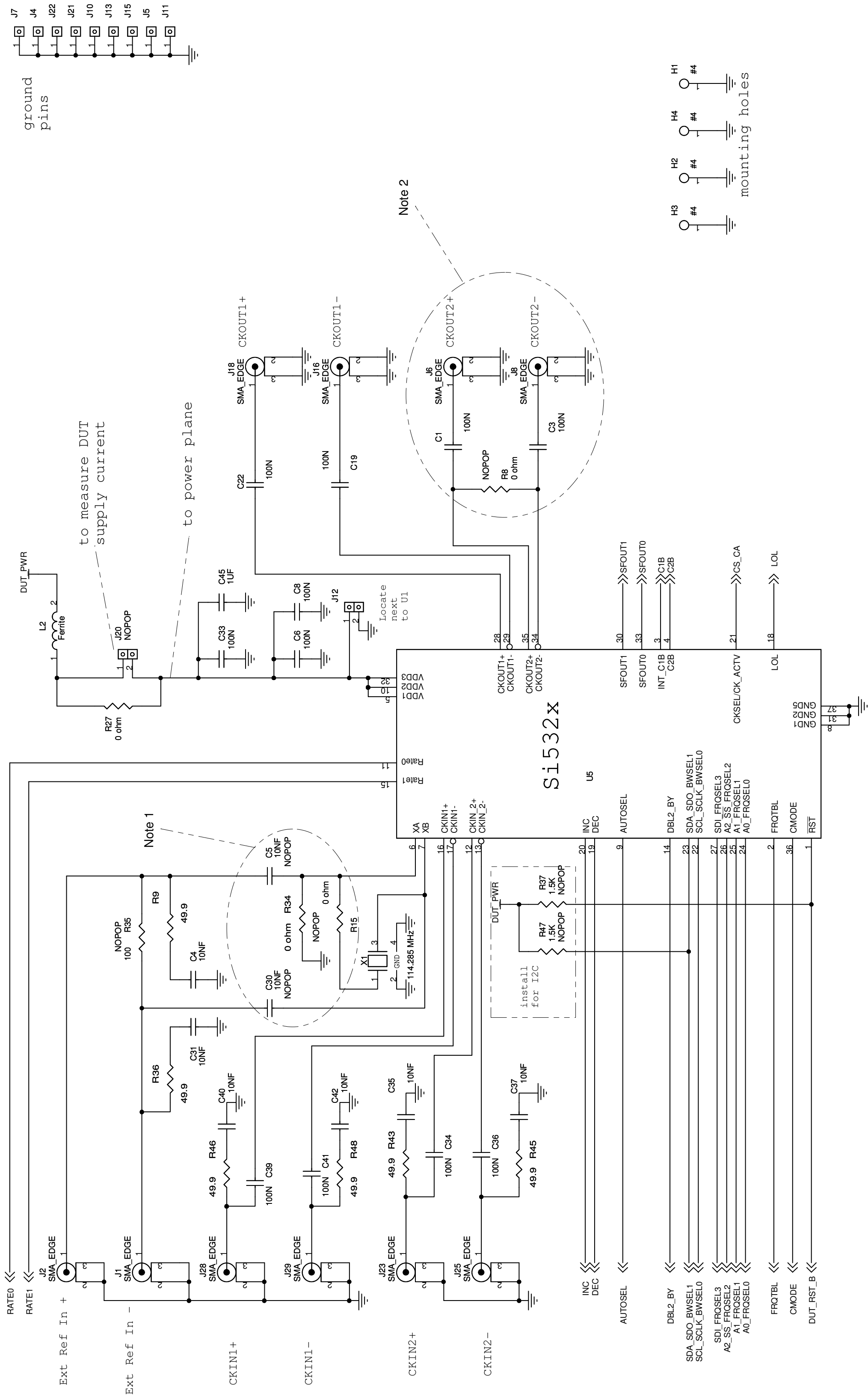
7.5. Precision Clock EVB Software Description

There are several programs to control the Precision Clock device. Each provides a different kind of access to the device. Refer to the online help in each program by clicking **Help→Help** in the menu for more information on how to use the software. Note: Some of the Precision Clock devices do not have a register map, so some programs may not be applicable to them.

Table 7. User Applications

Program	Description
Register Viewer	The Register Viewer displays the current register map data in a table format sorted by register address to provide an overview of the device's state. This program can save and print the register map.
Register Programmer	The Register Programmer provides low-level register control of the device. Single and batch operations are provided to read from and write to the device. Register map files can be saved and opened in the batch mode.
Setting Utility	This application allows for quick access to each control on the Precision Clock device (either pin- or register-based). It can save and open text files as well.
DSPLL*sim*	The DSPLL*sim* provides high-level control of the Precision Clock device. It has the frequency planning wizard as well as control of the pins and registers in a organized, intuitive manner.

8. Schematics



Notes:

1. Change for Si5322, Si5325, and External Reference.
2. NOPOP for Si5316.

Figure 5. Si532x

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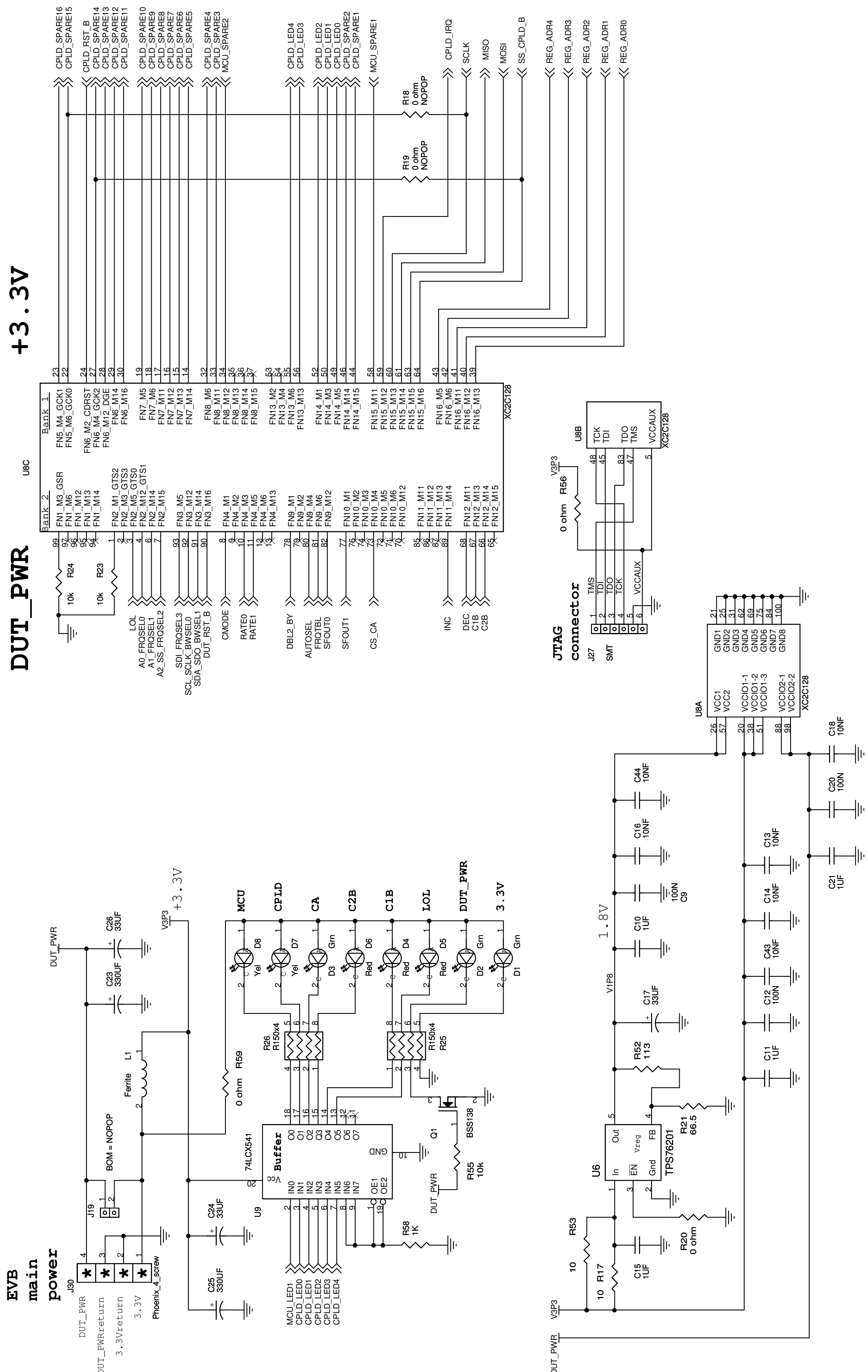


Figure 6. CPLD and Power

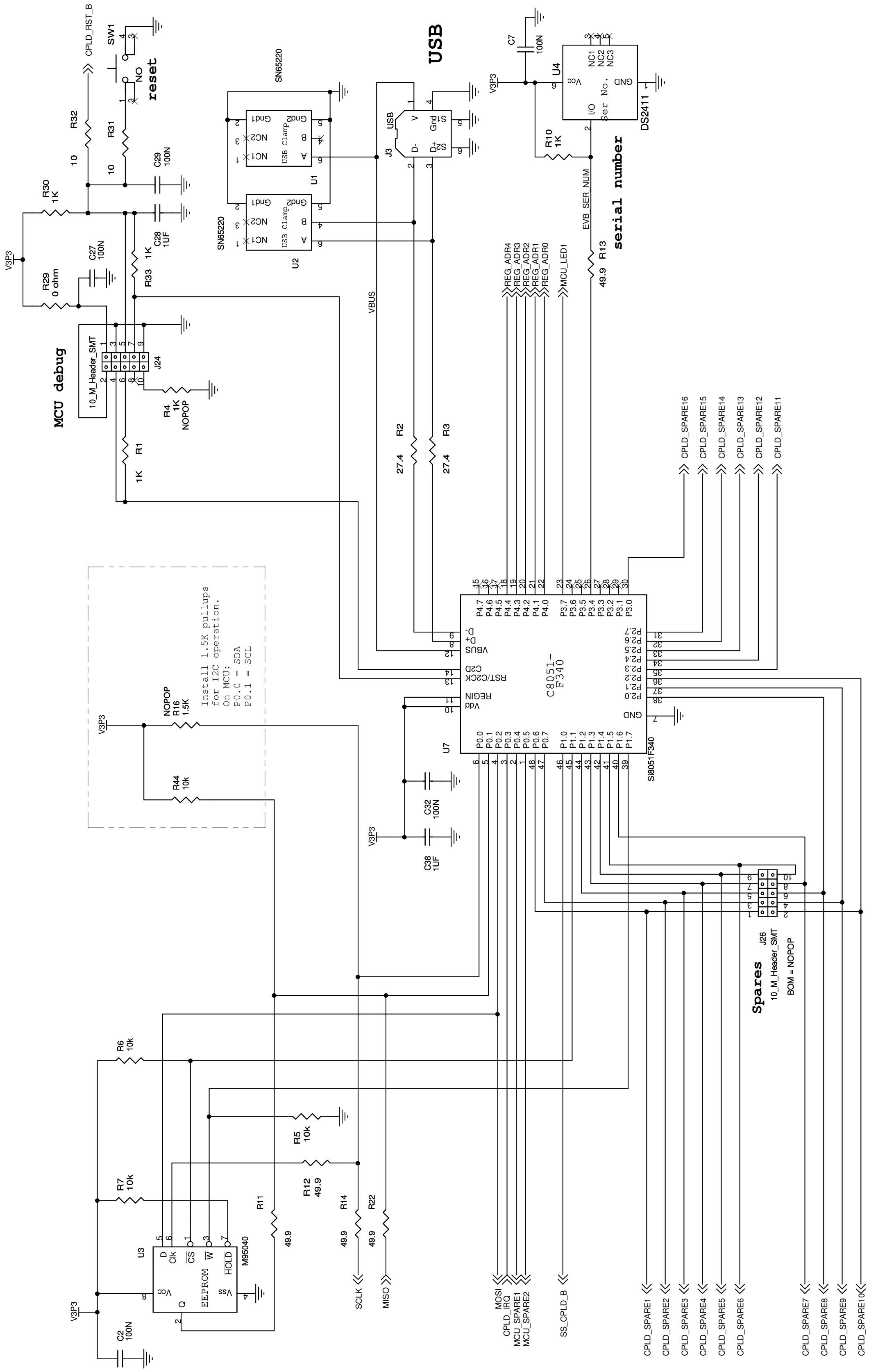
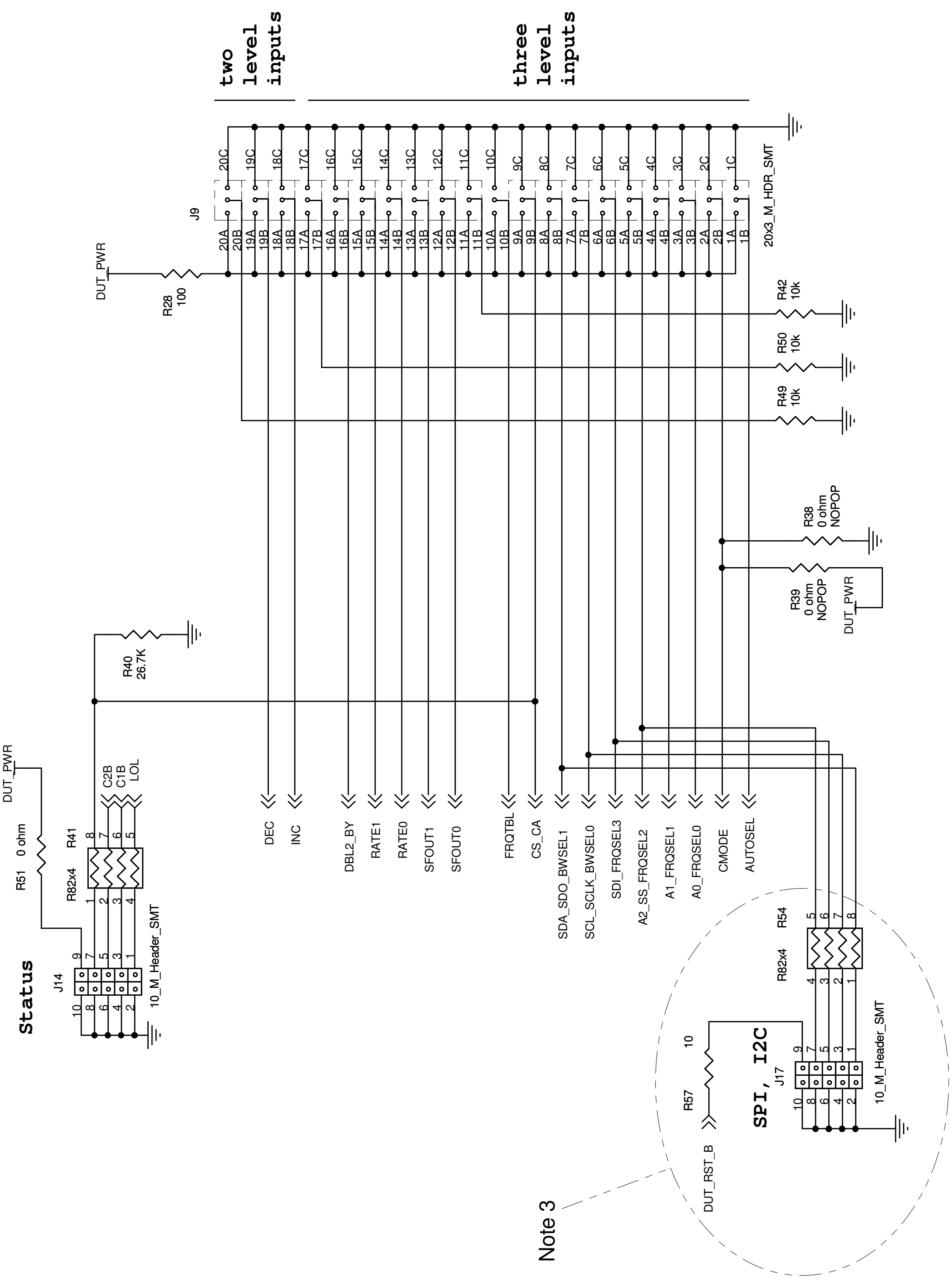

MCU debug
reset
USB
serial number
Spares
Install 1.5K pullups
for I2C operation.
On MCU:
P0.0 = SDA
P0.1 = SCL
C8051-F340
Si8051F340
U7
J24
10_M_Header_SMT
J26
10_M_Header_SMT
BOM = NOPOP
SN65220
U1
U2
J3
U4
DS2411
U3
M95040
EEPROM
SW1
CPLD_RST_B
REG_ADR4
REG_ADR3
REG_ADR2
REG_ADR1
REG_ADR0
MCU_LED1
EVB_SER_NUM
VBUS
V3P3
SCLK
MISO
MOSI
CPLD_IRQ
MCU_SPARE1
MCU_SPARE2
SS_CPLD_B
CPLD_SPARE1
CPLD_SPARE2
CPLD_SPARE3
CPLD_SPARE4
CPLD_SPARE5
CPLD_SPARE6
CPLD_SPARE7
CPLD_SPARE8
CPLD_SPARE9
CPLD_SPARE10
CPLD_SPARE11
CPLD_SPARE12
CPLD_SPARE13
CPLD_SPARE14
CPLD_SPARE15
CPLD_SPARE16

Figure 7. MCU



Note: NOPOP for Si5316, Si5322, and Si5323.

Figure 8. Two and Three Level Inputs

9. Bill of Materials

Table 8. Bill of Materials

Item	Qty	Reference	Part	Mfgr	MfgrPartNum
1	19	C1,C2,C3,C6,C7,C8,C9,C12,C19,C20, C22,C27,C29,C32,C33,C34,C36,C39, C41	100 N	Venkel	C0603X7R160-104KNE
2	12	C4,C13,C14,C16,C18,C31,C35,C37, C40,C42,C43,C44	10 NF	Venkel	C0603X7R160-103KNE
4	7	C10,C11,C15,C21,C28,C38,C45	1 UF	Venkel	C0603X7R6R3-105KNE
5	3	C17,C24,C26	33 UF	Venkel	TA0006TCM336MBR
6	2	C23,C25	330 UF	Panasonic	EEE-HA0J331XP
7	3	D1,D2,D3	Grn	Lumex	SML-LXT0805GW-TR
8	3	D4,D5,D6	Red	Lumex	SML-LXT0805SRW-TR
9	2	D7,D8	Yel	Lumex	SML-LXT0805YW-TR
10	4	H1,H2,H3,H4	#4 mounting hole		
11	10	J1,J2,J6,J8,J16,J18,J23,J25,J28,J29	SMA_EDGE	Johnson	142-0701-801
12	1	J3	USB	FCI	61729-0010BLF
13	9	J4,J5,J7,J10,J11,J13,J15,J21,J22	Jmpr_1pin		
14	1	J9	20x3_M_HDR_SMT	Samtec	TSM-120-01-L-TV
15	1	J12	Jmpr_2pin		
16	3	J14,J17,J24	10_M_Header_SMT	Samtec	HTST-105-01-lm-dv-a
19	1	J27	SMT	Sullins	GZC36SABN-M30
20	1	J30	Phoenix_4_screw	Phoenix	MKDSN 1.5/4-5.08
21	2	L1,L2	Ferrite	Venkel	FBC1206-471H
22	1	Q1	BSS138	On Semi	BSS138LT1G
23	5	R1,R10,R30,R33,R58	1 K	Venkel	CR0603-16W-1001FT
24	2	R2,R3	27.4	Venkel	CR0603-16W-27R4FT
26	10	R5,R6,R7,R23,R24,R42,R44,R49,R50, R55	10 k	Venkel	CR603-16W-1002FT
28	11	R9,R11,R12,R13,R14,R22,R36,R43, R45,R46,R48	49.9	Venkel	CR0603-16W-49R9FT
29	7	R15,R20,R27,R29,R51,R56,R59	0 ohm	Venkel	CR0603-16W-000T
31	5	R17,R31,R32,R53,R57	10	Venkel	CR0603-16W-10R0FT
32	1	R21	66.5	Venkel	CR0603-16W-66R5FT
33	2	R25,R26	R150x4	Panasonic	EXB-38V151JV
34	1	R28	100	Venkel	CR0603-16W-1000FT
36	1	R40	26.7 K	Venkel	CR0603-16W-2672FT
37	2	R41,R54	R82x4	Panasonic	EXB-38V820JV

Table 8. Bill of Materials (Continued)

Item	Qty	Reference	Part	Mfgr	MfgrPartNum
38	1	R52	113	Venkel	CR0603-16W-1130FT
39	1	SW1	NO	Mountain Switch	101-0161-EV
40	2	U1,U2	SN65220	TI	SN65220DBVT
41	1	U3	M95040	ST Micro	M95040-WMN6P
42	1	U4	DS2411	Maxim/Dallas	DS2411P
43	1	U5	Si5326A-X-GM*	Silicon Labs	Si5326A-X-GM
44	1	U6	TPS76201	TI	TPS76201DBVT
45	1	U7	Si8051F340	Silicon Labs	C8051F340-GQ
46	1	U8	XC2C128	Xilinx	XC2C128-7VQG100I
47	1	U9	74LCX541	Fairchild	74LCX541MTC_NL
48	1	X1	114.285 MHz	TXC	7MA1400014
49	1	X1 for the Si5324	114.285 MHz 20 ppm	NDK	EXS00A-CS00997
Not Populated					
3	2	C5,C30	10NF	Venkel	C0603X7R160-103KNE
17	2	J19,J20	Jmpr_2pin		
18	1	J26	10_M_Header_SMT	Samtec	HTST-105-01-lm-dv-a
25	1	R4	1 K	Venkel	CR0603-16W-1001FT
27	6	R8,R18,R19,R34,R38,R39	0 ohm	Venkel	CR0603-16W-000T
30	3	R16,R37,R47	1.5 K	Venkel	CR0603-16W-1501FT
35	1	R35	100	Venkel	CR0603-16W-1000FT

Note: X denotes the product revision. Consult the ordering guide in the Si5326 data sheet for the latest product revision.
For the Si5322/23-EVB, substitute Si5323-X-GM.
For the Si5316-EVB, substitute Si5316-X-GM.
For the Si5319-EVB, substitute Si5319-X-GM.
For the Si5324-EVB, substitute Si5324-X-GM.

10. Layout

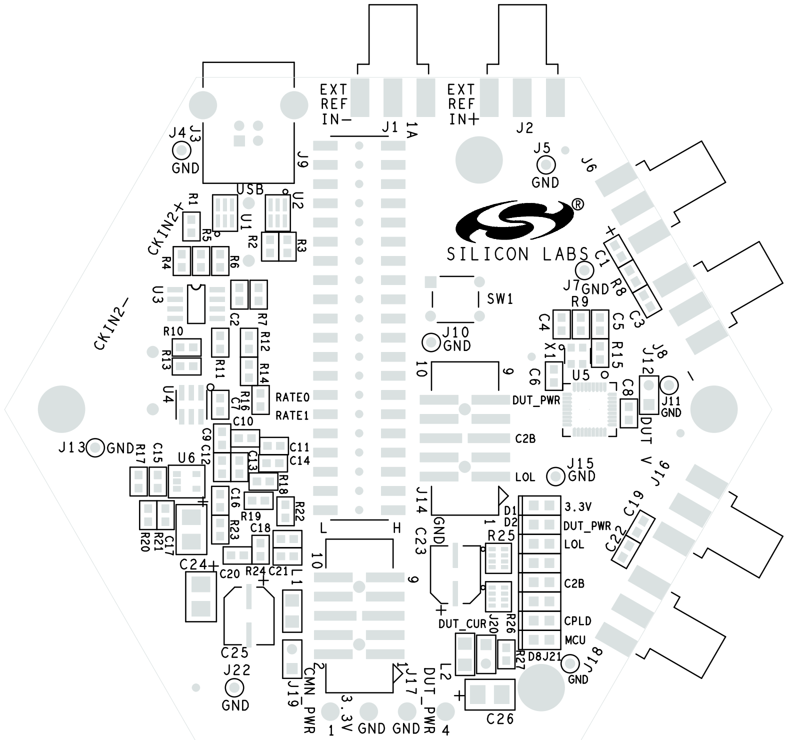


Figure 9. Silkscreen Top

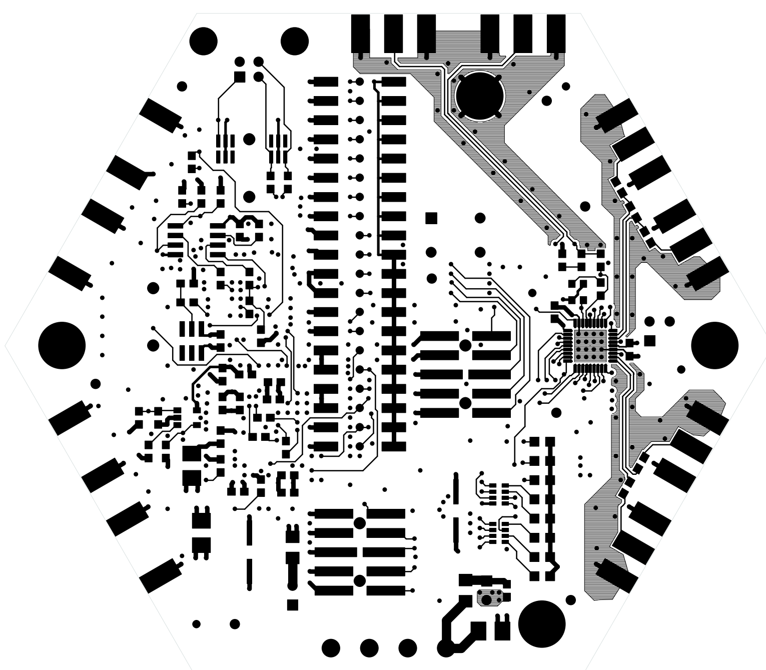


Figure 10. Layer 1

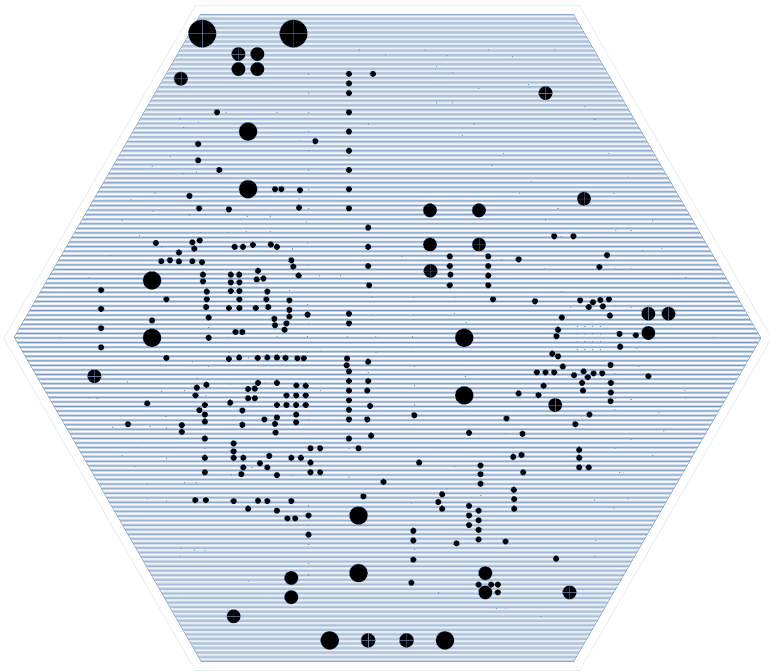


Figure 11. Layer 2, Ground Plane

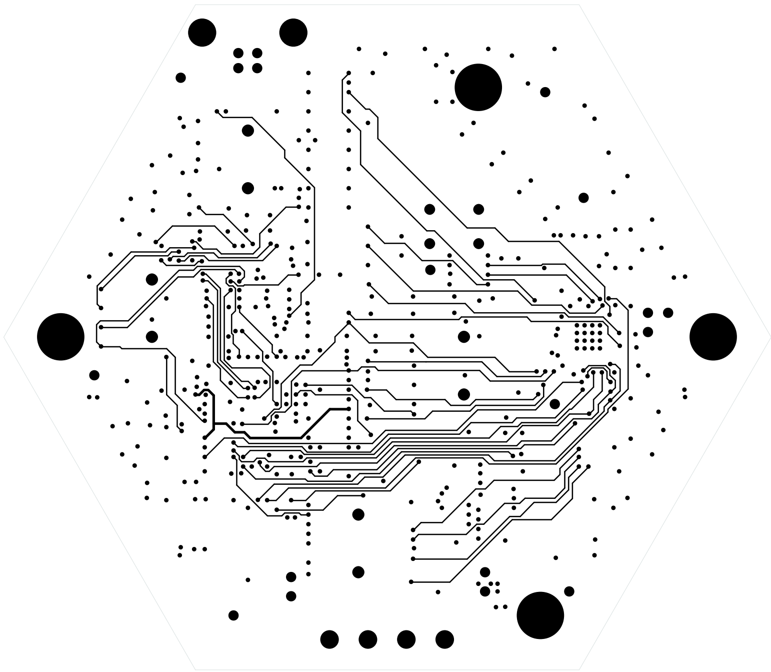


Figure 12. Layer 3

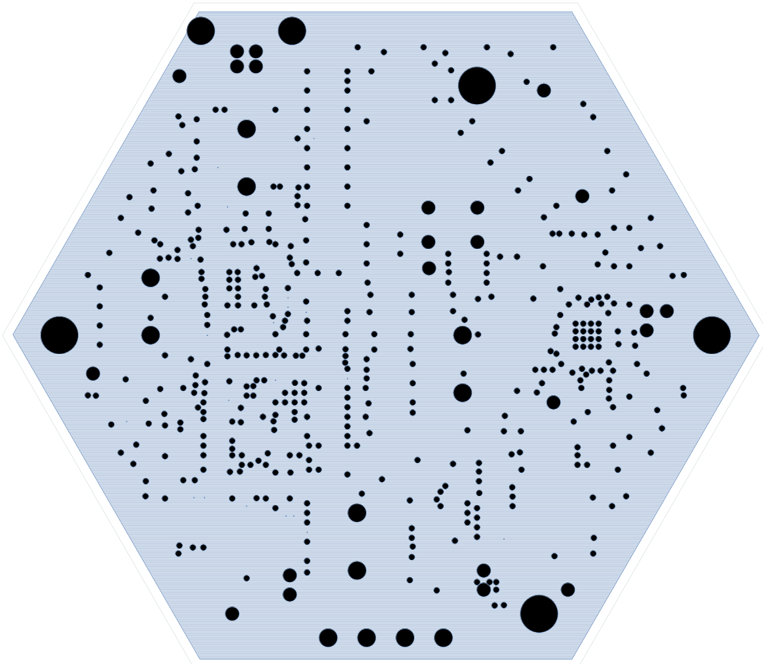


Figure 13. Layer 4, 3.3 V Power

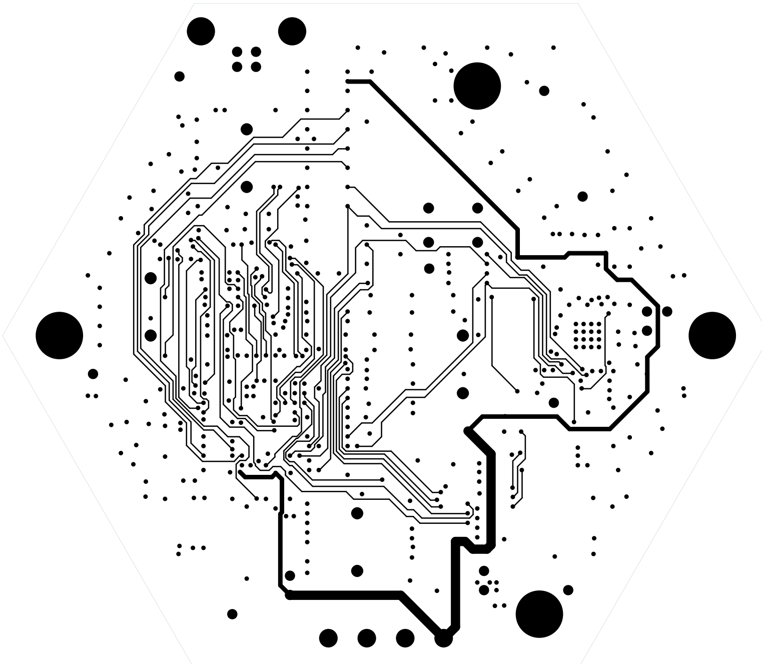


Figure 14. Layer 5

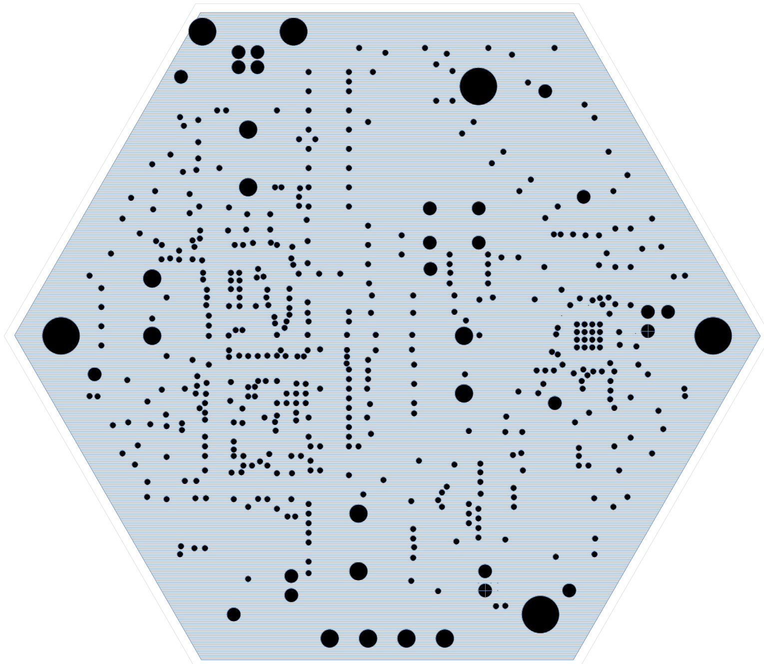


Figure 15. Layer 6, DUT Power

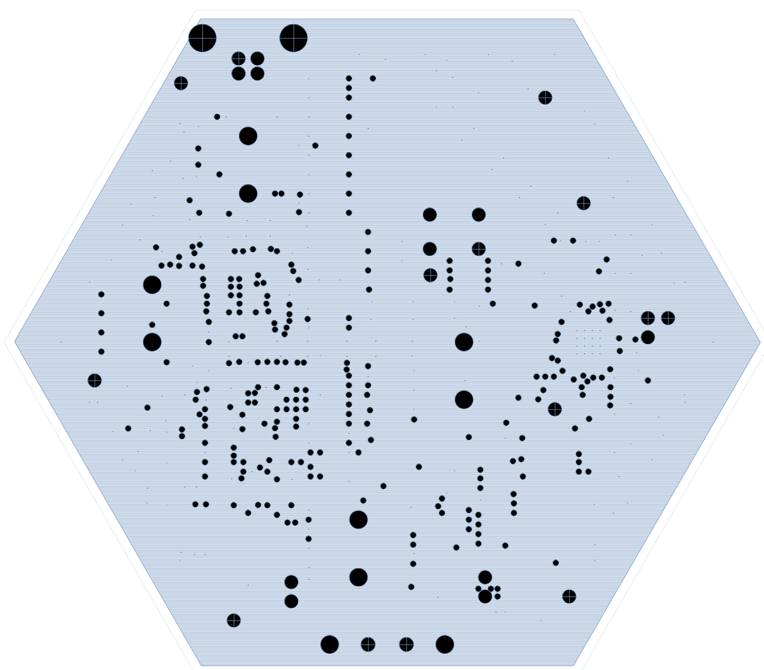


Figure 16. Layer 7, Ground Plane

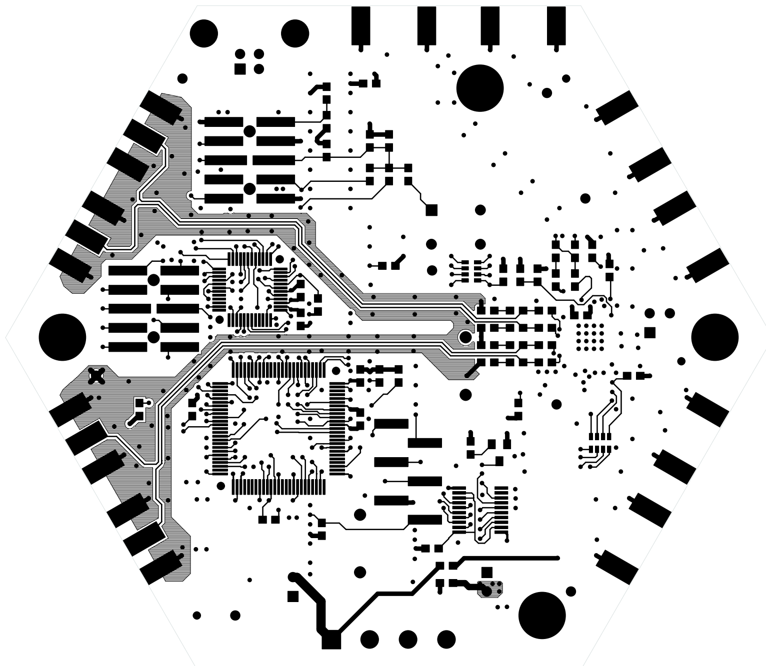


Figure 17. Layer 8

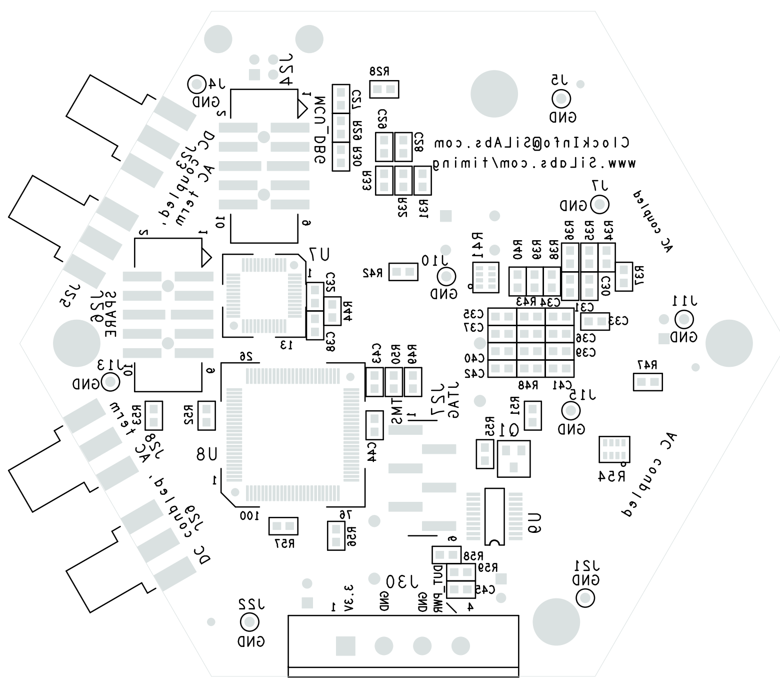


Figure 18. Silkscreen Bottom

APPENDIX—POWERUP AND FACTORY DEFAULT SETTINGS

For the Si5324-EVB and Si5325/26-EVB, the power up settings are as follows:

19.44 MHz input on CKIN1
CKIN2 is not used because of free run mode
155.52 MHz output on CKOUT1
622.08 MHz output on CKOUT2
Loop BW of 70 Hz (Si5325/26-EVB)
Loop BW of 7 Hz (Si5324-EVB)
LVEPCL outputs for CKOUT1 and CKOUT2

For the Si5322/23-EVB, the factory jumper settings are as follows:

Pin	Jumper	Comment
AUTOSEL	H	automatic, revertive
—	none	
FRQSEL0	none	FRQSEL = LMLM
FRQSEL1	L	19.44 MHz input
FRQSEL2	none	155.52 MHz output
FRQSEL3	L	
BWSEL0	H	BW is 96 Hz, the minimum
BWSEL1	H	
CS_CA	none	CS_CA is an output, not an input
FRQTBL	L	SONET frequency table
—	none	
SFOUT0	H	PECL outputs
SFOUT1	none	
RATE0	none	114.285 MHz ref xtal
RATE1	none	
DBL_BY	L	CKOUT2 enabled
—	none	
INC	none	
DEC	none	
—	none	

For the Si5319-EVB, the power up settings are as follows:
Free run mode, based on the 114.285 MHz crystal
19.44 MHz on CKOUT
Loop BW of 110 Hz
LVEPCL output for CKOUT

For the Si5316-EVB, the factory jumper settings are as follows:

pin	jumper	comment
—	none	
—	none	
FRQSEL0	L	FRQSEL = LL
FRQSEL1	L	19.44 MHz input/output
CK1DIV	L	div by 1
CK2DIV	L	div by 1
BWSEL0	H	BW is 100 Hz, the minimum
BWSEL1	H	
CS	L	select CKIN1
—	none	
—	none	
SFOUT0	H	PECL output
SFOUT1	none	
RATE0	none	114.285 MHz ref xtal
RATE1	none	
DBL_BY	L	CKOUT enabled
—	none	
—	none	
—	none	

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Added Si5319-EVB.
- Add "Appendix—Powerup and Factory Default Settings" on page 23.

Revision 0.2 to Revision 0.3

- Updated for free run mode.

Revision 0.3 to Revision 0.4

- Added Si5324-EVB

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