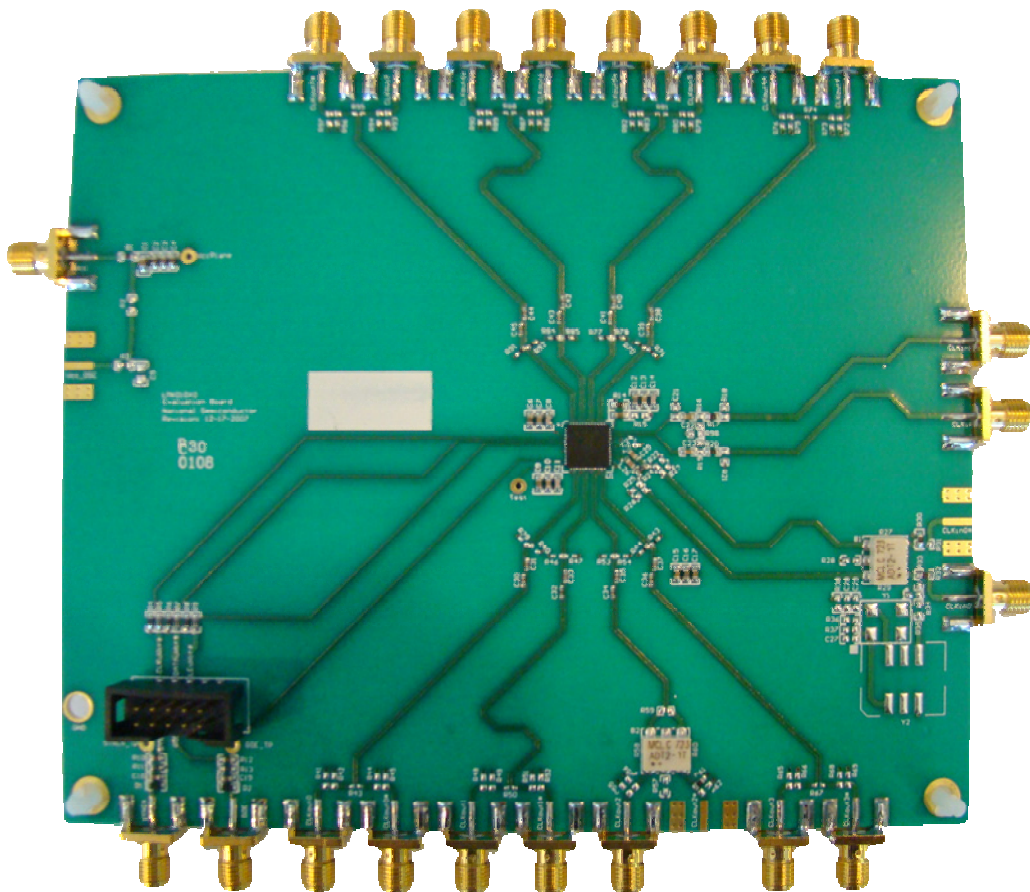




LMK01000
Precision Clock Conditioner
Evaluation Board Operating Instructions

2-20-2008

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General Description

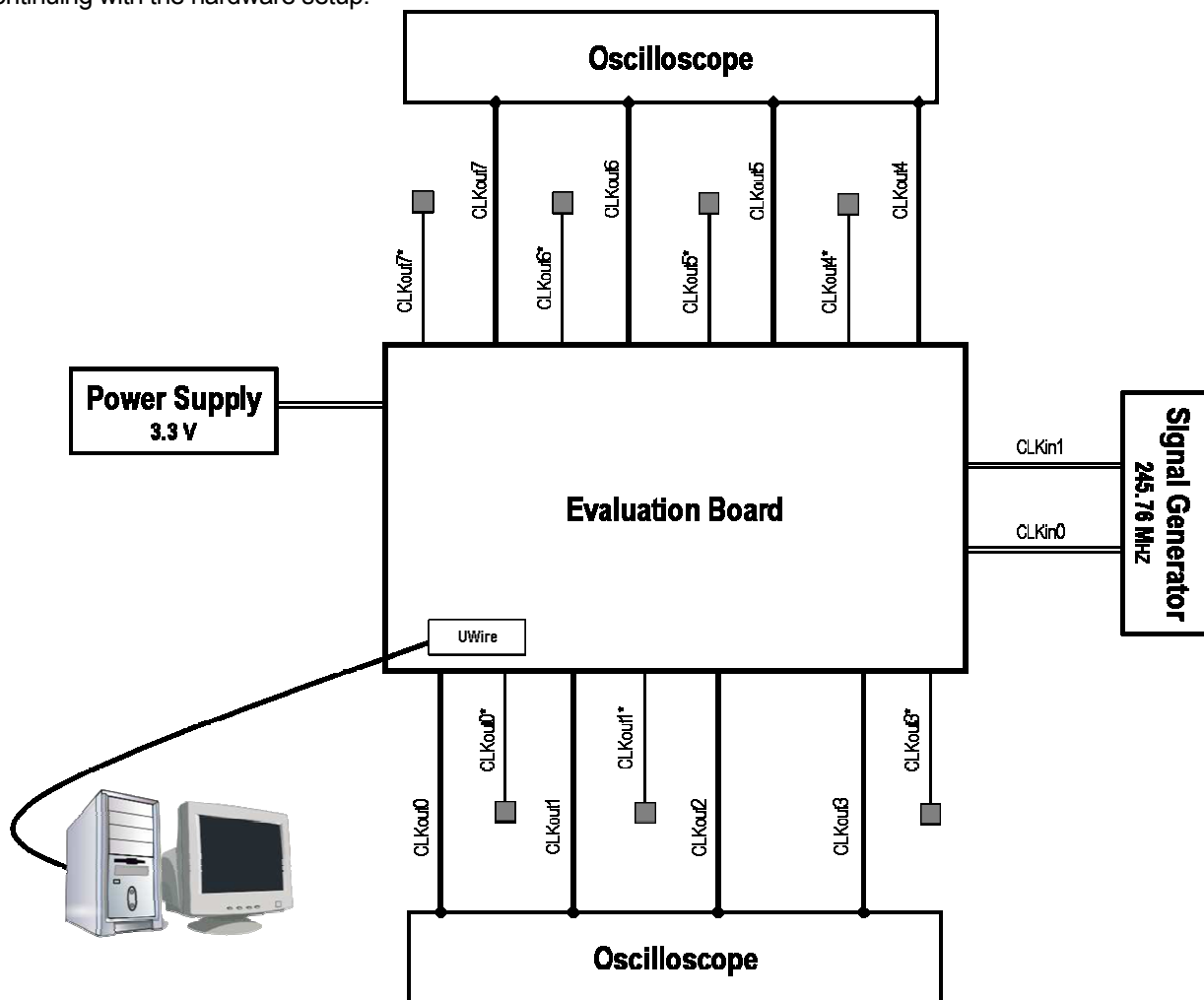
The LMK01000 Evaluation Board package simplifies evaluation of the LMK01000 Precision Clock Conditioner. Contents:

- Evaluation board
- LPT to 10 pin uWire cable
- *CodeLoader* software

The *CodeLoader* software will run on a Windows 2000 or Windows XP PC. The purpose of the *CodeLoader* software is to program the internal registers of the LMK01000 device through a MICROWIRE™ interface.

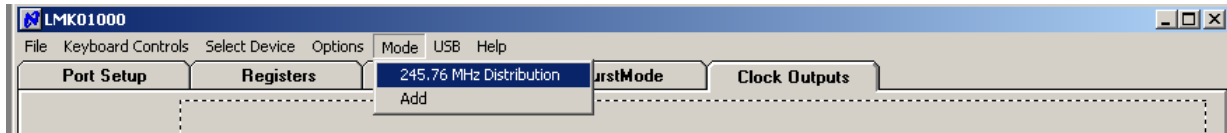
Basic Operation

To prepare the computer for use with the evaluation board, first install the *CodeLoader4* software. Reference the document, “*Installing CodeLoader 4*” and “*Installing USB Driver*” as needed to assist in this task before continuing with the hardware setup.



- 1) Connect a low noise **3.3 V** power supply to the **Vcc** connector located at the top left of the board
- 2) Connect the uWire cable to the **uWire** header located in the lower left.
- 3) Connect a suitable signal generator to one of the CLKin connectors on the right side of the board. One could also use an LVPECL or LVDS output to drive CLKin1. Be sure to indicate which clock is being used for the input on CodeLoader using the CLKin_SELECT bit on the bits/pins tab.

- 4) Connect...
- PC directly to the evaluation board with the LPT to 10 pin uWire cable, plugging the cable into an LPT port on the computer. This setup is shown below. **The cable can be removed after programming to minimize noise and EMI.**
 - Or
 - Available separately, upon request, the USB <--> uWire board can be connected to the PC with a USB cable. The board provides a 10 pin ribbon cable to connect to the uWire header on the evaluation board as done in step 1b (instead of the LPT to 10 pin uWire cable).
- 5) Select the default mode by clicking "**Mode**" → "245.76 MHz OSCin"

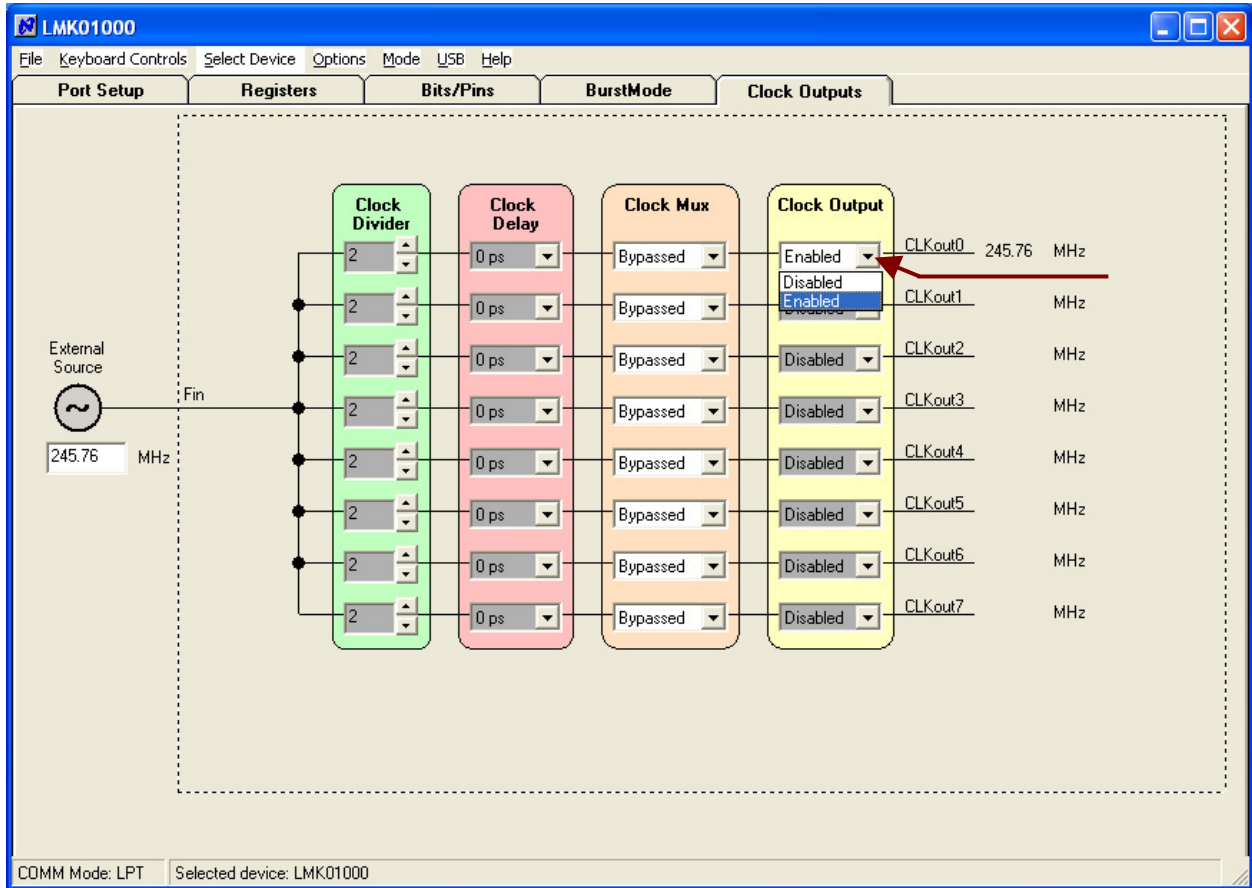


- 6) Load the part with CodeLoader. Communication with the part can be verified by enabling and disabling POWERDOWN bit on CodeLoader and observing a change in the current. If the current does not change, ensure that the port setup is correct. (See PORT SETUP section for further debugging information) Some common debugging tips are shown below:

LPT Mode	USB Mode
Ensure that CodeLoader is set to LPT mode in the Port Setup Tab	Ensure that CodeLoader is set to USB mode in the Port Setup Tab
Ensure that the proper port (LPT1, LPT2, or LPT3) is selected. CodeLoader does not auto detect the proper port.	Ensure that the green light is <u>on</u> for the USB board.
Ensure that some signal is actually coming from the part. If no signal is coming, then this indicates a windows issue – common windows issues with the parallel port include: the user needs to have administrative rights and the selected mode can sometimes make a difference.	Ensure that CodeLoader is properly communicating with the USB board. Note that communication to the USB board does not guarantee communication with the part. Also, try USB->Version from the menu. A version description should be displayed. If not, then the computer is not communicating with the USB board.

Basic Operation (continued)

- 7) **Select (ENABLE) output to measure**, any of CLKout (0-7) or EN_CLK from either Clock Outputs or Bits/Pins tabs. For default mode, all outputs are disabled.



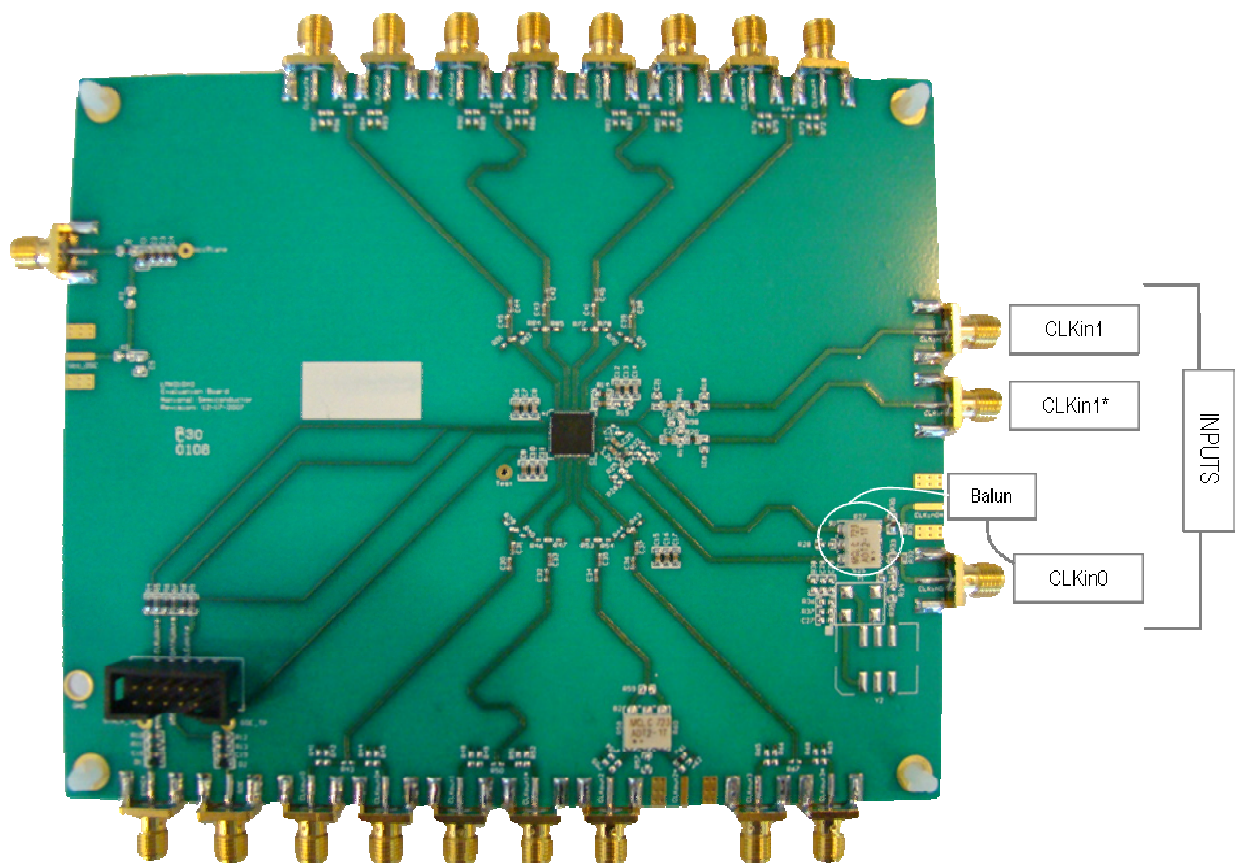
- 8) **Program the LMK01000 evaluation board** by clicking “Keyboard Controls” → “Load Device”, or by pressing **Ctrl+L**.
- 9) Make and record measurements. After programming, the **uWire cable can be unplugged from the evaluation board to minimize noise and EMI**.

Board Information

CLKin Inputs

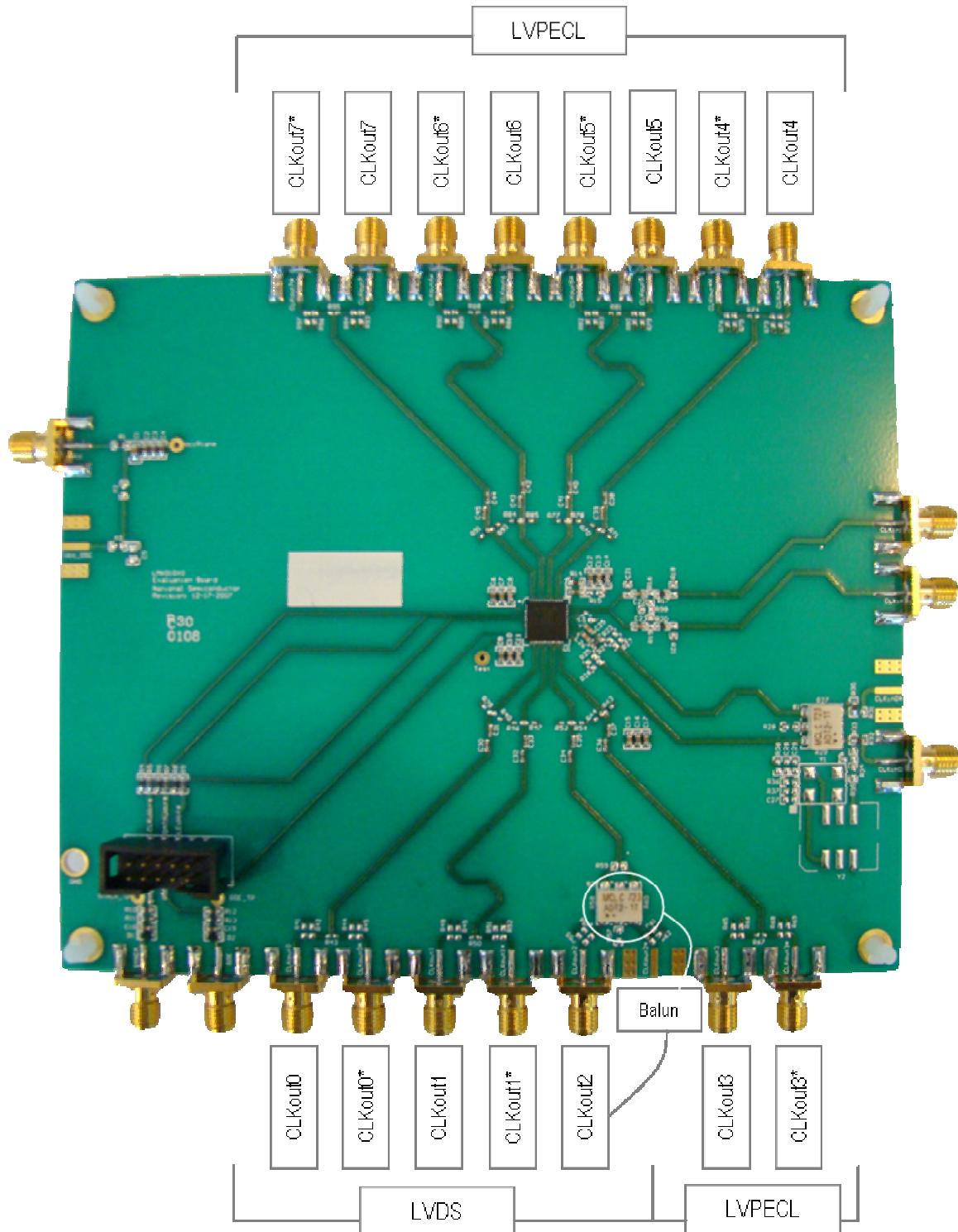
CLKin0 is one of two inputs that can be used to drive the LMK01000. Although this input is rated to higher frequencies, the balun on the board is only rated to 400 MHz. Ensure CLKin_SELECT is set to CLKin0 when using this input. If a higher frequency is required, above 400 MHz, then use CLKin1.

CLKin1 is very similar to CLKin0. If this input is driven single-ended, it is preferred to shunt CLKin1* to ground with a capacitor, but this capacitor is not placed on the board. CLKin1 is currently configured to be fed by a differential output, such as the output of the LMK03000C. Ensure that CLKin_SELECT is set to CLKin1 when using this input.



CLKout Outputs

CLKout0 to CLKout2 are LVDS outputs. For CLKout2, there is a balun attached, so it can be attached to single-ended test equipment. Although the output is rated to higher frequencies, the balun is only rated to 400 MHz. CLKout3 to CLKout7 are LVPECL outputs and all are configured the same.

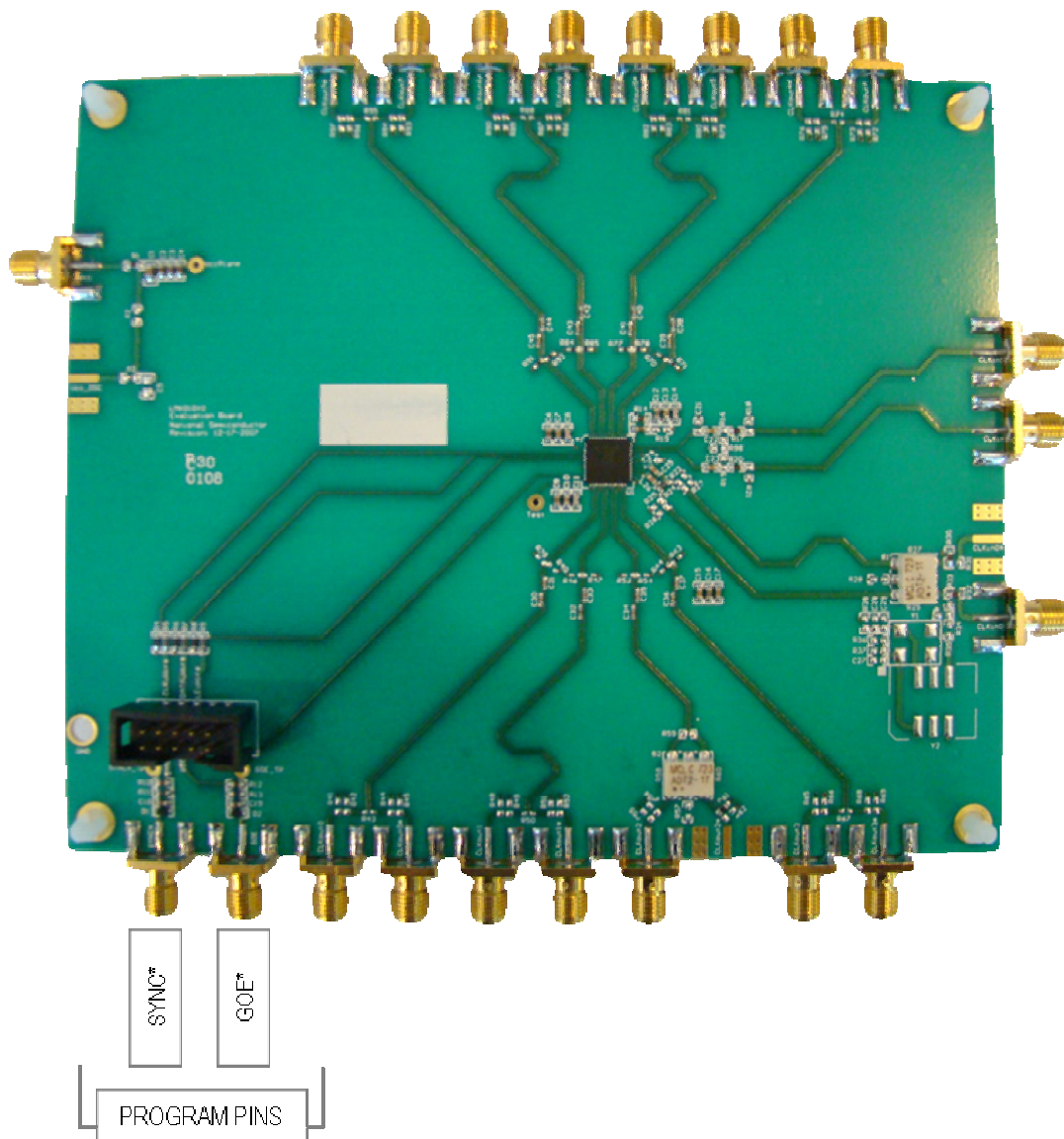


SYNC*

This input connects to the SYNC* pin that can be used to synchronize the outputs in the event that they are dividing the input signal (divided mode). For bypass mode, this is not necessary. For the LMK01000 to run, this has to be set to high logic level. On the board, there is a diode and pull up resistor such that if the CodeLoader cable is taken away, the pull-up will pull this high, but if the CodeLoader cable is attached, then this will override the pull-up resistor.

GOE*

This connector connects to the GOE pin on the chip, which needs to be set to high logic level to have all the outputs running. On the board, there is a diode and pull up resistor such that if the CodeLoader cable is taken away, the pull-up will pull this high, but if the CodeLoader cable is attached, then this will override the pull-up resistor.



Recommended Equipment

Power Supply

The Power Supply should be a low noise power supply. An Agilent 6623A Triple power supply with external LC filters or an HP E3610A with external LC filters was used in creating these evaluation board instructions. The LC filters on the outputs help to reduce noise from the power supplies.

Oscilloscope

An Agilent Infiniium DSO81204A was used.

Signal Generator

A signal generator can be used to drive either the CLKin0 or CLKin1 pin. If phase noise is measured, consider the signal generator noise, since it tends to dominate. CLKin1 can also be driven from an LVDS or LVPECL clock output, such as one from the LMK03000C evaluation board.

Noise Floor Measurements

Reason and Methodology

When measuring output noise, consideration should be taken to note the inherent noise of the input source in order to accurately reflect the performance of the LMK01000. The measured output noise consists of the output noise of the LMK01000 - plus the inherent noise of the signal generator, or reference signal input, chosen. To determine the actual noise floor of the device, the input noise must be measured, or interpolated. The charts referenced below were compiled with measurements from an Agilent E5052A Signal Source Analyzer.

This methodology can be visualized in the following formula expressions:

Measured Noise

$$10^{(MeasuredNoise/10)} = 10^{(DeviceNoise/10)} + 10^{(SigGenNoise/10)}$$

The above expression can be solved for *DeviceNoise* as follows:

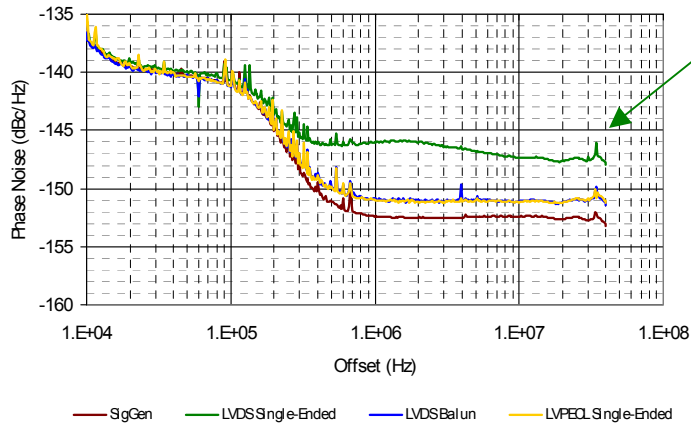
$$DeviceNoise = 10 \cdot \log\left(10^{MeasuredNoise/10} - 10^{SigGenNoise/10}\right)$$

Three (3) samples are depicted to help further explain this methodology:

- Raw Data chart – depicting an input of 245.76 MHz with no internal dividers affecting output (See Chart #1)
- Smoothed Data chart – Raw data “smoothed” to help remove extraneous noise from the graphical representation. (See Chart #2)
- Corrected Data chart – depicts an input of 245.76 MHz with no internal dividers affecting output. Input noise (as measured above in the Raw data chart) removed and calculated actual noise floor of device and outputs shown. (See Chart #3)

Charts

245.76 MHz Input – Actual Measurements



LVDS—elevated dBc measurements— not intended for single-ended performance.

Chart #1

245.76 MHz Input – Smoothed Measurements

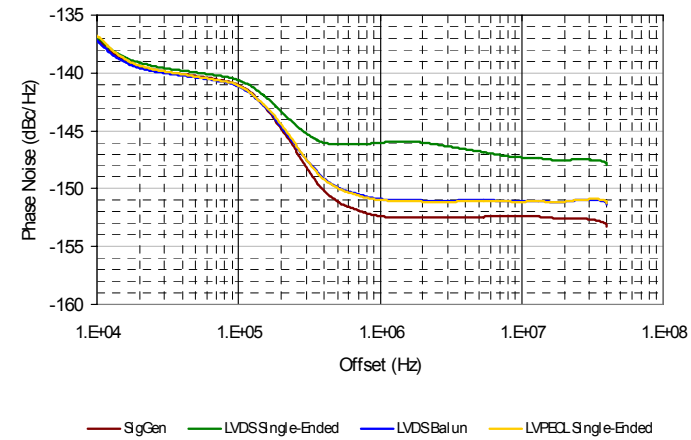


Chart #2

245.76 MHz Input – Corrected Measurements (SigGen Input Removed)

This calculation is sensitive, especially visible, when measured noise data is close to the signal generator noise.

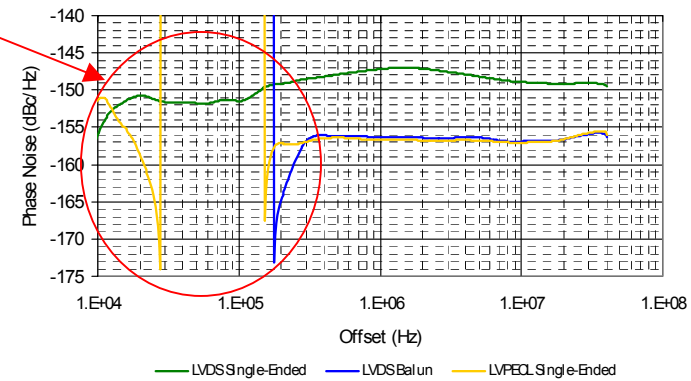
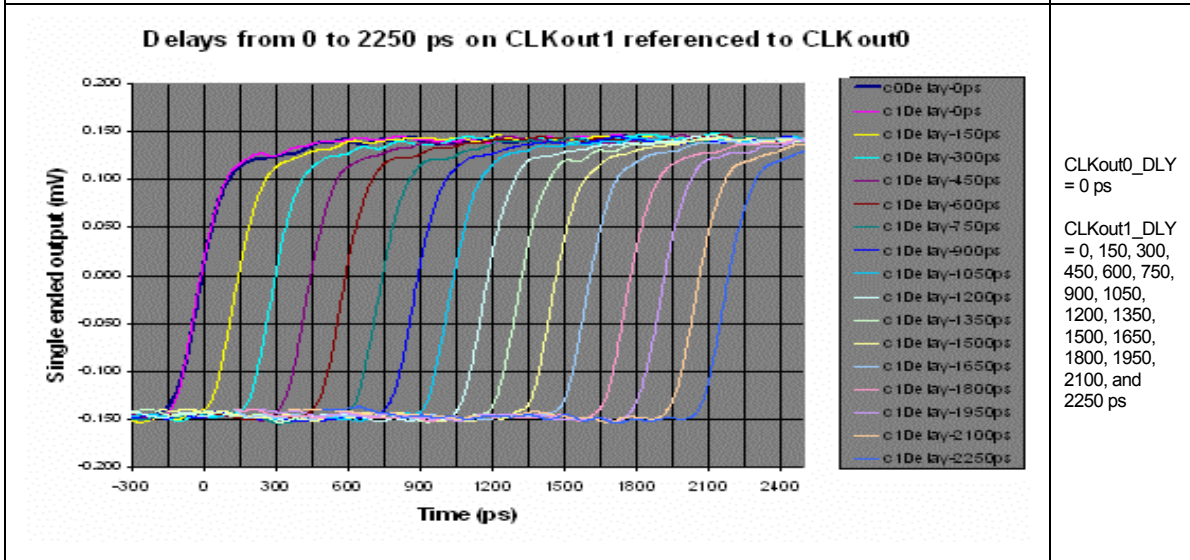


Chart #3

Delay Measurements

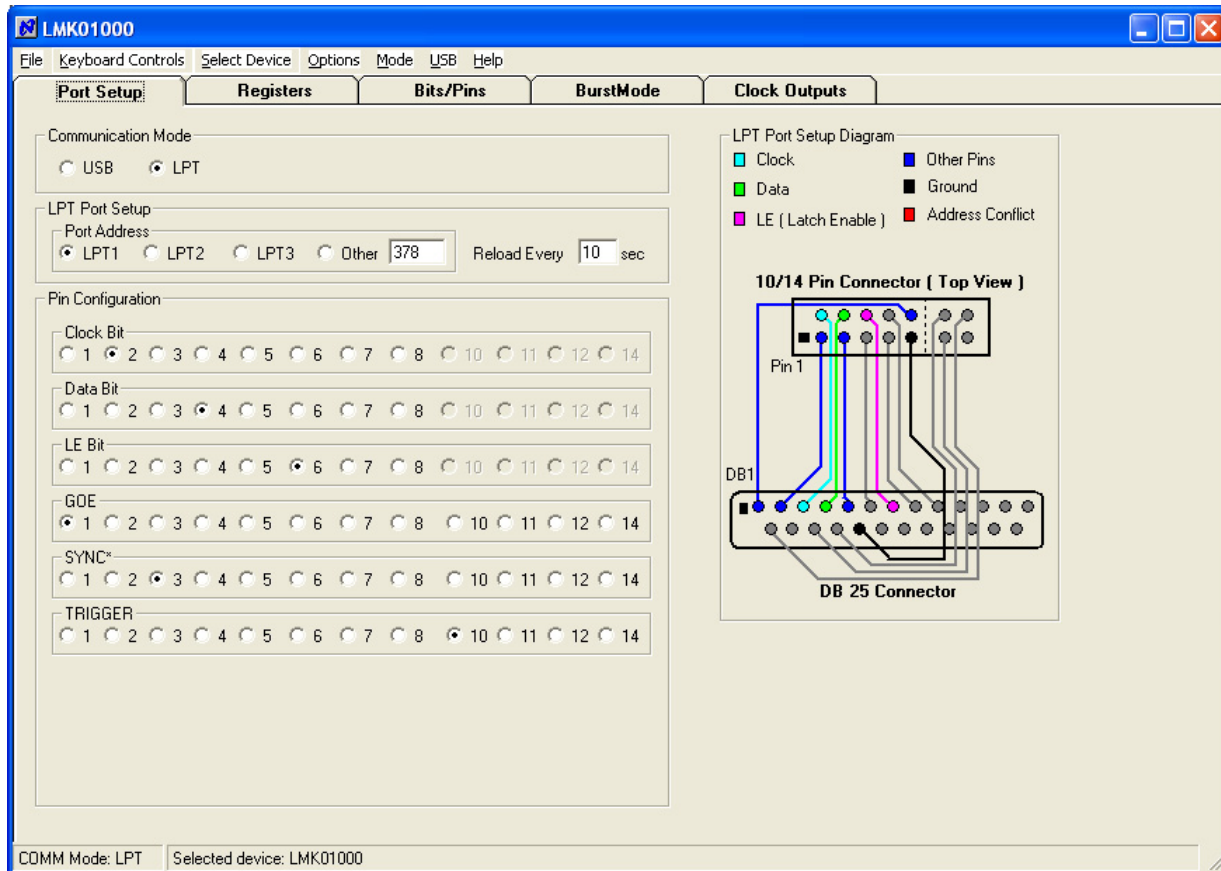


Delays 150, 300, 450, 600, 750 ps



CLKout0_DLY = 0 ps
 CLKout1_DLY = 0, 150, 300, 450, 600, 750, 900, 1050, 1200, 1350, 1500, 1650, 1800, 1950, 2100, and 2250 ps

Port Setup and Debugging Communication Issues



Debugging Communication Issues

1. Ensure that the correct mode of USB or LPT is selected.
2. Ensure that the port setup is correct
3. Ensure that the cable is properly hooked to the board such that it dangles off the edge of the board, as opposed to across the board.
4. Click the POWERDOWN bit on the Bits/Pins page and press Ctrl+L and observe the current the board draws. Now unclick the POWERDOWN bit and observe the current. If you can change the current in this way, then communication is working.

Debugging LPT Communication Issues

1. Ensure that the proper port is selected. CodeLoader does not auto detect this.
2. You need administrative rights on the machine to write to the parallel port.
3. After installing CodeLoader, restart the machine to ensure that the parallel port drivers are installed correctly.
4. For windows settings, make sure that the port is enabled. Sometimes, there is a windows setting called AUTO, which causes issues with CodeLoader if this port is shared by a printer.

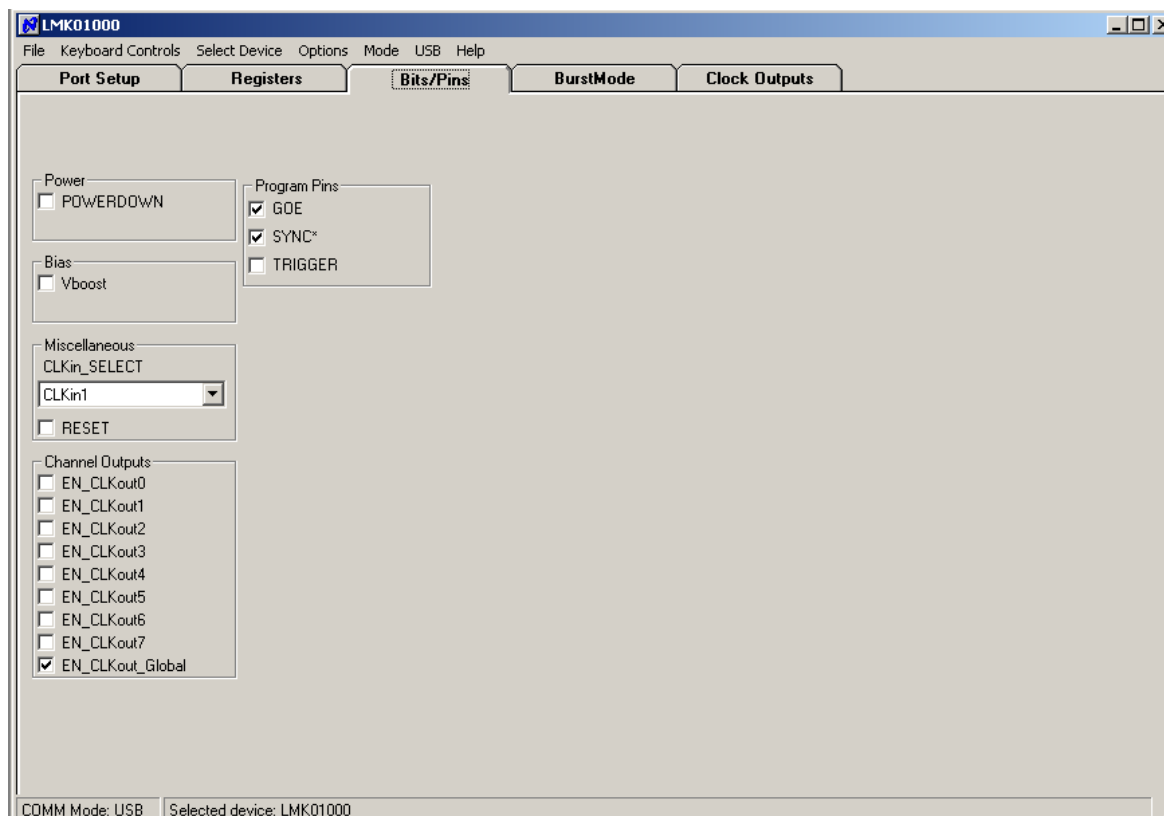
Debugging USB Communication Issues

1. Ensure that the green light is on for the USB board.
2. Try USB->Version to get the USB version ID. If it comes back blank, then CodeLoader is not communicating properly with the USB board.
3. This should not be necessary, but if somehow the USB driver is not installed properly, unplug the USB board, uninstall it from the device manager, then plug it back in.

Bits/Pins Tab

The Bits/Pins tab shows some of the internal registers, which are not accessible from any of the other visual tabs like “Clock Outputs”.

Right-click on any of the bits to view a description.



Program Bits	
POWERDOWN	Powers the part down.
RESET	The registers can be defaulted by checking and un-checking RESET. Software bits will not reflect this.
Vboost	Enabling this bit increases the voltage level of these outputs and often improves the noise floor of the outputs. However, enabling this bit will cause the voltage levels to be too high for LVPECL/LVDS standards at low frequencies.
EN_CLKout0-7	Enable CLKout bits from CLKout0 to CLKout7. Also accessible from Clock Outputs tab.
EN_CLKout_Global	Enable all clock outs. If unselected then the EN_CLKouts are overridden and the outputs are all disabled.

Program Pins	
GOE*	Set Global Output Enable to high or low logic level. GOE is not used. See Board Information section for usage of this pin.
SYNC*	Set SYNC* pin to high or low logic level.
TRIGGER	Set auxiliary trigger pin to high or low logic level.

Clock Outputs Tab

The Clock Outputs tab allows the user to visualize the clock distribution portions of the device. From this tab the device's dividers, delays, clock output muxes, and output drivers can be programmed. Remember to enable an output to observe it.

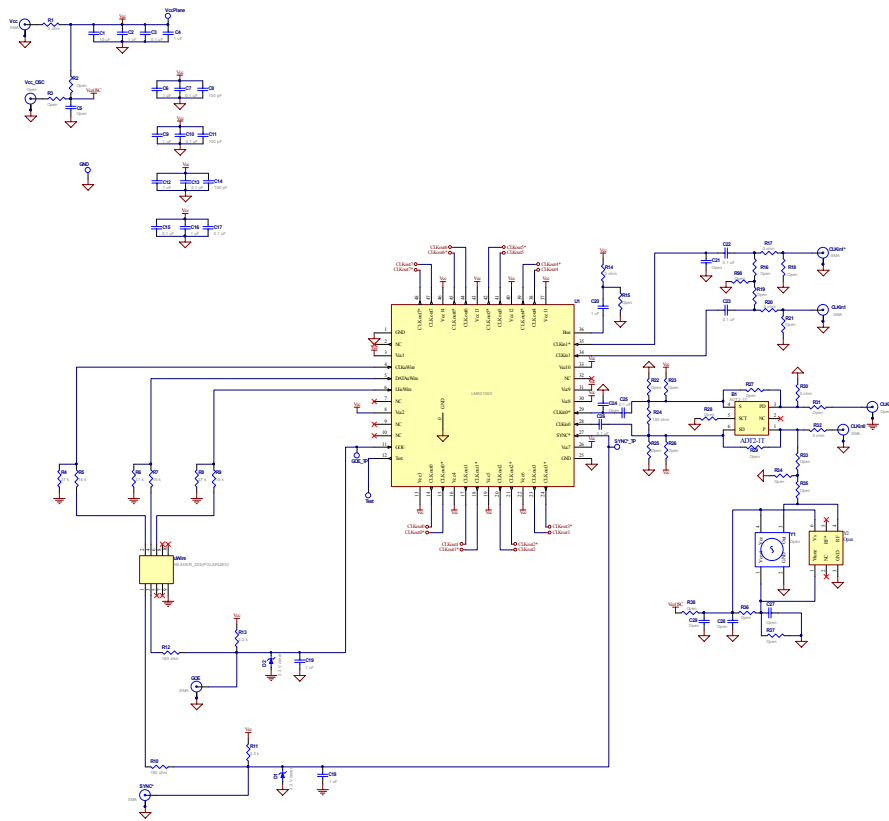
Note: the enables on this page are linked directly to the EN_CLKoutX on the Bits/Pins tab.

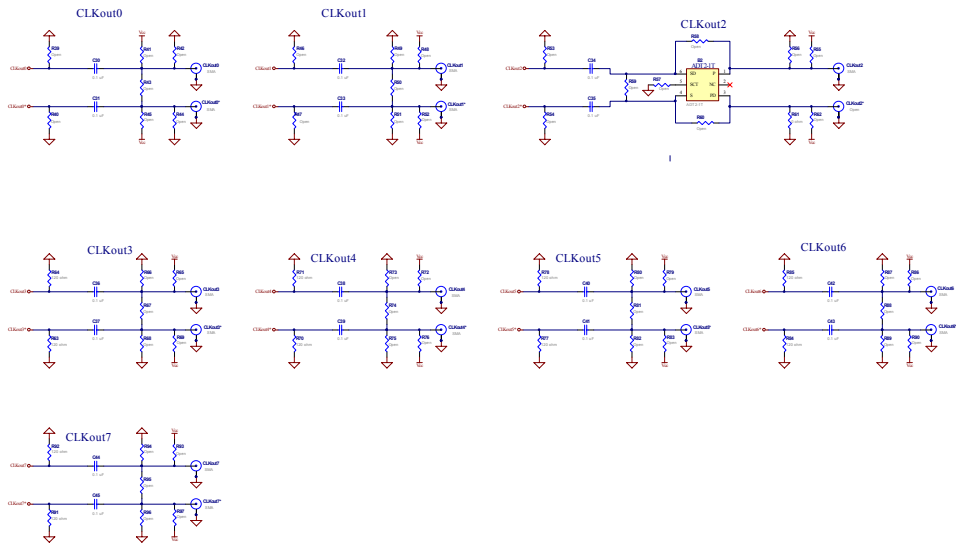
The screenshot displays the LMK01000 software interface with the 'Clock Outputs' tab selected. The interface shows an external source of 245.76 MHz connected to the 'Fin' input. The configuration is as follows:

Output	Divisor	Delay (ps)	Mux	Enabled	Frequency (MHz)
CLKout0	2	0	Bypassed	Disabled	
CLKout1	2	0	Bypassed	Disabled	
CLKout2	2	0	Bypassed	Disabled	
CLKout3	2	0	Bypassed	Enabled	245.76
CLKout4	2	0	Bypassed	Disabled	
CLKout5	2	0	Bypassed	Disabled	
CLKout6	2	0	Bypassed	Disabled	
CLKout7	2	0	Bypassed	Disabled	

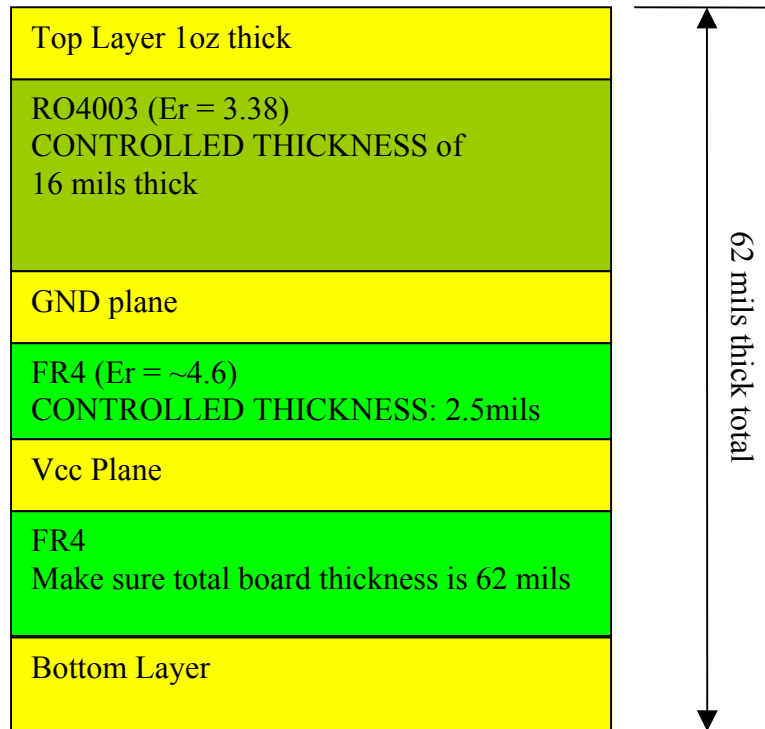
At the bottom of the window, it shows 'COMMM Mode: LPT' and 'Selected device: LMK01000'.

Appendix A: Schematic





Appendix B: Layer Stack up Information



Appendix C: Bill of Materials

Date	12/14/2007					
Item	Type	Part	Manufacturer	Part Number	Qty	Identifier
0	Open	Open Capacitors	n/a	n/a	6	C5,C21, C24,C27-C29
		Open Resistors	n/a	n/a	60	R2,R3, R15,R16,R18,R19,R21-R23,R25-R29,R31, R33 -R60, R62,R65 - R69, R72 - R76, R79 - R83, R86 - R90, R93 - R98
		Open Other	n/a	n/a	5	Y1,Y2,Vcc_OSC,CLKin0*,CLKout2*
1	Capacitors	100 pF	Kemet	C0603C101J5GAC	3	C8, C11, C14
2		0.1 uF	Kemet	C0603C104J3RAC	10	C3, C7, C10, C13, C15, C17, C22, C23,C25, C26
3		0.1 uF	Kemet	C0402C104J4RAC	16	C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45
4		1 uF	Kemet	C0603C105K8VAC	9	C2, C4, C6, C9, C12, C16, C18, C19, C20
5		10 uF	Kemet	C0805C106K9PAC	1	C1
6	Resistors	0 ohm	Vishay	CRCW0603000ZRT1	7	R1, R14, R17, R20, R30, R32, R61
8		100 ohm	Vishay/Dale	CRCW0603101JRT1	1	R24
9		120 ohm	Vishay	CRCW0402120RJNED	10	R63, R64, R70, R71, R77, R78, R84, R85, R91, R92
10		180 ohm	Vishay	CRCW0603181JRT1	2	R10, R12
11		2.2 k	Vishay/Dale	CRCW06032K20JNEA	2	R11, R13
12		15 k	Vishay	CRCW0603153JRT1	3	R5, R7, R9
13		27 k	Vishay	CRCW0603273JRT1	3	R4, R6, R8
14	Other	ADT2-1T	Minicircuits	ADT2-1T	2	B1, B2
15		HEADER_2X5(POLARIZED)	FCI Electronics	52601-S10-8	1	uWire
16		SMA	Johnson Components	142-0701-851	21	Vcc,CLKin0,CLKin1,CLKin1*,CLKout0, CLKout0*, CLKout1,CLKout1*,CLKout2, CLKout3,CLKout3*, CLKout4, CLKout4*,CLKout5,CLKout5*,CLKout6,CLKout6*, CLKout7, CLKout7*,GOE,SYNC*
17		LMK010X0 PCB	National Semiconductor	LMK010X0EVPCB	1	n/a
18		0.375" Stand-Offs	SPC Technology	SPCS-6	4	Place in 4 corner holes of the board
19		Clock Conditioner	National Semiconductor	LMK01000	1	U1
20		3.3 V zener	Comchip	CZRU52C3V3	2	D1, D2