# FPD-Link II Display SerDes Overview

National Semiconductor
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## Introduction

National's FPD-Link II family of embedded clock LVDS SerDes provide enhanced features, and improved signal quality over prior generations of FPD-Link SerDes devices for Display applications. FPD-Link Chipsets serialized the wide parallel RGB buses down to 4 or 5 pairs of LVDS signaling depending upon the chipset. 18-bit RGB was serialized to three LVDS data lines and a LVDS clock, while 24-bit RGB was serialized to four LVDS data lines and a LVDS clock. This provided a smaller, higher speed video bus and has become the defacto standard for Notebook Display interfaces.

The FPD-Link II SerDes family serializes the wide parallel display bus all the way to a single serial differential signal as shown in *Figure 1* below. Signal compression ratios of 24:1 or even greater (if ground wires are taken into account) are obtained. Current devices in the family support common 18-bit and 24-bit RGB Display applications. With the single serial signal, skew problems between multiple lines (lanes) are removed and cable lengths up to 10 meters are supported. This makes the FPD-Link II SerDes ideal for long reach applications with low cost small cables.

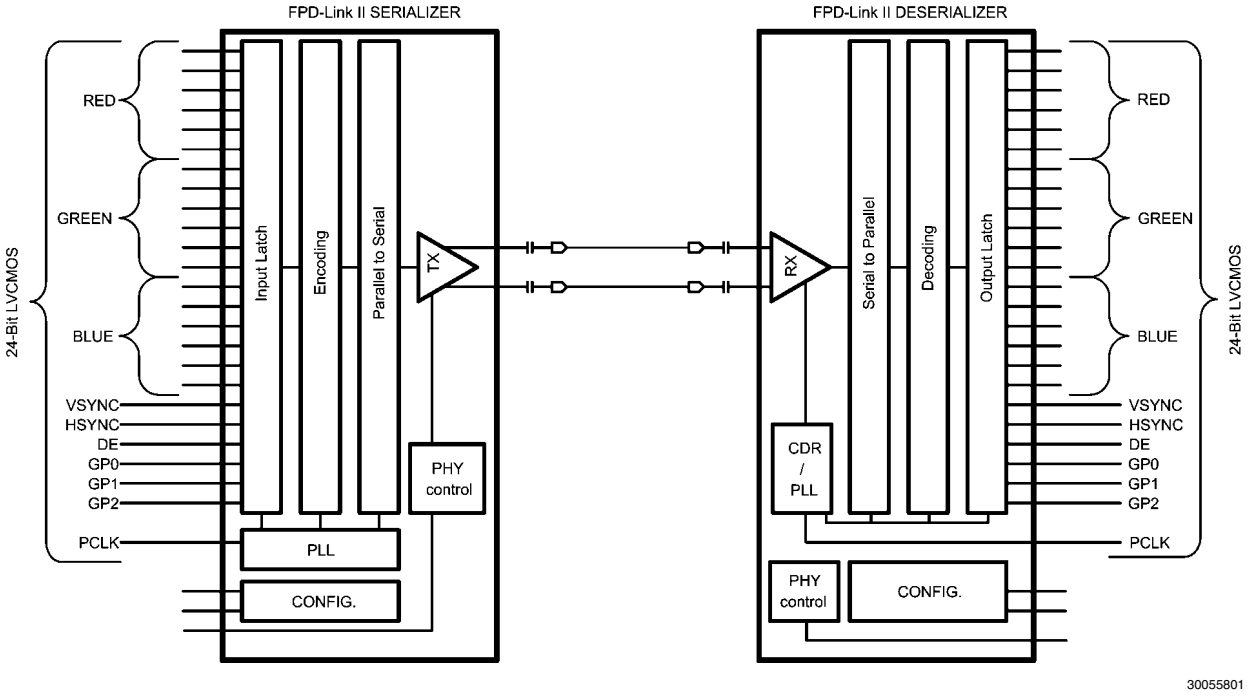


**FIGURE 1. General Block Diagram – FPD-Link II 18-bit RGB Display Application**

The single serial differential signal carries the parallel data (RGB and control) information, clock information and a small amount of serial overhead. Routing of the single signal pair greatly eases system design, saves bulk interconnect, saves connector pins, and reduces concern over interface interconnect skew.





 

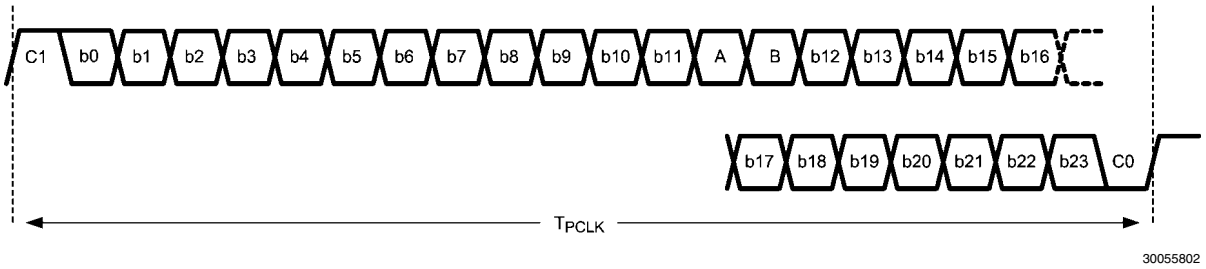


**FIGURE 2. 24-bit Serial Payload Example**

An example of the 24-bit (user) payload is shown in *Figure 2*. The 24-bit data field is appended with four additional serial bits which provide the embedded clock information, link coding, and operating mode information. A fixed clock edge is created between the C0 and C1 bits, and the coding/mode information is conveyed by the A & B bits.

## The SERIALIZER Function

The Serializer (SER) function generically collects a wide parallel bus plus its clock signal, performs payload optimization, appends the serial control bits and level translates the high-speed serial signal to LVDS-like levels. The payload is optimized for serial transmission over AC-coupled interconnects. This step balances the data being sent to support the AC-coupled transmission. Depending upon the chipset being used, payload randomization and scrambling is also done to enhance the signal quality across the link.

A few options are also supported depending upon the SER device. Various input (parallel) buses are supported. This ranges from bus width and also signaling physical layer. LVCMOS buses at 3.3V are supported, with optional 1.8V support on some products. In addition, serializers with FPD-Link (LVDS based) inputs convert to FPD-Link II (i.e. DS99R421 and DS90UR907).

## The DESERIALIZER Function

The Deserializer (DES) function is to recover the clock and data signals and to provide them to the target device (a display for example). The FPD-Link II DES is very unique as it is able to quickly lock to the serial stream without the need of a local reference clock or any special training patterns from the SER. These features set the FPD-Link II SerDes apart from many competing interfaces. They simplify the application, support hot plugging, and also require less external components (less board space and cost). The DES even provides a LOCK output signal to allow the system to check serial link status.

A few options are also supported depending upon the DES device selected. Various output (parallel) buses are supported. This ranges from bus width and also the signaling physical layer. LVCMOS buses at 3.3V are supported, with optional 1.8V support on some products. In addition, deserializers are available with FPD-Link (LVDS based) outputs (i.e. DS90UR908).

## Serial Payload

The serial payload is optimized for the different chipsets in the FPD-Link II family and also for the applications they support. A common serial payload to explain as a reference is the 28-bit serial frame shown in *Figure 2* above. The 28 bits are comprised of: 24 data bits, 2 bits of embedded clock information, and 2 bits of serial control for the link. Thus, for every 24 bits of data, 28 serial bits are sent. This makes the basic link 24/28 (86%) efficient. This is an important bench mark, as it is always desirable to keep overhead low. This scheme is also ~30% better than the common data communication 8b/10b scheme which is 80% efficient. Note that the 24 data bits are modified by the balancing, randomization, and scrambling. This is done to support the AC coupling on the link, and also to help reduce ISI (Inter-symbol Interference) effects when sending relatively static data. The two clock bits are fixed, with one bit high (C1) and one bit low (C0) – note these two are DC balanced as a pair. The two serial control bits, commonly noted as DCA (A) and DCB (B), provide information to the DES to recover the data and also the link status and mode. Chipsets supporting 24-bit RGB encode the status of video synchronization signals in the serial stream.

## Streaming RGB Display Applications

The FPD-Link II chipset is mainly used for RGB applications with various display resolutions. With the basic chipset (DS90UR241/124), 18-bit color depth is commonly used. A wide range of PCLK rates are supported depending upon the chipset selected. Of the user data payload, i.e. the 24 data bits, 18 bits of RGB information, 3 display control signals (HS, VS, DE) and 3 general purpose signals are sent per PCLK.

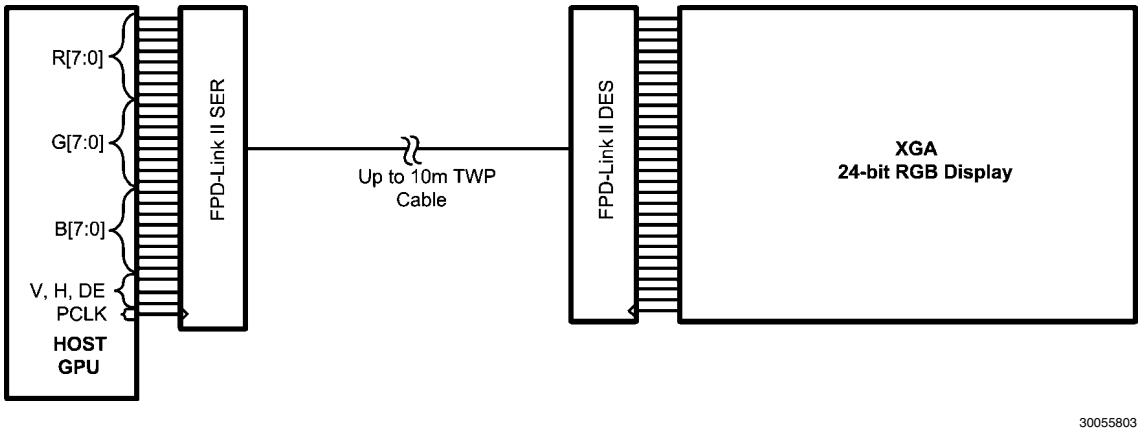


**FIGURE 3. 24-bit RGB FPD-Link II SERDES XGA Display Application**

In this example, if the PCLK was at 43MHz, the serial transmission rate is 28 times the PCLK, or 1.2 Gbps. The user data rate is 24X of PCLK, or 1.0 Gbps in this example.

## Signal Quality Enhancers

As noted above, the data payload is modified to randomize, scramble, and balance the data to support AC-coupling of the interface and to also enhance the signal quality of the serial signal. In addition to these, the physical layer is also enhanced and allows for various options depending upon the chipset.

Certain FPD-Link II line drivers feature an adjustable Pre-Emphasis feature. This is useful with longer distance applications or with high-loss interconnects. A resistor is connected to the PRE pin to ground and the value sets the amount of additional output current that is driven. If the following logic bit is the same logic state, the “additional” current is turned off for the following bit. With this scheme, ISI (jitter) is reduced and also some power is saved.

Other FPD-Link II line drivers provide De-Emphasis. Similar to Pre-Emphasis, this feature is adjustable via an external resistor. A serial control bus provides another means to adjust a programmable register setting. De-Emphasis reduces the differential output swing after the initial data transition, thus minimizing ISI.

Certain FPD-Link II line drivers also support a differential output voltage magnitude select pin. This pin is typically set to low for standard swings. But if a larger VOD is desired, the pin allows for an increased swing setting by setting it High.

Cable equalization is provided by some FPD-Link II receivers. This feature compensates for cable loss. Adjustment is made via pin control or serial bus controlled registers.

## EMI Mitigation Features

The differential LVDS style physical layer is used to help minimize the generation of EMI. Line driver transition times are controlled to be balanced and centered. This is done to minimize any common-mode currents from the line driver. The odd-mode (differential) signaling generates equal and opposite currents in the pair which also help to lower overall emissions. The serial link is terminated at both the source and load ends to minimize any signal reflections. Certain parts provide internal terminations to reduce external part count and to also minimize the resulting stub lengths.

The Parallel Bus at the DES (receiver output) is also optimized to reduce EMI. Edge rates are controlled, and on certain DES devices an output drive strength control is provided. Most DES devices support PTO (progressive turn-on), a feature that groups the data outputs into banks and offsets the switching point in time to reduce simultaneous switching and thus reduce supply noise. Other devices employ frequency spread PTO to dynamically alter the output switching sequence and further enhance the noise reduction of the wide bus. Spread spectrum clock generation is provided by some deserializers. This feature modulates the output clock and data period to effectively spread the energy associated with periodic output transitions and minimize emissions.

## Current FPD-Link II SerDes Devices

Many variants of FPD-Link II SER and DES devices are currently available with more to follow.

**TABLE 1. Select FPD-Link II SER and DES Device Comparison Table**

| NSID (root) | Function | Color Depth (bits per pixel) | General Purpose I/O | Parallel Interface | PCLK (MHz) |
|---|---|---|---|---|---|
| DS90C241Q | SER | 18-bit | 3 | LVCMOS | 5 to 35 |
| DS90C124Q | DES | 18-bit | 3 | LVCMOS | 5 to 35 |
| DS90UR241Q | SER | 18-bit | 3 | LVCMOS | 5 to 43 |
| DS90UR124Q | DES | 18-bit | 3 | LVCMOS | 5 to 43 |
| DS99R421Q | SER | 18-bit | 3 | FPD-Link (3D + C LVDS) | 5 to 43 |
| DS90UR905Q | SER | 24-bit | N/A | LVCMOS | 5 to 65 |

| NSID (root) | Function | Color Depth (bits per pixel) | General Purpose I/O | Parallel Interface | PCLK (MHz) |
|---|---|---|---|---|---|
| DS90UR906Q | DES | 24-bit | N/A | LVCMOS | 5 to 65 |
| DS90UR907Q | SER | 24-bit | N/A | FPD-Link (4D + C LVDS) | 5 to 65 |
| DS90UR908Q | DES | 24-bit | N/A | FPD-Link (4D + C LVDS) | 5 to 65 |
| Check website for latest product introductions. | | | | | |

## Summary

The FPD-Link II SerDes devices provide an embedded clock single serial stream for Display, Imaging, Pixel based, and other applications. The serial interface greatly eases interconnect design in terms of space, pins, skew and cost. The FPD-Link II DES devices with the special clock recovery circuitry are unique in that they do not require training patterns, a local reference clock, and support hot-plugging into a live link.

# Notes

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| Switching Regulators | www.national.com/switchers | Distributors | www.national.com/contacts |
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