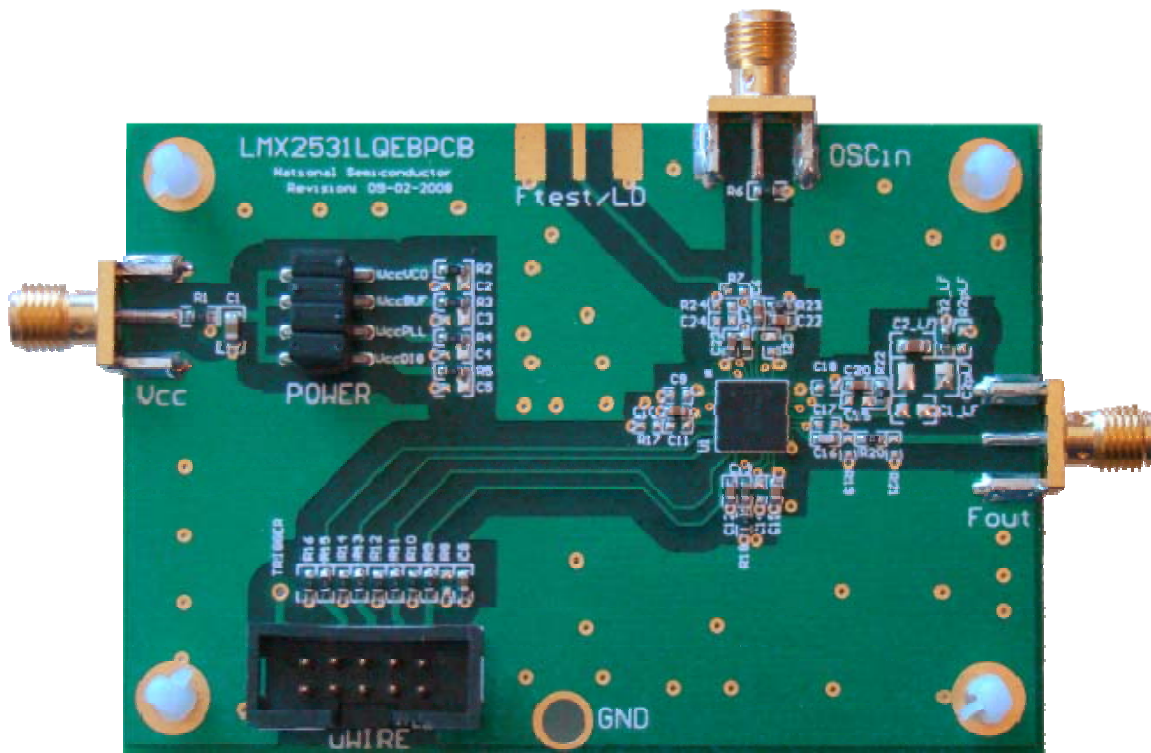


## **LMX2531LQ3010E**

### **Evaluation Board Operating Instructions**



**National Semiconductor Corporation**  
**Timing Devices Business Group**

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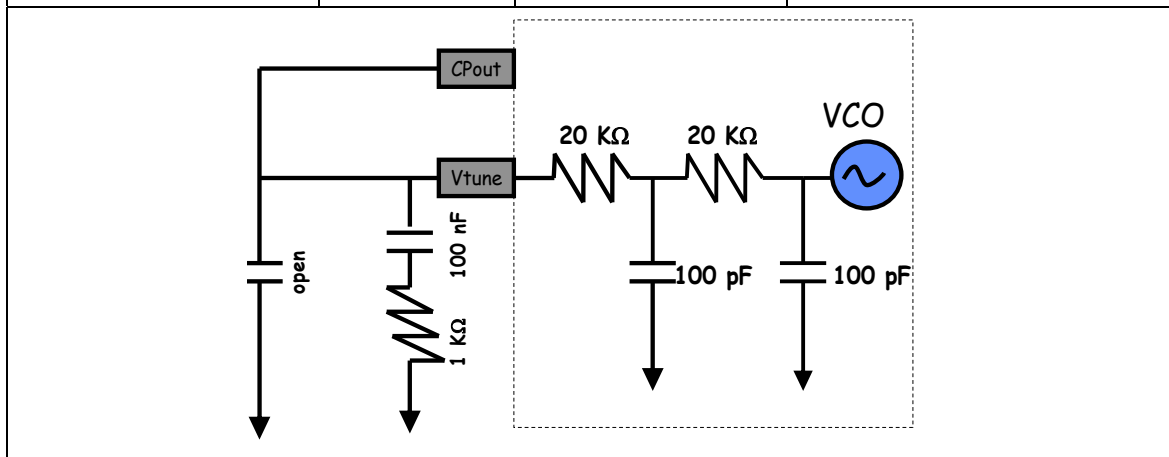
**LMX25313010EVAL Instructions Rev 6.24.2009**

## Table of Contents

Table of Contents .....	2
Loop Filter .....	3
Quick Setup.....	3
Troubleshooting .....	4
SOFTWARE DOES NOT COMMUNICATE WITH THE EVALUATION BOARDS .....	4
PART RESPONDS TO PROGRAMMING, BUT DOES NOT LOCK TO THE CORRECT FREQUENCY .....	4
CLOSE-IN PHASE NOISE IS WORSE THAN EVALUATION BOARD INSTRUCTIONS SHOW .....	4
FAR-OUT PHASE NOISE IS WORSE THAN EVALUATION BOARD INSTRUCTIONS SHOW .....	5
Device Data.....	5
PHASE NOISE .....	6
FREE-RUNNING VCO PHASE NOISE (INTERNAL DIVIDE BY 2 DISABLED).....	7
FREE-RUNNING VCO PHASE NOISE (INTERNAL DIVIDE BY 2 ENABLED).....	8
FRACTIONAL SPURS (INTERNAL DIVIDE BY 2 DISABLED) .....	9
FRACTIONAL SPURS (INTERNAL DIVIDE BY 2 ENABLED) .....	10
INTEGER SPURS (INTERNAL DIVIDE BY 2 DISABLED).....	11
INTEGER SPURS (INTERNAL DIVIDE BY 2 ENABLED).....	12
IN-BAND FACTIONAL SPURS INTEGER SPURS (INTERNAL DIVIDE BY 2 DISABLED).....	13
IN-BAND FACTIONAL SPURS INTEGER SPURS (INTERNAL DIVIDE BY 2 ENABLED).....	14
Inter-modulation Spurs .....	15
CodeLoader Settings.....	16
SELECT DEVICE.....	16
BITS/PINS.....	18
PLL/VCO .....	19
REGISTERS .....	20
PORT SETUP .....	21
Schematic .....	22
Bill of Materials .....	23
Top Layer.....	24
Mid Layer 1 "Ground Plane" .....	25
Mid Layer 2 "Power" .....	26
Bottom Layer "Signal" .....	27
Top Build Diagram .....	28

## Loop Filter

<b>Loop Bandwidth</b>	13.8 kHz	<b>K<math>\phi</math></b>	1440 $\mu$ A (16X)
<b>Phase Margin</b>	54.5 $^{\circ}$	<b>F<sub>PD</sub></b>	10 MHz
<b>Crystal Frequency</b>	10 MHz	<b>Output Frequency</b>	2910 to 3132 MHz (DIV2=0) 1455 to 1566 MHz (DIV2=1)
<b>Supply Voltage</b>	3.0 Volts	<b>VCO Gain</b>	13 to 29 MHz/Volt



## Quick Setup

- Install the CodeLoader software which is available at [www.national.com/timing/software/](http://www.national.com/timing/software/).
- Attach the parallel cable or USB <--> uWire cable to the computer and the evaluation board.
- Connect 3.0 volts to the **Vcc** connector.
- Connect the **Fout** connector to a spectrum analyzer or phase noise analyzer.
- Connect a clean 10 MHz source to the **OSCin** pin. Typically, the 10 MHz output from the back of the RF test equipment is a good source. Signal generators tend to be very noisy and should be used with caution. If a signal generator is used, the signal generator phase noise contribution can be reduced by setting the signal to 80 MHz and dividing this down to a phase detector frequency of 10 MHz.
- Set up the CodeLoader software.
  - Select the proper part from the menu as Select Part->PLL+VCO->LMX2531LQ3010E
  - Select the proper mode from the Mode menu.
  - Load the part by pressing Ctrl+L or selecting Keyboard Controls->Load Device from the menu.
- It is recommended to ensure proper communication with the device.
  - Click the REG\_RST bit on the bits/pins page and observe the current go to 0 mA.
  - Unclick the REG\_RST bit AND press Ctrl+L. The current should be approximately 35 mA.
  - If device does not respond to this, consult the troubleshooting section.

## Troubleshooting

### Software does not communicate with the evaluation boards

#### LPT or USB Mode

- Ensure a valid signal is presented to the **OSCin** connector. If a signal generator is used, ensure the RF is ON.
- Consult the CodeLoader instructions for more detailed information on communication issues.

#### LPT Mode (Uses Parallel Port Cable)

- Ensure that CodeLoader is selected to LPT mode on the Port Setup tab
- Ensure the proper port number is selected (LPT1, LPT2, LPT3). CodeLoader does NOT automatically detect this.
- Ensure the LPT cable is securely connected to the computer and board.
- Exit and Restart CodeLoader.
- Ensure the parallel port is in the correct mode.
  - Windows often requires Administrative access to write to the parallel port.
  - Ensure that the parallel port is set to "Enabled" in windows device manager.
  - A reboot upon installation of CodeLoader is sometimes necessary to get the parallel port to work.
  - Standard mode is the most reliable. This can be set in the BIOS mode of the computer as "Normal", "Output Only", or "AT."

#### USB Mode (Uses USB <--> uWire Interface Board, NSID = USB2UWIRE)

- On the menu, select LPT/USB->Version to verify communication with the board.
- Ensure the Green LEDs are lit on the USB board.
- Ensure there are no conflicts with other USB devices and reinstall the board.

### Part responds to programming, but does not lock to the correct frequency

- Ensure that there is a valid signal presented to the **OSCin** connector. If a signal generator is used, ensure that the RF is set to ON.
- If using the lower frequency band (DIV2=1), the VCO frequency in CodeLoader should be twice the frequency at the Fout pin.
- Ensure that the VCO FREQUENCY CAL bits on the Bits/Pins tab are correct.
- Ensure that the loop filter is optimized if the charge pump current, phase detector frequency, or loop filter values have been changed from their original settings. Ensure that the integrated loop filter components on CodeLoader are set to their proper settings.

### Close-in phase noise is worse than evaluation board instructions show

- Ensure the signal presented to OSCin connector is clean. Try another source, or if it is a signal generator, try using a higher frequency and dividing it down to the phase detector frequency.
- Ensure the OSCin signal after the connecting cable provides sufficient power level.
- If the phase detector frequency or charge pump current are lowered from their original settings, the in-band phase noise can be degraded, even if the loop filter is re-designed for the same loop bandwidth.
- If the loop bandwidth is decreased, in-band phase noise can be degraded

## Far-out Phase noise is worse than evaluation board instructions show

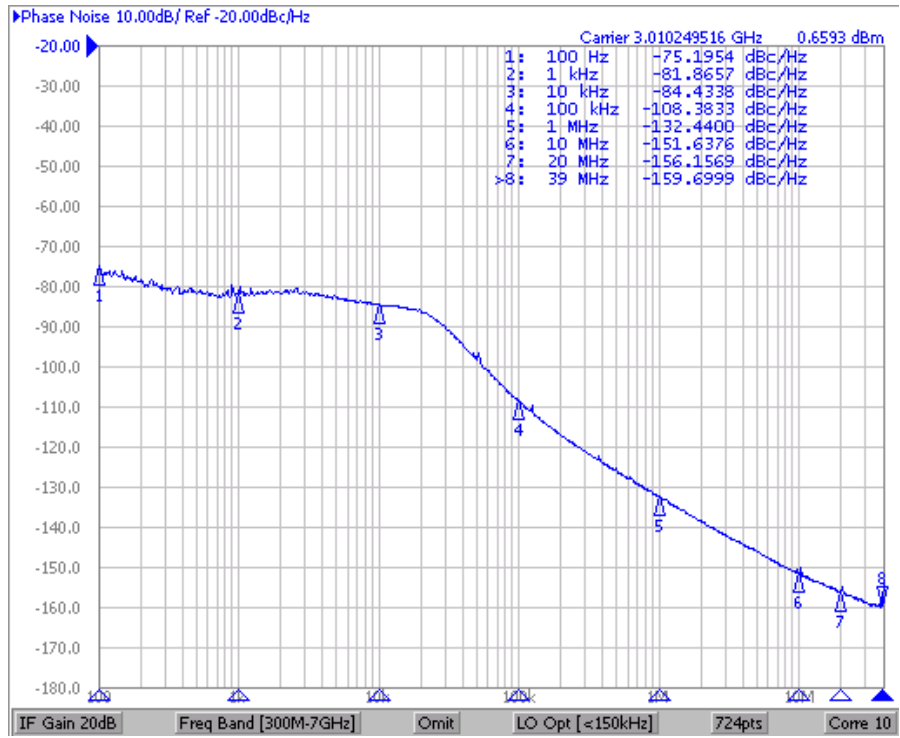
- Ensure the measurement equipment noise floor is not limiting the measurement. For spectrum analyzers, the noise floor at a particular setting can be measured by removing the RF input signal
- If the settings are changed from what the board was designed for, ensure the delta-sigma modulator is not increasing the far-out noise. To determine this, tune to an integer channel and set the ORDER bit to “Reset Modulator”. The far out phase noise should not decrease. If it does, try a loop filter with more attenuation or select a lower order delta-sigma modulator.

### Device Data

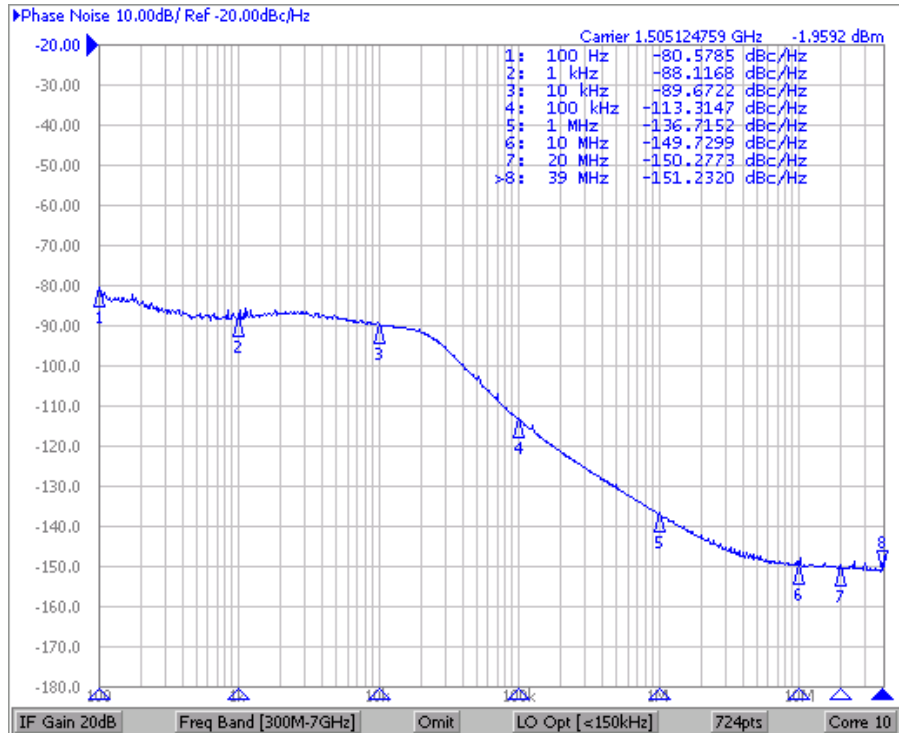
The next few pages show data collected from the LMX2531LQ3010 evaluation board.

### Phase Noise

Output Frequency = 3010.25 MHz  
Internal Divide by 2 Disabled (DIV2=0)

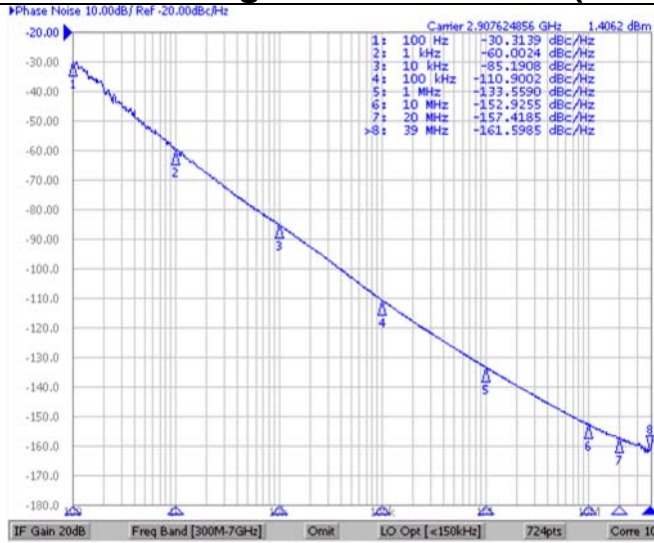


Output Frequency = 1505.125 MHz  
Internal Divide by 2 Enabled (DIV2=1)

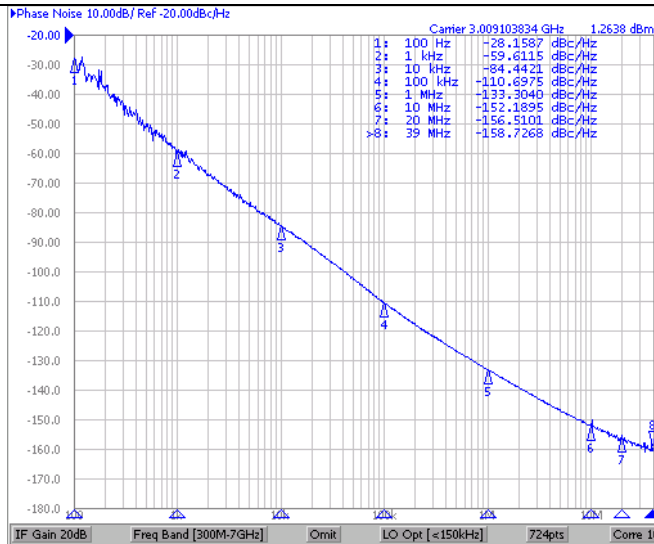


### Free-Running VCO Phase Noise (Internal Divide by 2 Disabled)

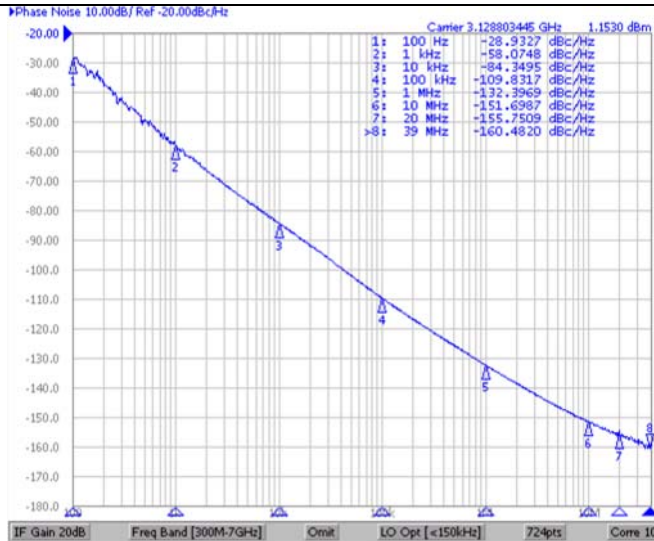
**Fout = ~2910 MHz**



**Fout = ~3010 MHz**



**Fout = ~3130 MHz**

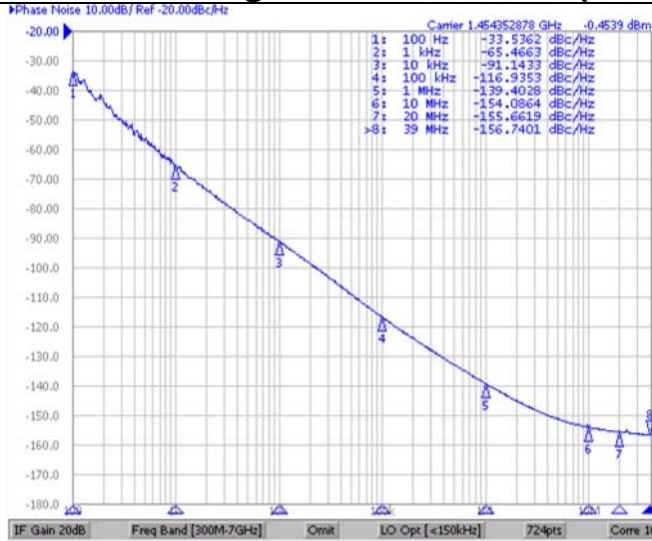


The plots to the left show the true phase noise capability of the VCO. In order to take these plots, the E5052 phase noise analyzer was used. The method was to lock the PLL to the proper frequency, then disable the EN\_PLL, EN\_PLLLDO1, EN\_PLLLDO2, EN\_DIGLDO, and EN\_OSC bits. The equipment needs to be able to track the VCO phase noise to measure in this way, and one can not let the VCO drift too far off in frequency. If this kind of equipment is not available, the VCO phase noise can also be measured by making a very narrow loop bandwidth filter.

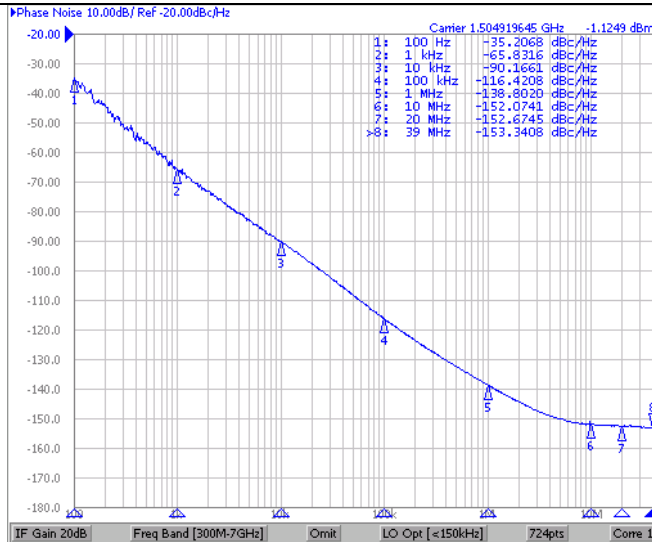


### Free-Running VCO Phase Noise (Internal Divide by 2 Enabled)

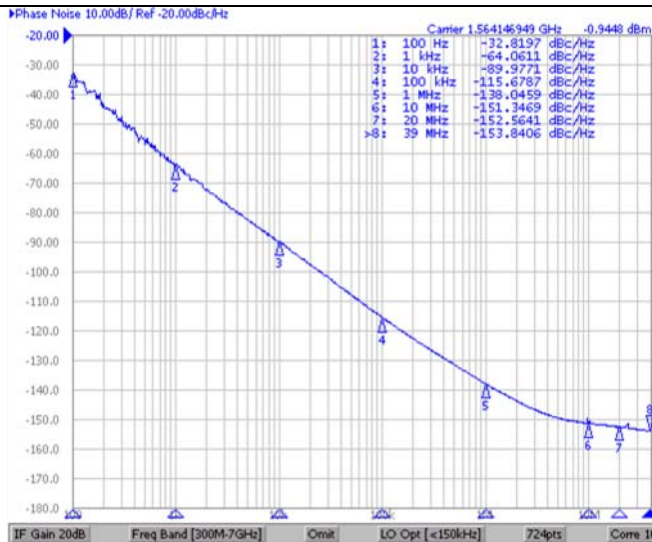
**Fout = ~1455 MHz (~2910 MHz/2)**



**Fout = ~1505 MHz (~3010 MHz/2)**



**Fout = ~1565 MHz (~3130 MHz/2)**

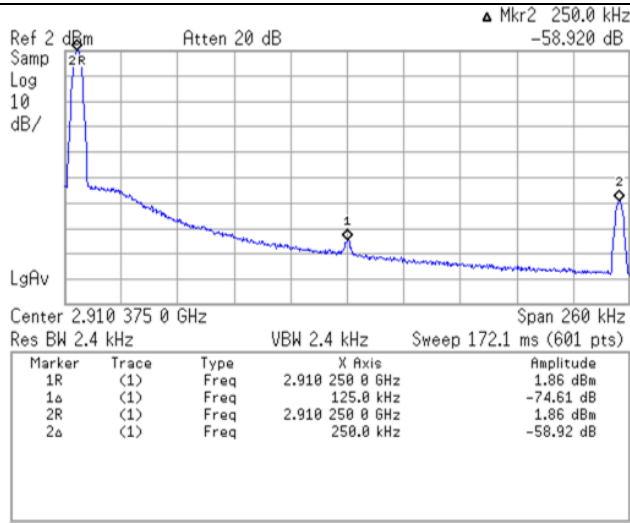


The plots to the left show the true phase noise capability of the VCO. In order to take these plots, the E5052 phase noise analyzer was used. The method was to lock the PLL to the proper frequency, then disable the EN\_PLL, EN\_PLLLDO1, EN\_PLLLDO2, EN\_DIGLDO, and EN\_OSC bits. The equipment needs to be able to track the VCO phase noise to measure in this way, and one can not let the VCO drift too far off in frequency. If this kind of equipment is not available, the VCO phase noise can also be measured by making a very narrow loop bandwidth filter.

When divide by 2 is enabled, the phase noise at lower offsets is about 6 dB better; but at high offsets, the phase noise improvement may be less because the divider noise floor is adding to the phase noise.

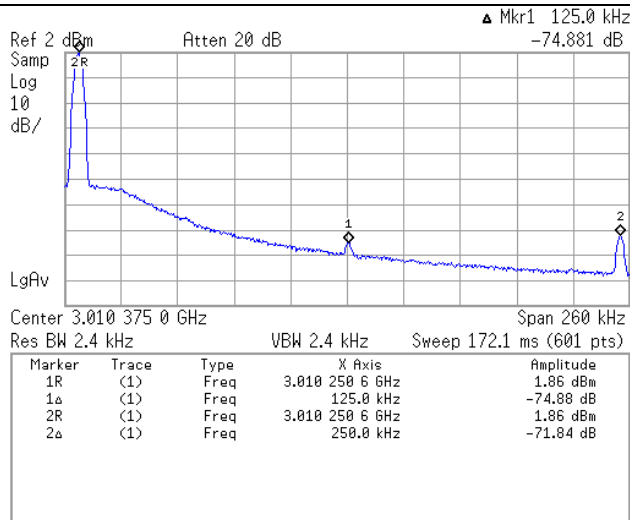


### Fractional Spurs (Internal Divide by 2 Disabled)



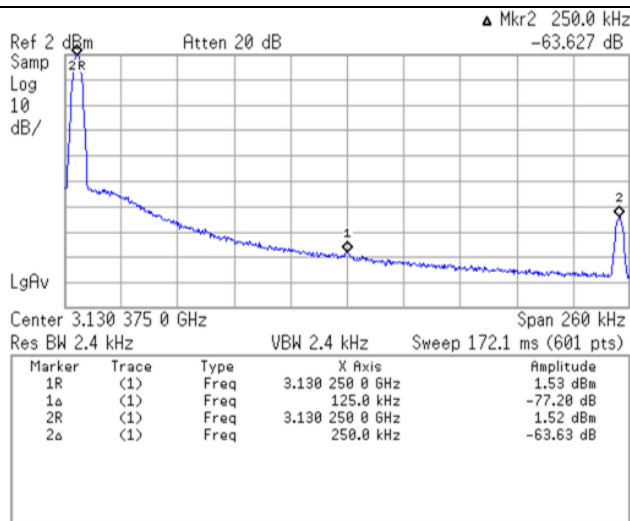
The -58.9 dBc fractional spur at 250 kHz offset is at a worst case frequency of 2910.25 MHz. The -74.6 dBc sub-fractional spur at 125 kHz offset is also visible.

Worst case channels occur at exactly one channel spacing above or below a multiple of the crystal frequency.



The -71.8 dBc fractional spur at 250 kHz offset is at a worst case frequency of 3010.25 MHz. The -74.9 dBc sub-fractional spur at 125 kHz offset is also visible.

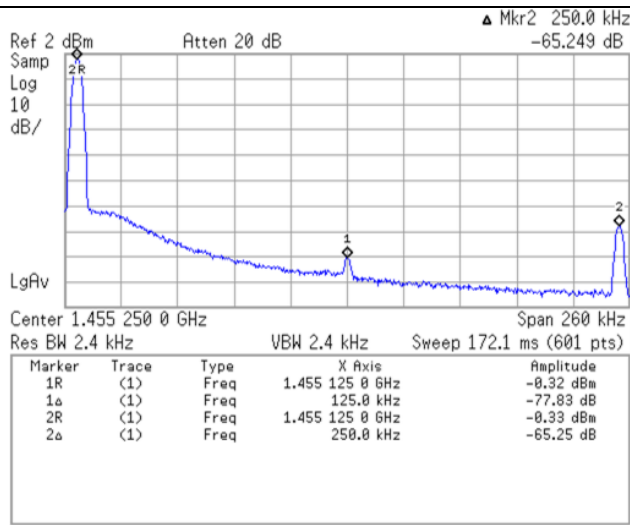
Worst case channels occur at exactly one channel spacing above or below a multiple of the crystal frequency.



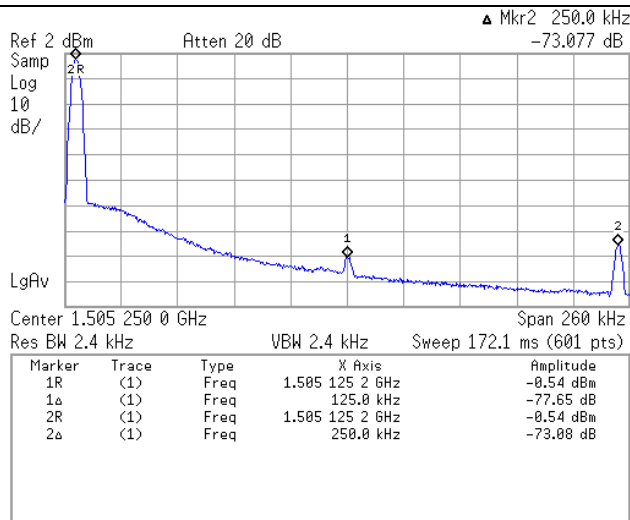
The -63.6 dBc fractional spur at 250 kHz offset is at a worst case frequency of 3130.25 MHz. The -77.2 dBc sub-fractional spur at 125 kHz offset is also visible.

Worst case channels occur at exactly one channel spacing above or below a multiple of the crystal frequency.

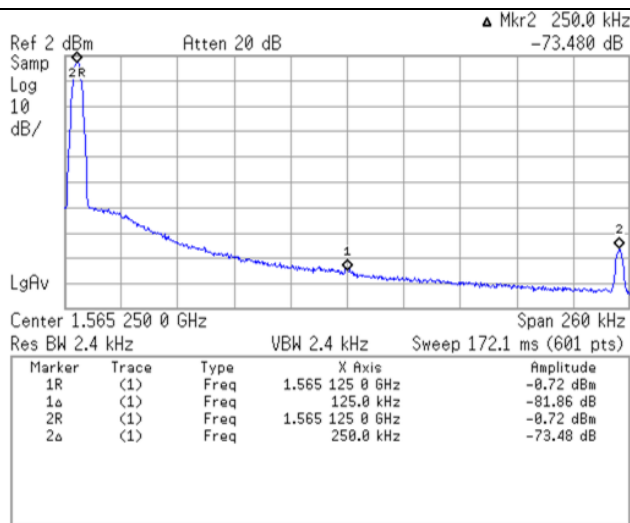
### Fractional Spurs (Internal Divide by 2 Enabled)



The -65.2 dBc fractional spur at 250 kHz offset is at a worst case frequency of 1455.125 MHz. The -77.8 dBc sub-fractional spur at 125 kHz offset is also visible.

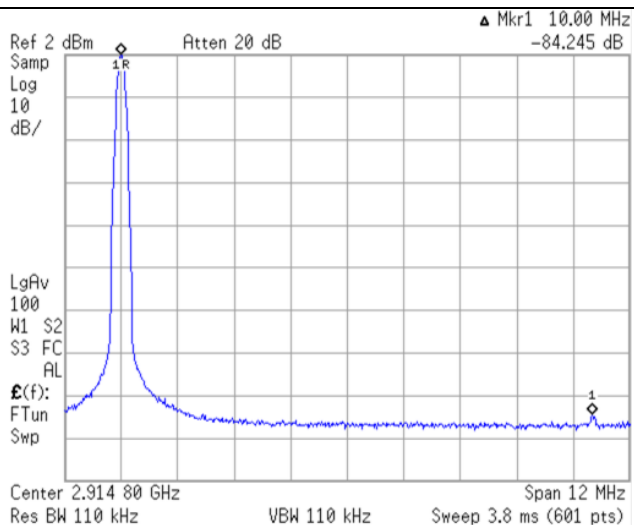


The -73.1 dBc fractional spur at 250 kHz offset is at a worst case frequency of 1505.125 MHz. The -77.6 dBc sub-fractional spur at 125 kHz offset is also visible.

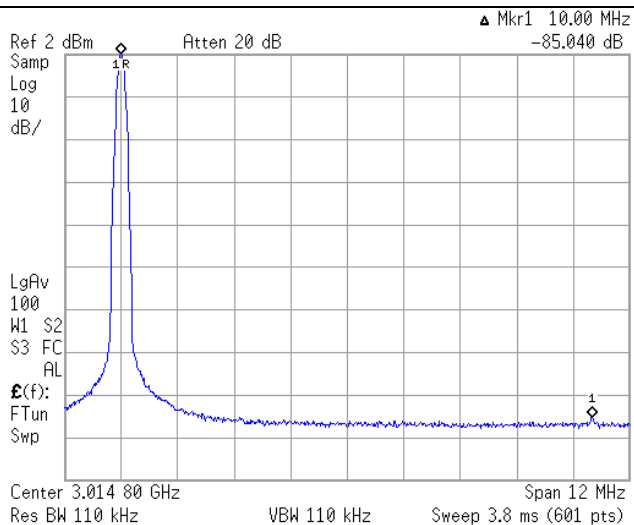


The -73.5 dBc fractional spur at 250 kHz offset is at a worst case frequency of 1565.125 MHz. The -81.9 dBc sub-fractional spur at 125 kHz offset is also visible.

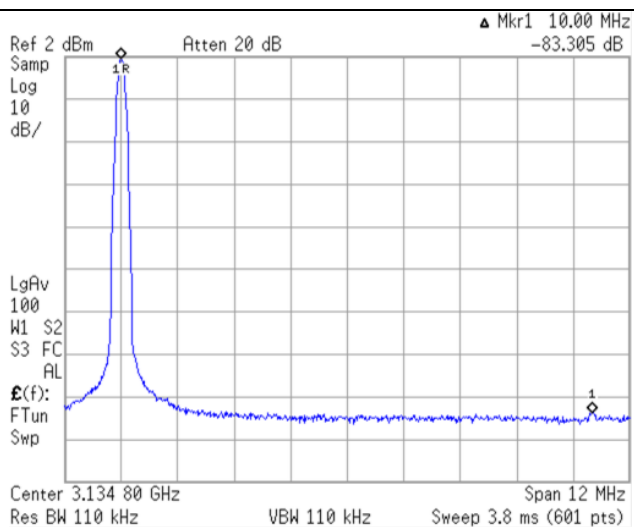
### Integer Spurs (Internal Divide by 2 Disabled)



The integer spur at 10 MHz offset at an Fout frequency of 2910 MHz is -84.2 dBc.

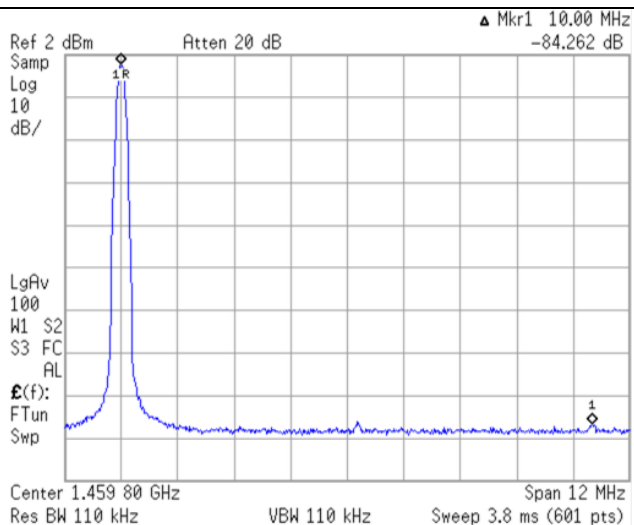


The integer spur at 10 MHz offset at an Fout frequency of 3010 MHz is -85.0 dBc.

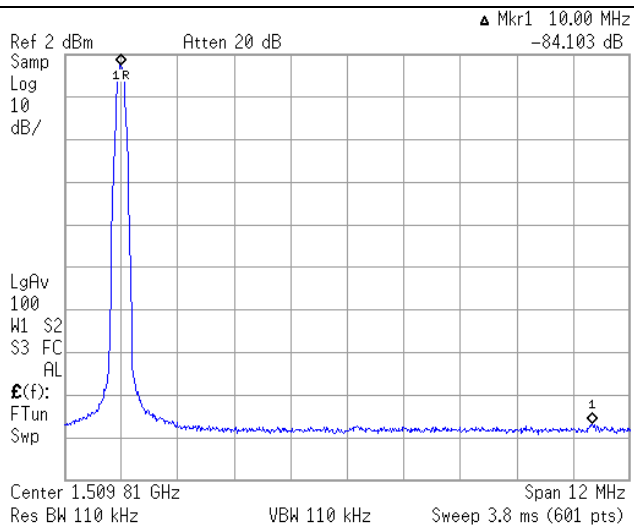


The integer spur at 10 MHz offset at an Fout frequency of 3130 MHz is -83.3 dBc.

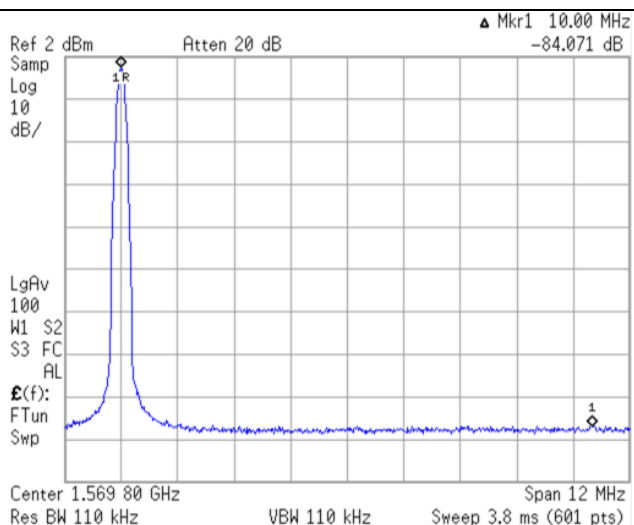
### Integer Spurs (Internal Divide by 2 Enabled)



The integer spur at 10 MHz offset at an Fout frequency of 1455 MHz is -84.3 dBc.

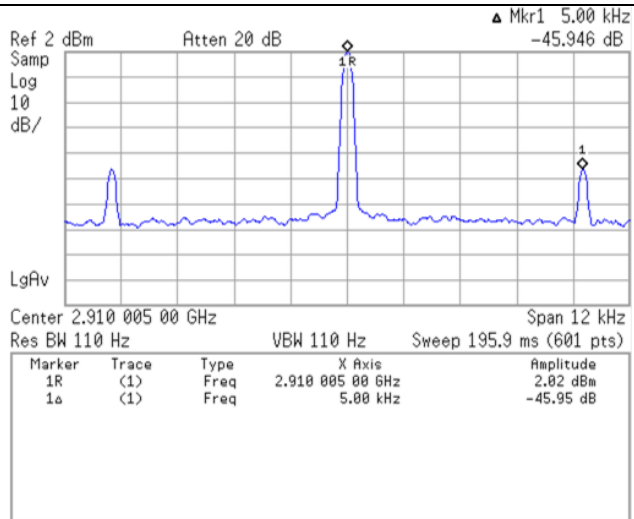


The integer spur at 10 MHz offset at an Fout frequency of 1505 MHz is -84.1 dBc.



The integer spur at 10 MHz offset at an Fout frequency of 1565 MHz is -84.1 dBc.

### In-band Fractional Spurs Integer Spurs (Internal Divide by 2 Disabled)

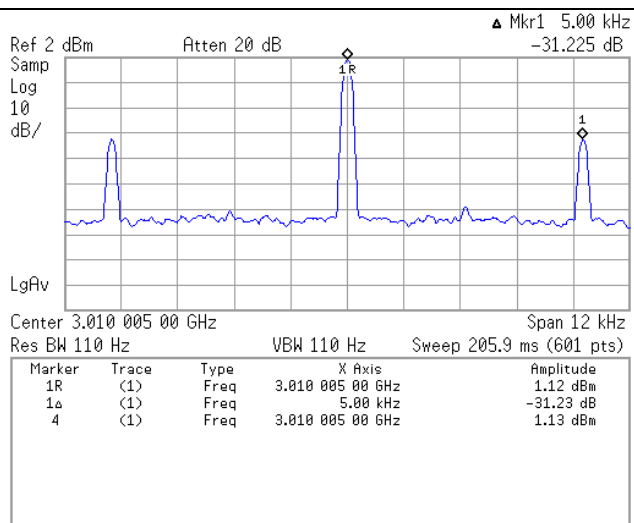


The In-band fractional spur at 5 kHz offset at an Fout frequency of 2910.005 MHz is -46.0 dBc.

ORDER = 4<sup>th</sup> Order Modulator

Fractional numerator = 500

Fractional denominator = 1,000,000

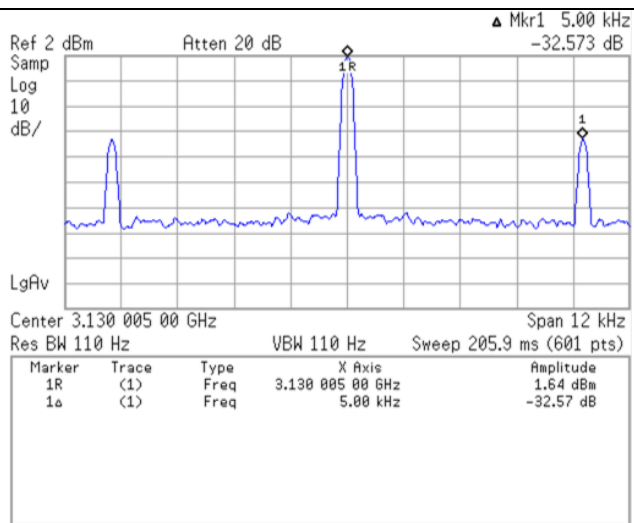


The In-band fractional spur at 5 kHz offset at an Fout frequency of 3010.005 MHz is -31.2 dBc.

ORDER = 4<sup>th</sup> Order Modulator

Fractional numerator = 500

Fractional denominator = 1,000,000



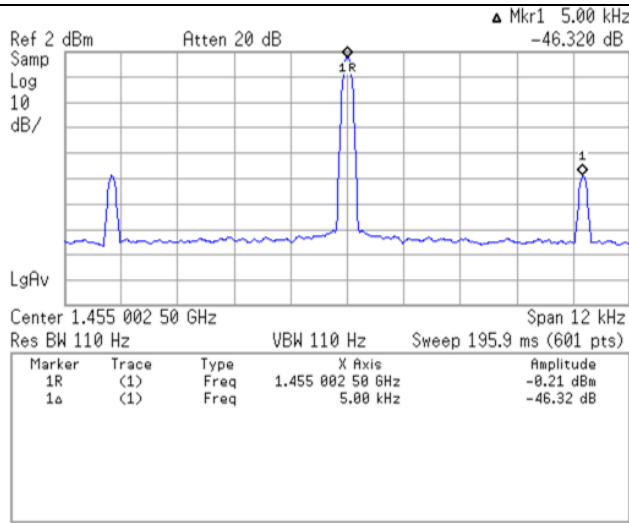
The In-band fractional spur at 5 kHz offset at an Fout frequency of 3130.005 MHz is -32.6 dBc.

ORDER = 4<sup>th</sup> Order Modulator

Fractional numerator = 500

Fractional denominator = 1,000,000

### In-band Fractional Spurs Integer Spurs (Internal Divide by 2 Enabled)

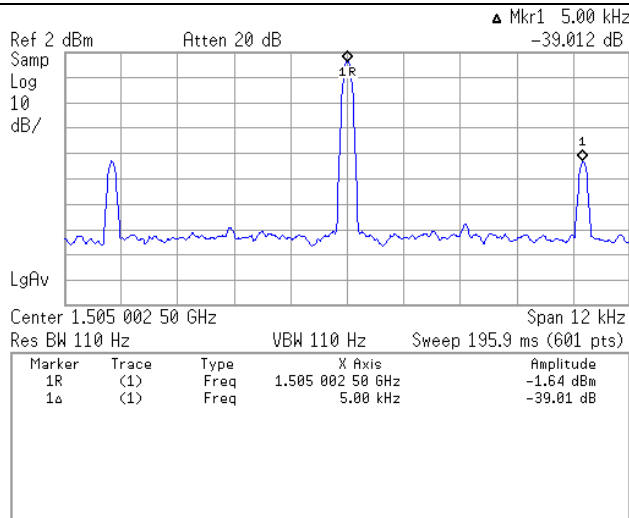


The In-band fractional spur at 5 kHz offset at an Fout frequency of 1455.0025 MHz is -46.3 dBc.

ORDER = 4<sup>th</sup> Order Modulator

Fractional numerator = 500

Fractional denominator = 1,000,000

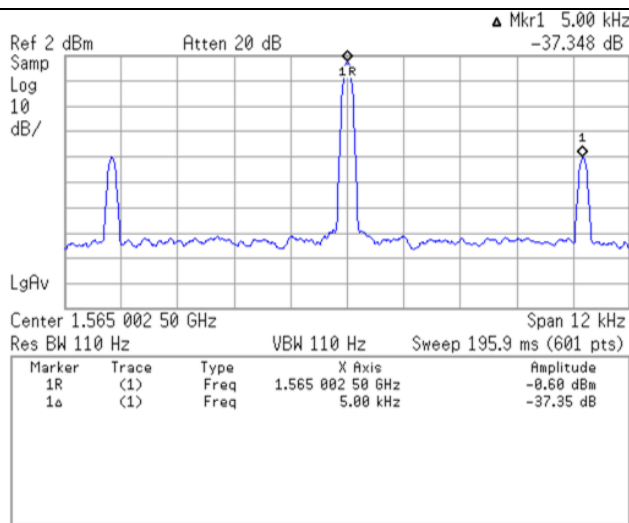


The In-band fractional spur at 5 kHz offset at an Fout frequency of 1505.0025 MHz is -39.0 dBc.

ORDER = 4<sup>th</sup> Order Modulator

Fractional numerator = 500

Fractional denominator = 1,000,000



The In-band fractional spur at 5 kHz offset at an Fout frequency of 1565.0025 MHz is -37.35 dBc.

ORDER = 4<sup>th</sup> Order Modulator

Fractional numerator = 500

Fractional denominator = 1,000,000

## Inter-modulation Spurs

The LMX2531 features an output divider which may divide the VCO frequency by two. The result is an  $F_{out}$  frequency half the VCO frequency. When this VCO divider is enabled a spur will occur between a multiple of the phase detector frequency and the  $F_{out}$  frequency.

In the example below the phase detector frequency ( $F_{PD}$ ) is 10 MHz. The VCO frequency is 3020.005 MHz. The divide by two is enabled and the output frequency ( $F_{out}$ ) is 1510.0025 MHz

1510 MHz = 10 MHz \* 151, which is a multiple of the  $F_{PD}$ .

1510.0025 MHz is the divided output frequency.

Therefore a spur will occur at 2.5 kHz offset = (1510.0025 – 1510 MHz)

If the frequency was set to 1509.9975 MHz there would be a spur at 2.5 kHz because:

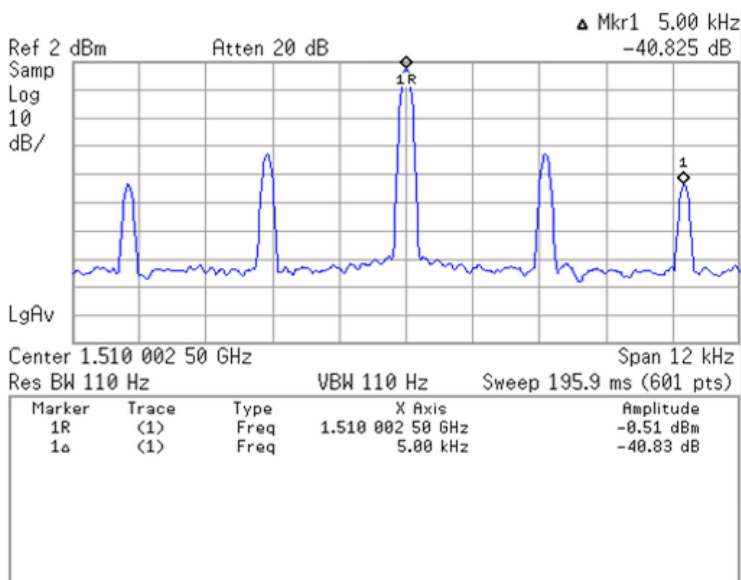
1510 MHz = 10 MHz \* 151, which is a multiple of the  $F_{PD}$ .

1509.9975 MHz is the divided output frequency.

Therefore a spur will occur at 2.5 kHz offset = (1509.9975 – 1510 MHz)

Technically there are spurs at caused by mixing with all multiples of the phase detector frequency but they will be far away from the carrier and the loop filter will eliminate them.

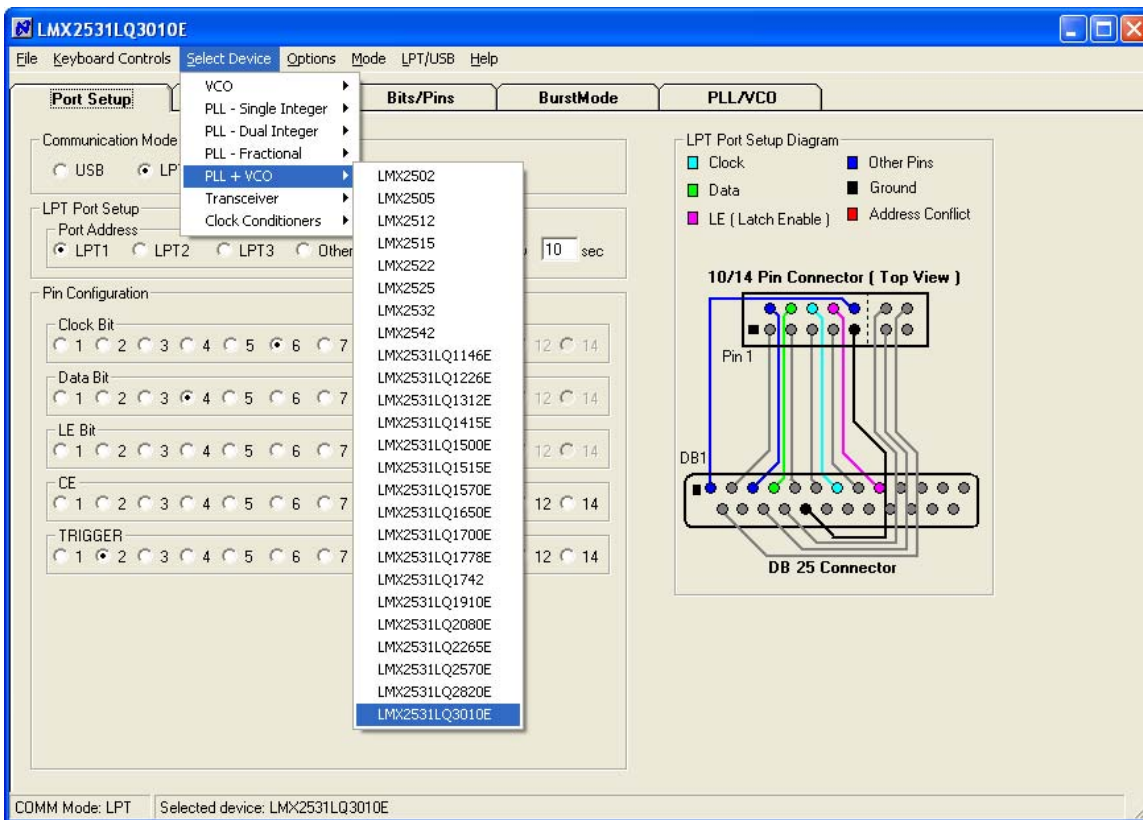
The spur shown below at 2.5 kHz off from 1510.0025 MHz is an example of inter-modulation that occurs. This only happens when the VCO divider is enabled.





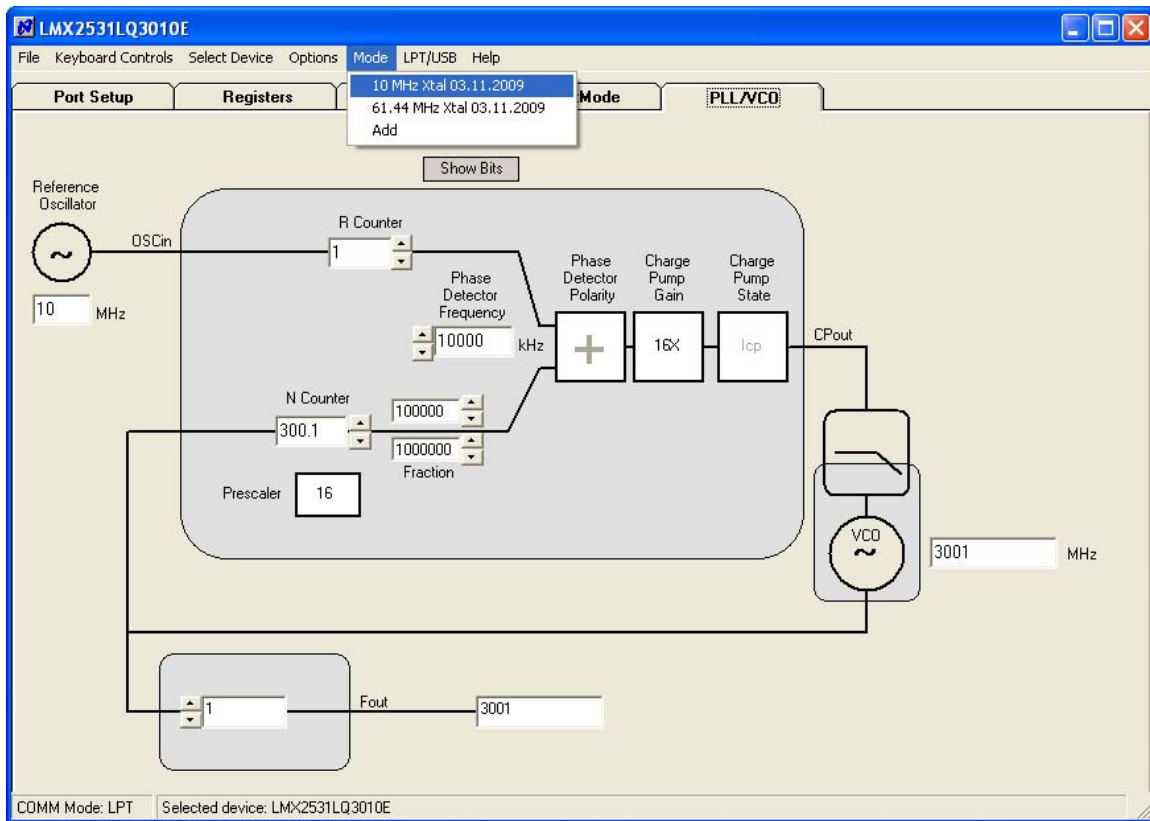
## CodeLoader Settings

### Select Device



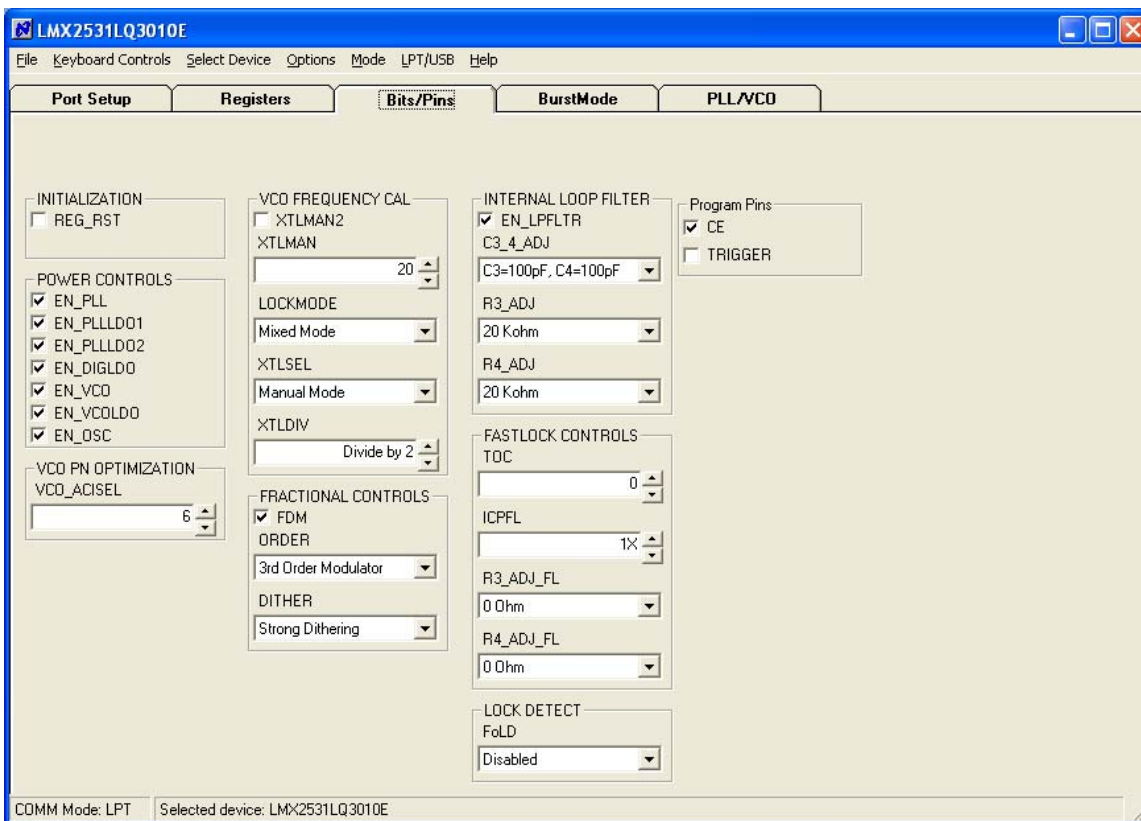
CodeLoader runs many devices. When CodeLoader is first started, it is necessary to select the correct device.

## Select Mode



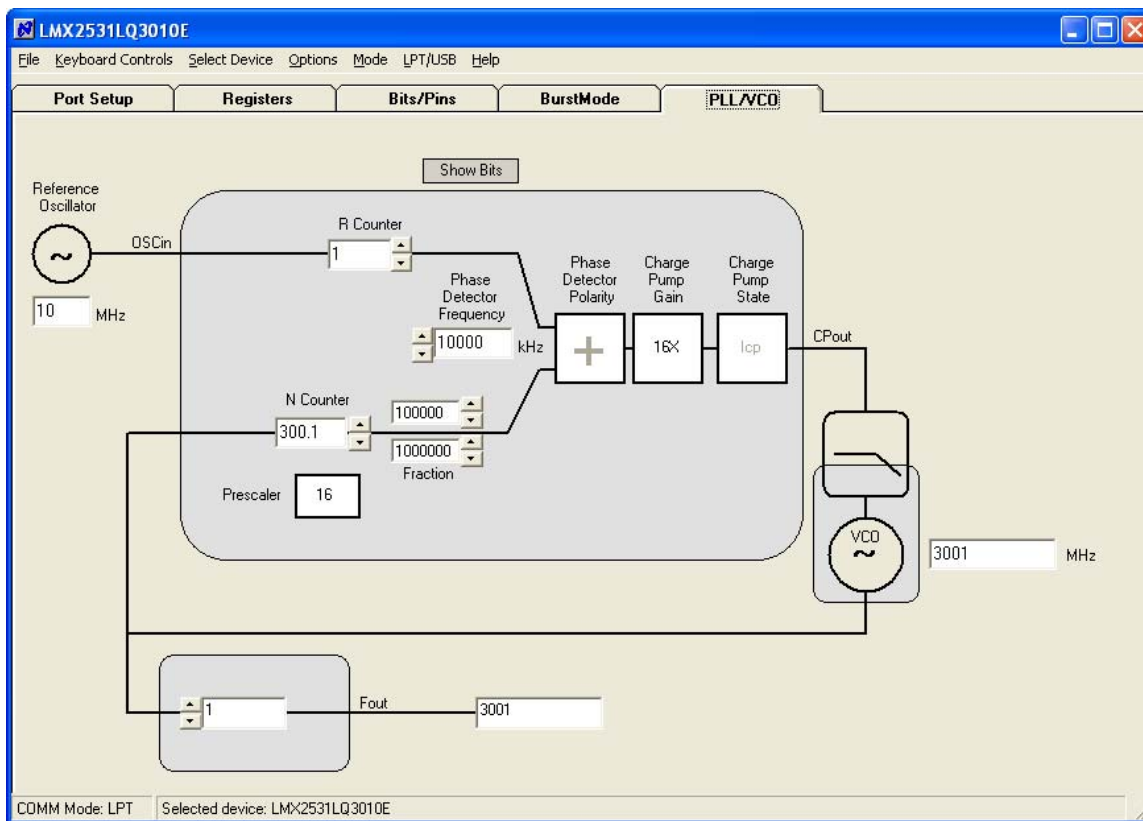
There can be different modes defined for a particular part. A mode can be recalled easily from the menu. This restores bit settings and frequencies, but not the Port Setup information. For the CodeLoader program, the default reference oscillator used for these instructions was 10 MHz, but there is a mode for a 61.44 MHz oscillator as well. If the bits become scrambled, their original state may be recalled by choosing the appropriate mode.

## Bits/Pins



The Bits/Pins tab displays many of the bits used to program the part. Right mouse click any bit to view more information about what this does.

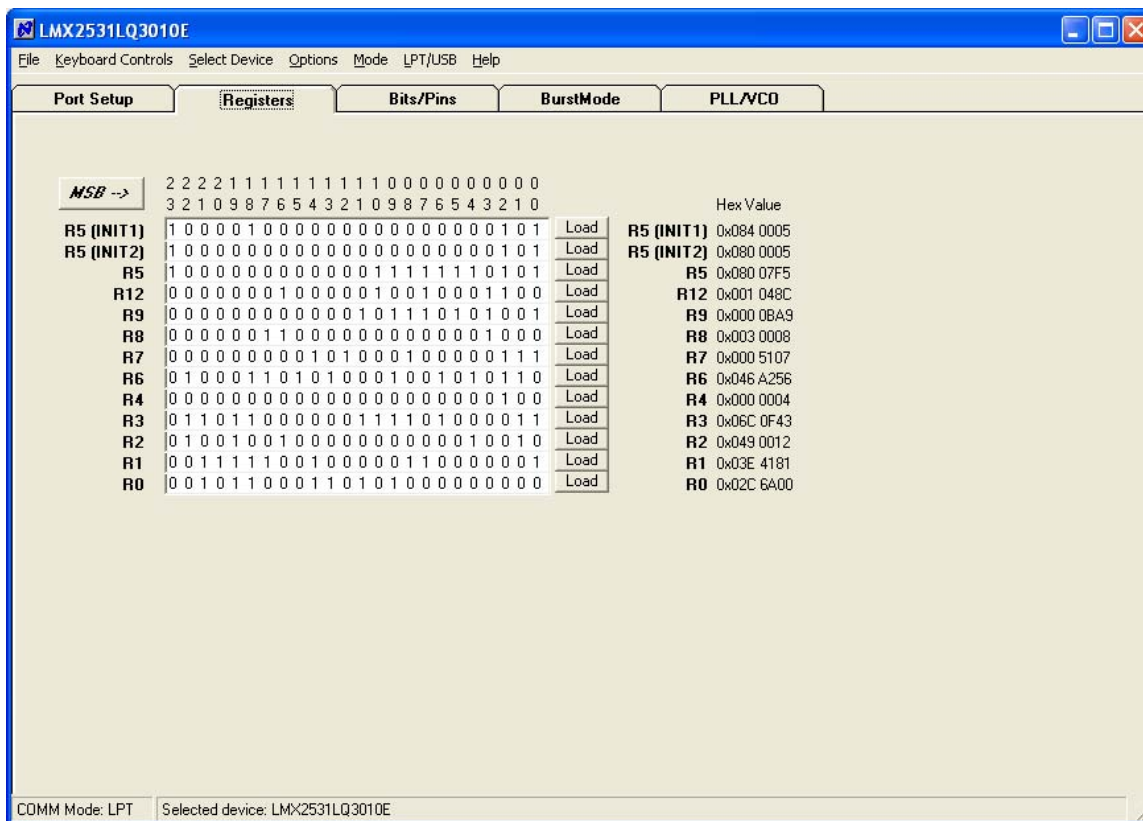
## PLL/VCO



The PLL/VCO tab shows all the important PLL controls. Reference Oscillator should be programmed to the reference frequency connected to the OSCin of the evaluation board. R Counter, Phase Detector Frequency, N Counter, and Charge Pump Gain should be set to provide the desired output frequency with an optimized loop filter. The desired VCO frequency may also be entered directly into the VCO frequency box.

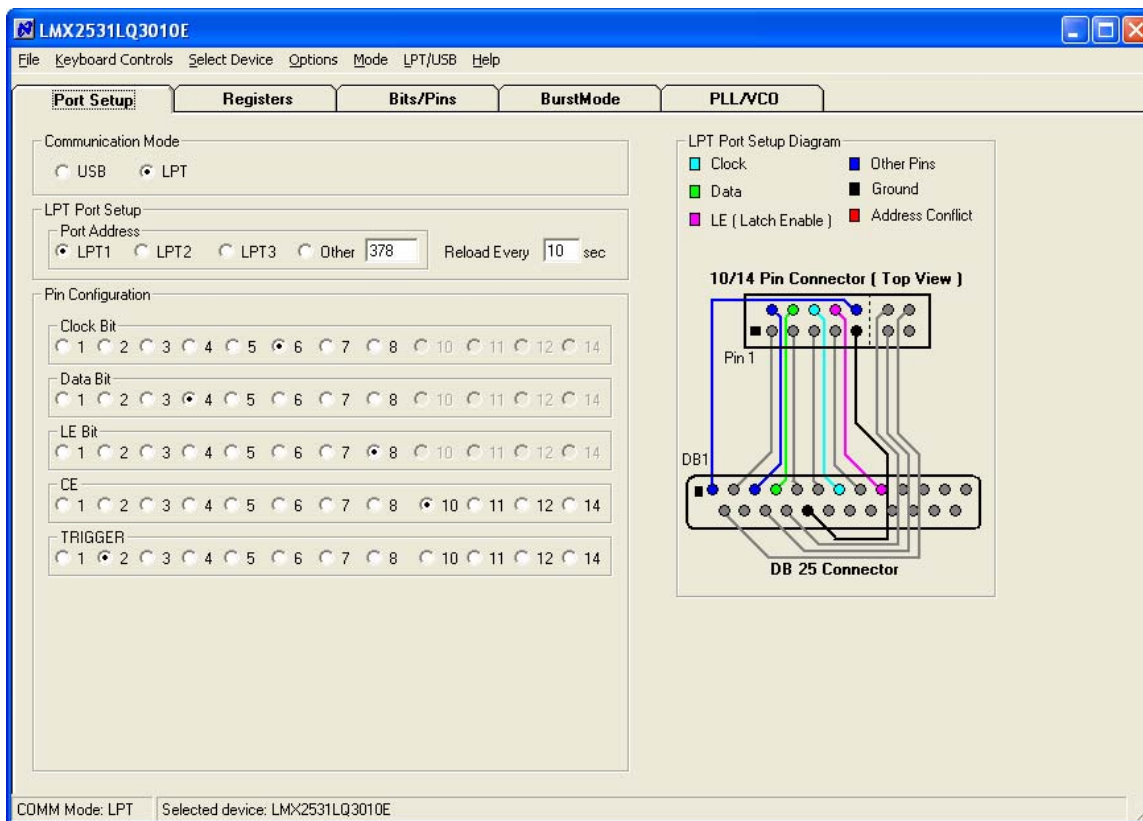
The LMX2531 also has an output divider which can be enabled by change divide value from 1 to 2 by Fout frequency box. Be sure to load the device (Ctrl+L) after changing this divider to allow the VCO to calibrate for optimal phase noise performance.

## Registers



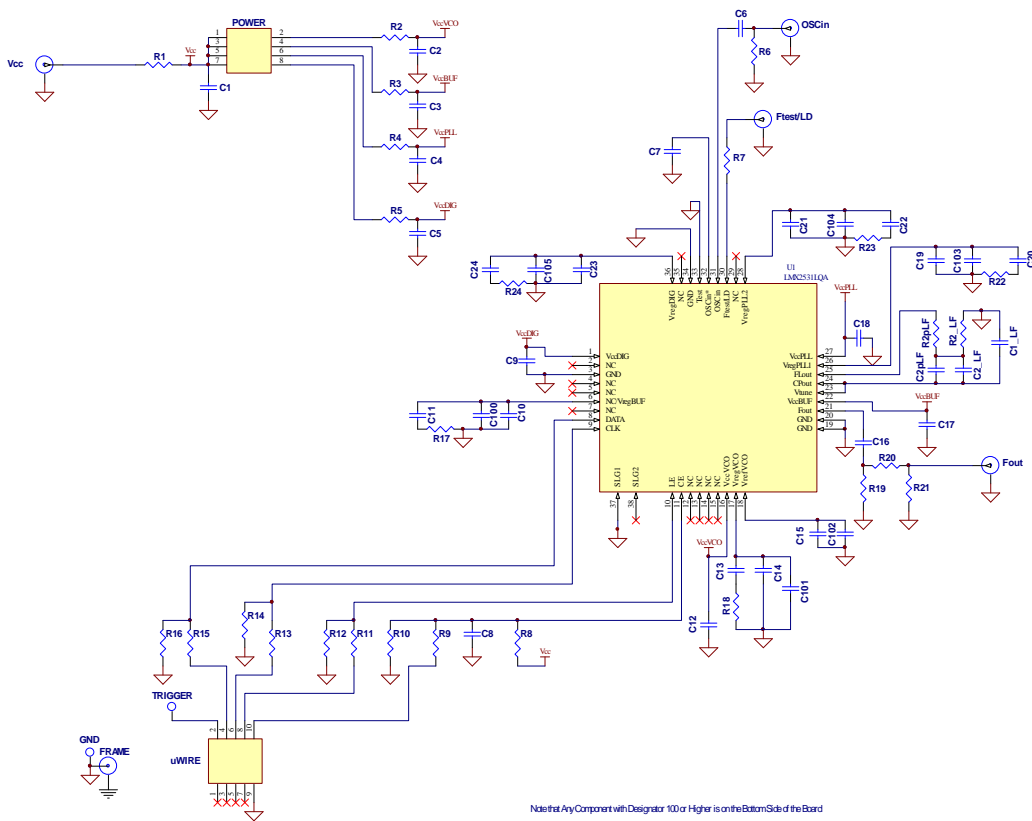
The Registers tab shows the literal bits that are being sent to the part. These are the registers every time the PLL is loaded by using the menu command or Ctrl+L. R5 (INIT1) and R5 (INIT 2) are just the R5 register being used to properly initialize the part. So a single Ctrl+L will load the part.

## Port Setup



The port setup tells CodeLoader what information goes where. If this is wrong, the part will not program. Although LPT1 is usually correct, CodeLoader does NOT automatically detect the correct port. On some laptops, it may be LPT3.

Schematic

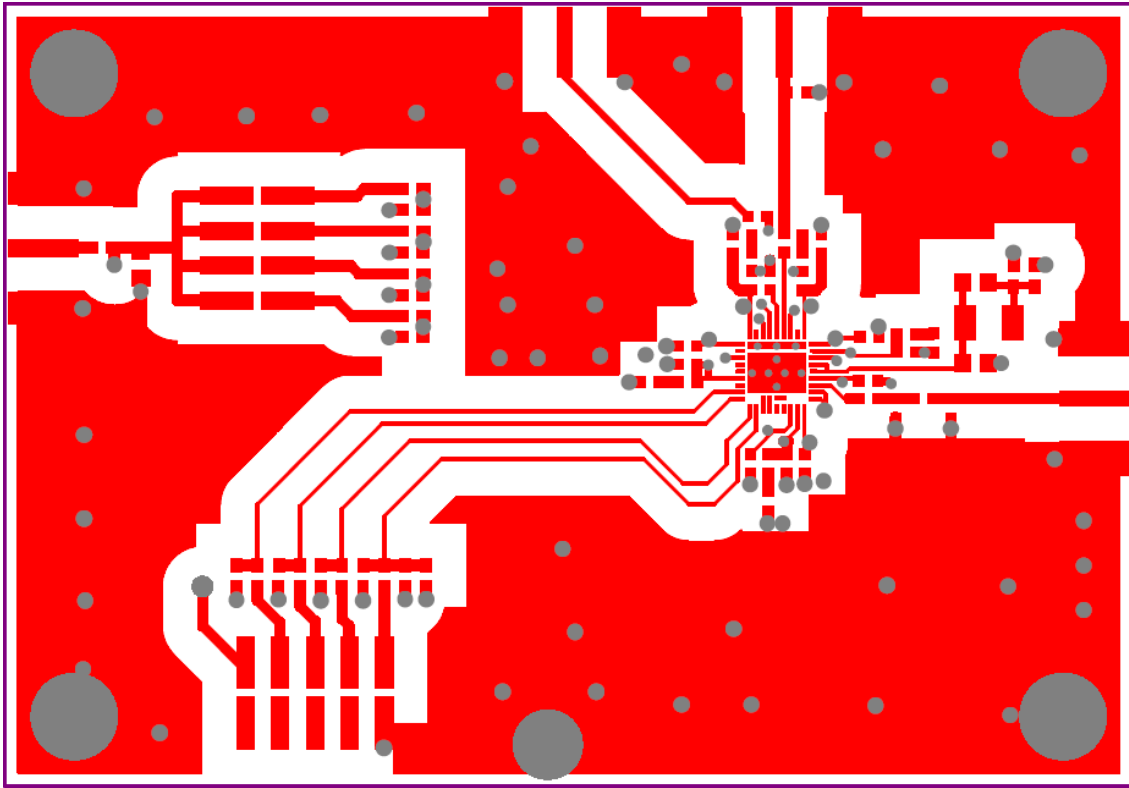




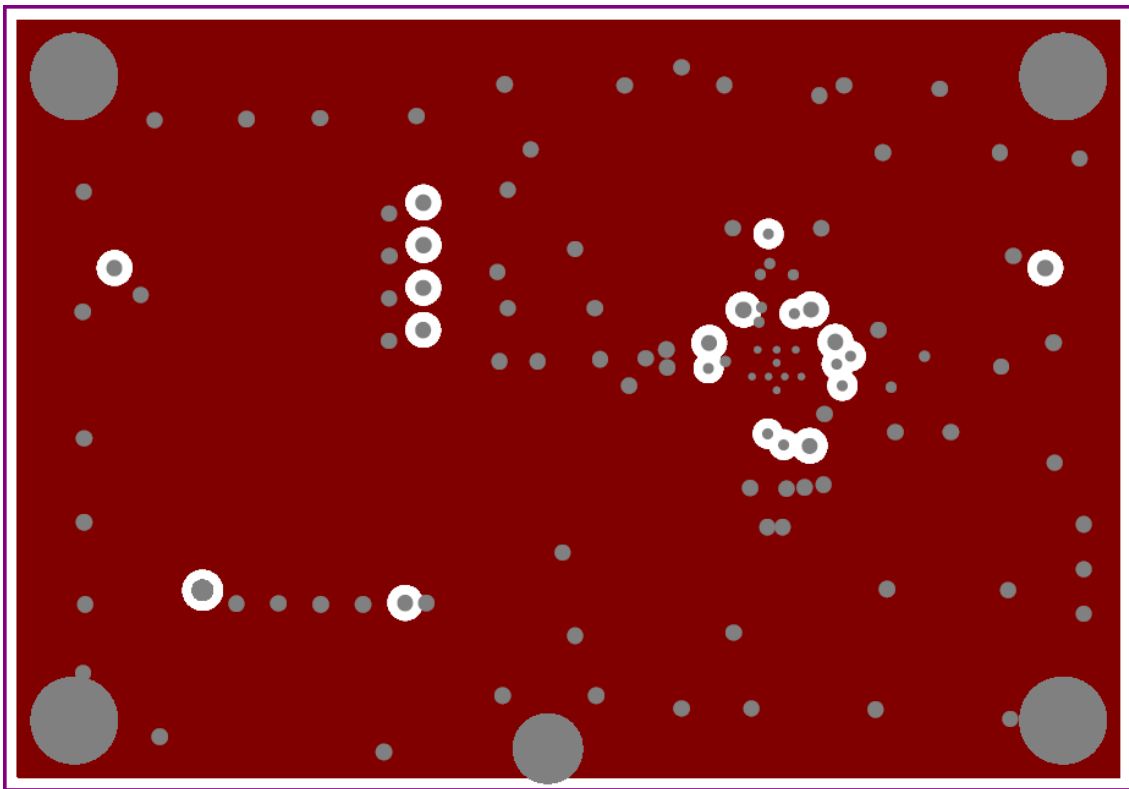
### Bill of Materials

Bill of Materials				LMX2531_HF					Revision 3.28.2008	
Item	QTY	Manufacturer	Part #	Size	Tol	Voltage	Material	Value	Designators	
0	20	n/a						Open Capacitors	C1_LF, C2pLF, C2, C3, C4, C5, C9, C11, C14, C17, C18, C19, C21, C24, C100, C101, C102, C103, C104, C105	
	7							Open Resistors	R2pLF, R7, R8, R17, R19, R21, R24	
	1							Open Miscellaneous	Ftest/LD	
1	1	Kemet	C0603C101J5GAC	603	5%	50V	C0G	100pF	C16	
2	2	Kemet	C0603C103J5RAC	603	5%	50V	X7R	10nF	C10, C23	
3	1	Kemet	C0805C104K5RACTU	805	5%	25V	C0G	100nF	C2_LF	
4	6	Kemet	C0603C104J3RAC	603	5%	25V	X7R	100nF	C6, C7, C12, C15, C22, C20	
5	1	Kemet	C0603C105K4RAC	603	10%	16V	X5R	1uF	C8	
6	1	Kemet	C0603C475K9PAC	603	10%	6.3V	X5R	4.7uF	C13	
7	1	Kemet	C0805C106K8PAC	805	10%	10V	X5R	10uF	C1	
8	1	Vishay	CRCW0603000ZRT1	603	5%	0.1W	Thick Film	0Ω	R20	
9	2	Panasonic	P.22AHCT-ND	603	10%	0.1W	Thick Film	0.22Ω	R22, R23	
10	2	Vishay	CRCW06033R3JRT1	603	5%	0.1W	Thick Film	3.3Ω	R1, R18	
11	4	Vishay	CRCW0603100JRT1	603	5%	0.1W	Thick Film	10Ω	R2, R3, R4, R5	
12	1	Vishay	CRCW0603510JRT1	603	5%	0.1W	Thick Film	51Ω	R6	
13	1	Vishay	CRCW0603102JRT1	603	5%	0.1W	Thick Film	1KΩ	R2_LF	
14	4	Vishay	CRCW0603103JRT1	603	5%	0.1W	Thick Film	10KΩ	R9, R11, R13, R15	
15	4	Vishay	CRCW0603123JRT1	603	5%	0.1W	Thick Film	12KΩ	R10, R12, R14, R16	
16	1	Comm Con Connectors	HTSM3203-8G2	2X4	n/a	n/a	Metal/Plastic	Header	POWER	
17	1	FCI Electronics	52601-S10-8	2X5	n/a	n/a	Metal/Plastic	Header	uWire	
18	3	Johnson Components	142-0701-851	SMA	n/a	n/a	Metal	SMA	Fout, OSCin, Vcc	
19	1	National Semiconductor	LMX2531LQEBPCB	n/a	n/a	n/a	FR4	PCB Board	n/a	
							62 mil Thick	1st Layer 10 mils		
20	1	National Semiconductor	LMX2531	LLP36	n/a	2.7	Silicon	LMX2531	U1	
21	4	Com Con Connectors	CCIJ255G	2-Pin	n/a	n/a	Metal/Plastic	Shunt	Place Across:	
									POWER: 1-2, 3-4, 5-6, 7-8	
22	4	SPC Technology	SPCS-8	0.156"	n/a	n/a	Nylon	Nylon Standoffs	Place in 4 Holes in Corners of Board	

Top Layer

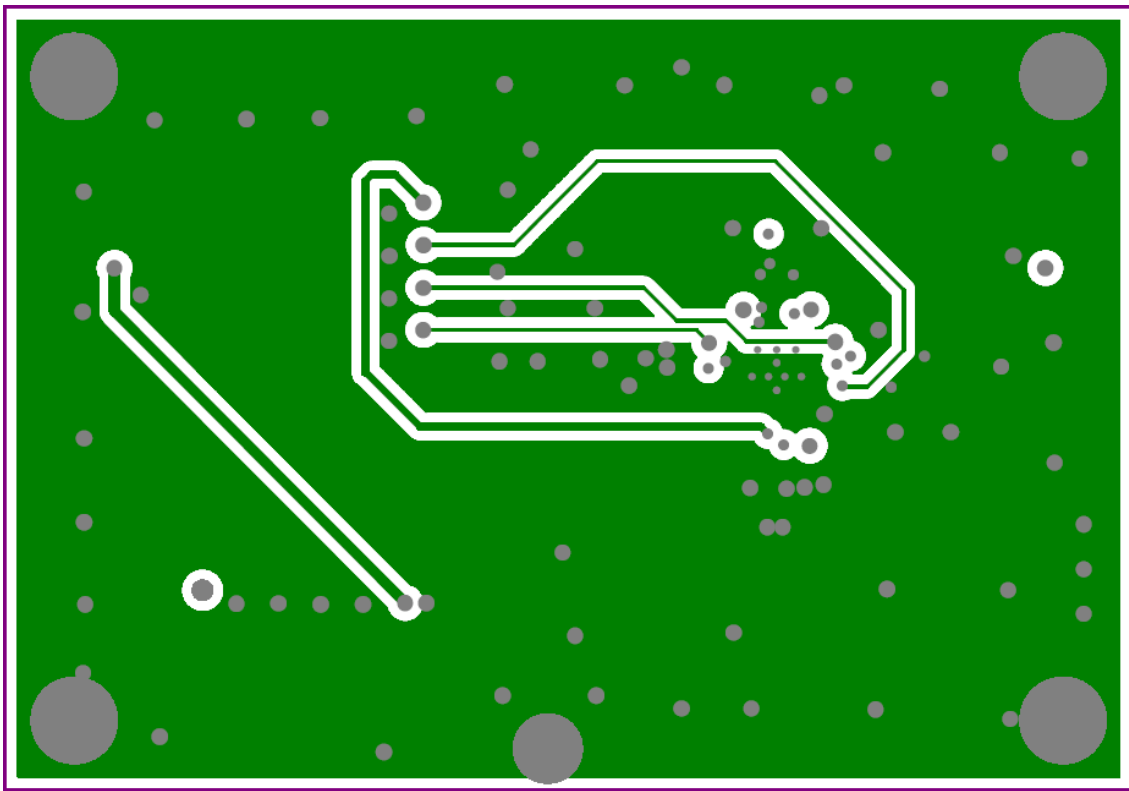


Mid Layer 1 "Ground Plane"

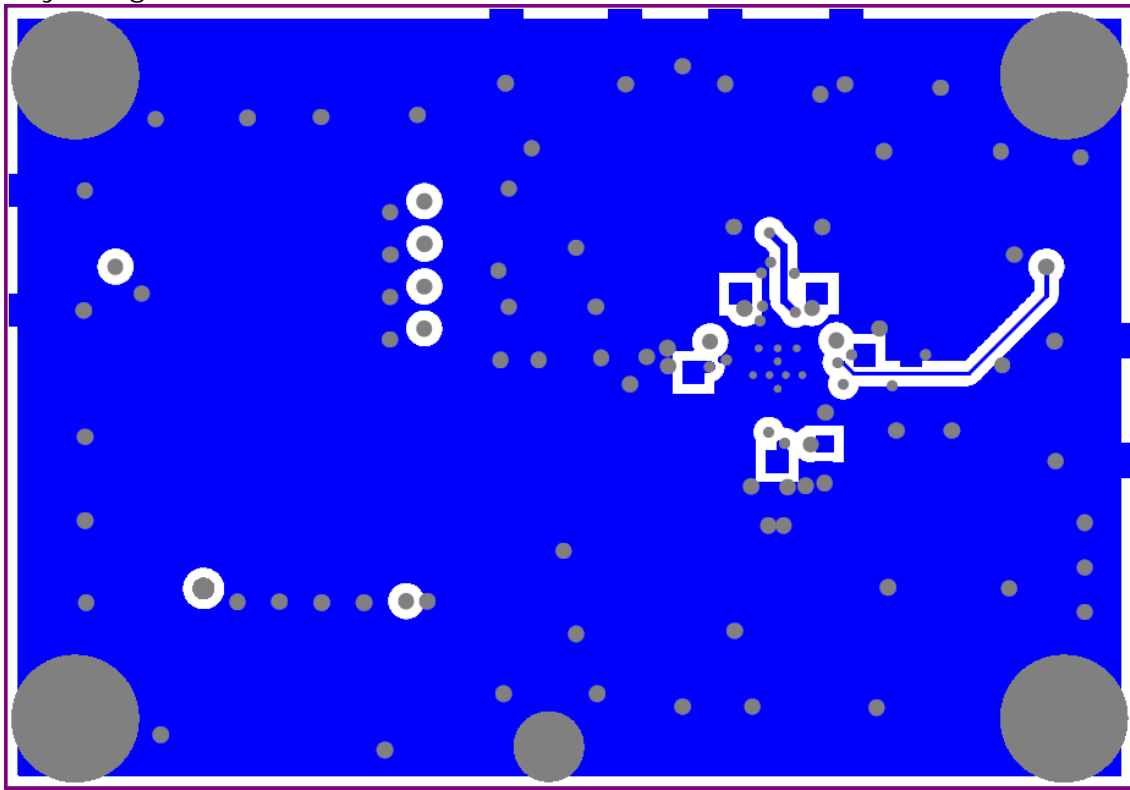


(15 mils below top FR4 layer)

Mid Layer 2 "Power"



Bottom Layer "Signal"



Note: Total Board Thickness = 61 mils

### Top Build Diagram

