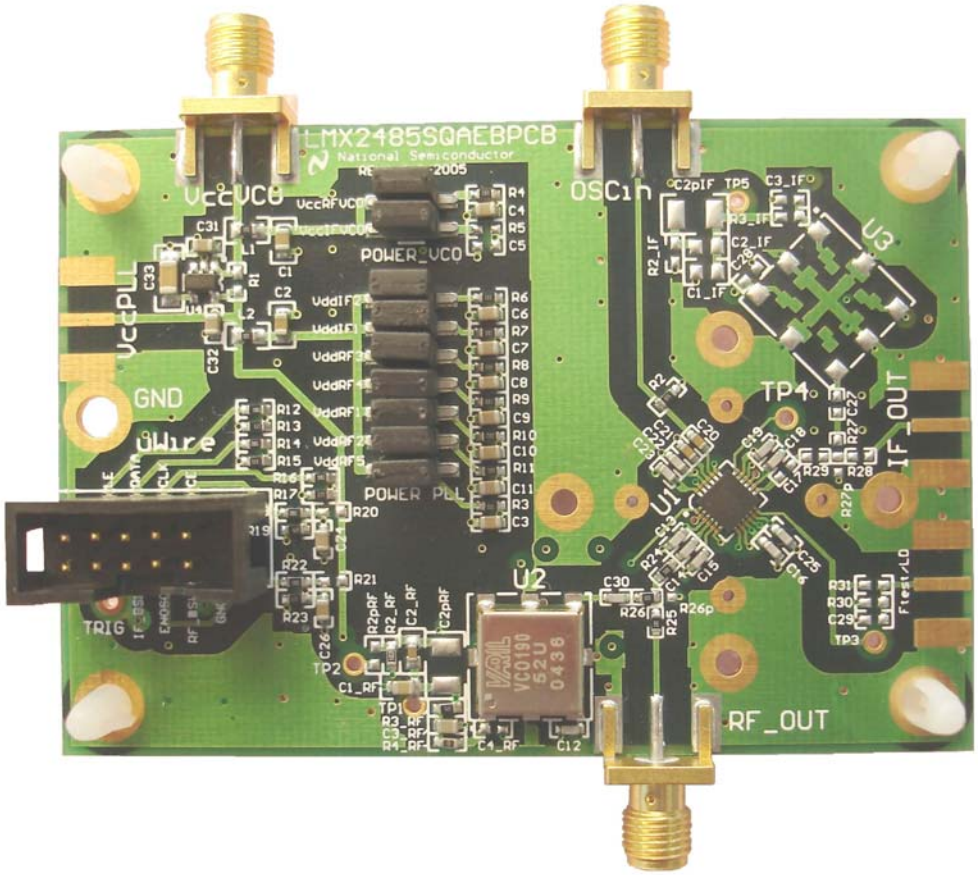
LMX2485E Evaluation Board Instructions



National Semiconductor Corporation
Wireless Communications, RF Products Group

2900 Semiconductor Dr.
M/S A2-600
Santa Clara, CA 95052-8090

LMX2485ESQFPEBI Rev 3.10.2006

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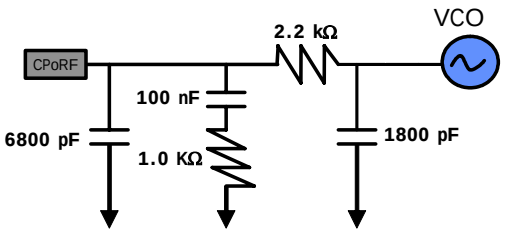
General Description

The LMX2485E Evaluation Board simplifies evaluation of the LMX2485E 2.6 GHz/0.8 GHz PLLatinum™ dual frequency synthesizer. The primary function of this board is to evaluate the LMX2485E device performance at low RF input frequencies, which is 50 MHz.

The board enables all performance measurements with no additional support circuitry. The evaluation board consists of a LMX2485E device, an RF VCO module and RF loop filters built with discrete components. The SMA flange mount connectors are provided for an external reference input, an RF VCO output, and a power connection. A cable assembly is bundled with the evaluation board for connecting to a PC through the parallel port. By means of MICROWIRE™ serial port emulation, the CodeLoader software included can be run on a PC to facilitate the LMX2485E internal register programming for evaluation and measurement.

The VCO used on the evaluation board is a Sirenza VCO190-52U. Using a 5 Volt supply, the frequency range of the Sirenza VCO190-52U is specified to cover 51 to 53 MHz with a 0.5V to 4.5 V control. The LMX2485E device is powered from a 3.3 V regulated supply, which gives a Charge Pump output dc voltage swing of 0.5 to 2.7 volts for optimum performance. Charge Pump output voltage can be measured at TP1. With these voltages, the VCO output frequency will nominally be 48.6 to 49.6 MHz. No IF VCO is attached. Therefore, the IF section is powered down for all measurements.

RF Loop Filter			
Phase Margin	48.0 deg	Pole Ratio T3 /T1	29.8 %
Loop Bandwidth	4.5 kHz		
Lock Time	48.6 – 49.6 MHz to 1 kHz tolerance in 450 us w/o CSR	Roll-Off @ 200 KHz	-68.4 dB
		**Settings for Operation**	
		Kϕ	8X (760 uA)
		Comparison Frequency	1000 kHz
		Output Frequency	48.6 – 49.6 MHz
		PLL Supply	3.3 Volts
		VCO Supply	5 Volts
		Other Information	
		VCO Used	SIRENZA VCO190-52U
		VCO Gain	2.5 MHz/Volt
		VCO Input Capacitance	820 pF

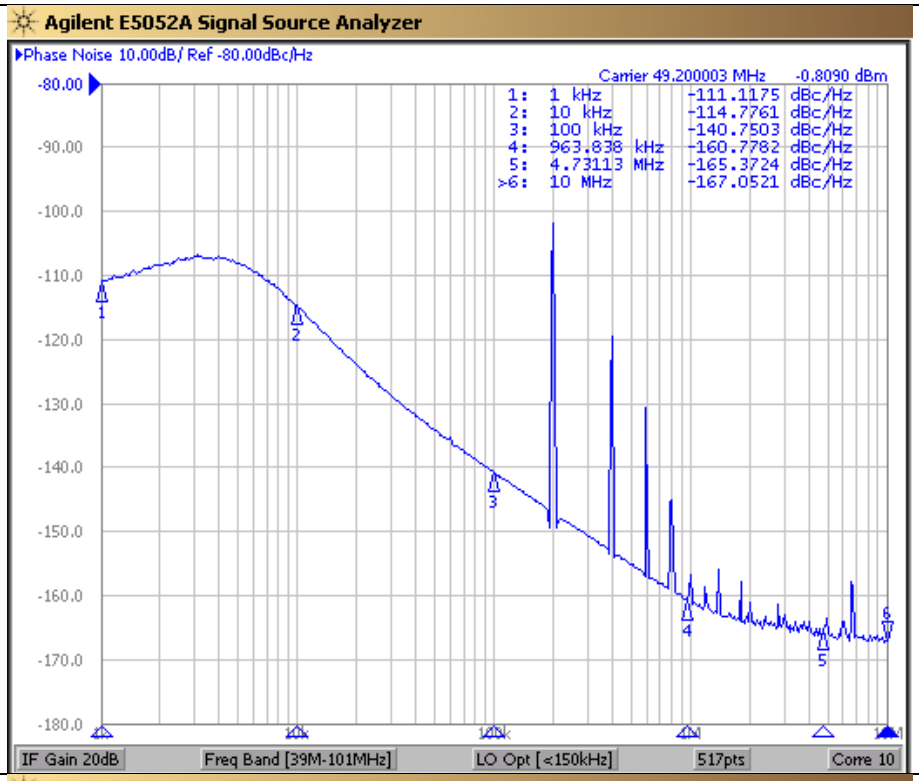
Evaluation Hints

It is strongly recommended that the user reviews sections 1.9 FRACTIONAL SPUR AND PHASE NOISE CONTROLS and 2.1.2 RF_N[10:0] – RF N Counter Value in the LMX2485/LMX2485E Datasheet. These sections will specify minimum divide ratio limits for the LMX2485E. This will determine how high the comparison frequency can be. Also, it points out that lower order modulators have better performance. It seems that the best performance at these low frequencies is with the dithering disabled. Also, it seems that there is improved and consistent performance with lower fractional denominators at these low frequencies. Page 11 shows Impact of Large Fractional Denominator on fractional spurs.

It is recommended that the minimum slew rate specification of 100 V/µs be maintained. If the power level is 1 dBm or higher, the slew rate specification will be met at 50 MHz. Slew rates less than 100 V/µs could have an negative effect on the performance of the LMX2485E.

The default state for the LMX2485E Evaluation board in these instructions are 2nd delta sigma modulator with dithering disabled and charge pump current set to 8X (0.76 mA). Also RF_P is set to 1 for a Prescaler value of 8 to achieve low divide ratios while not violating minimum divide ratio specifications.

RF PLL Phase Noise with Different CP Currents



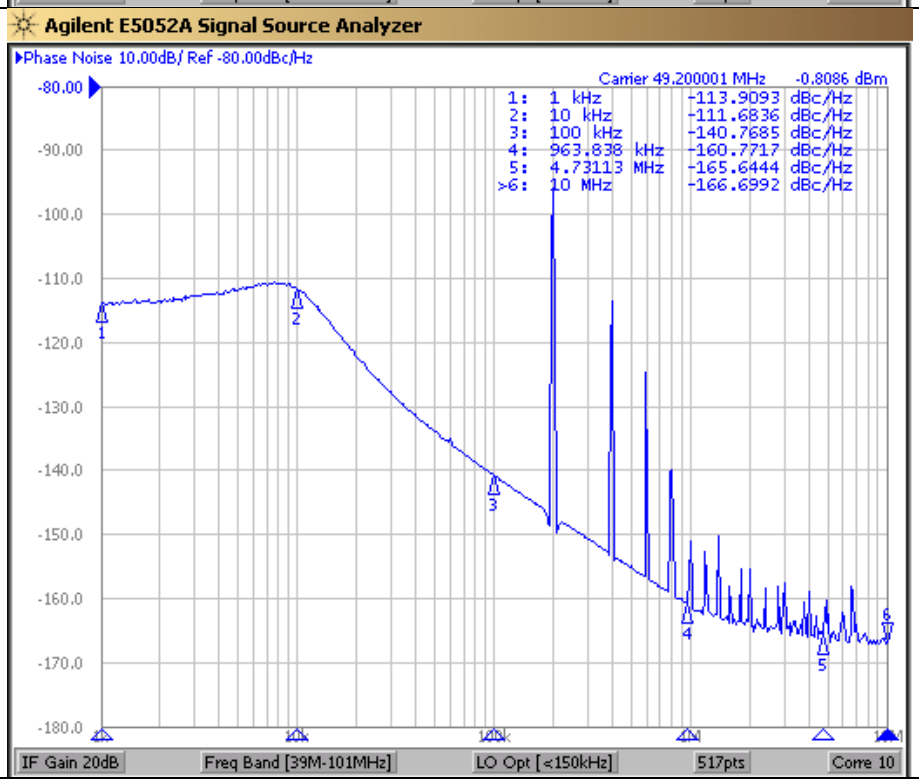
Phase Noise measured at 49.2 MHz

CP gain = 0.76 mA (8X) (default setting)

FM=2

Fraction Compensation set to 1/5

Dithering disabled



Phase Noise measured at 49.2 MHz

CP gain = 1.52mA (16X)

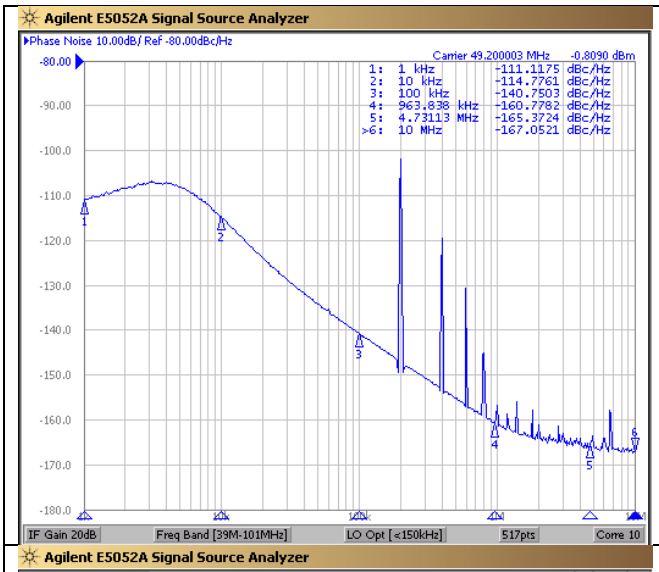
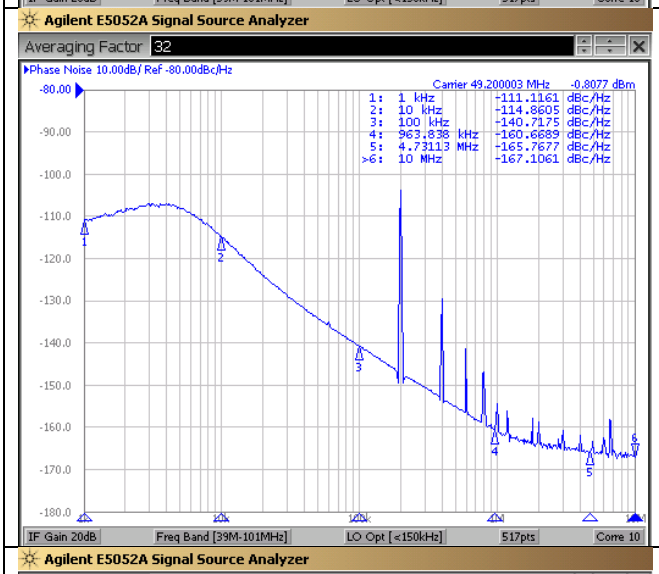
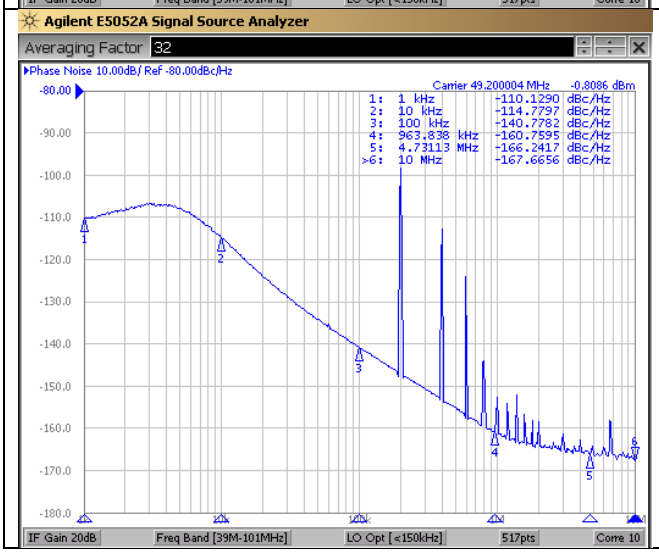
FM=2

Fraction Compensation set to 1/5

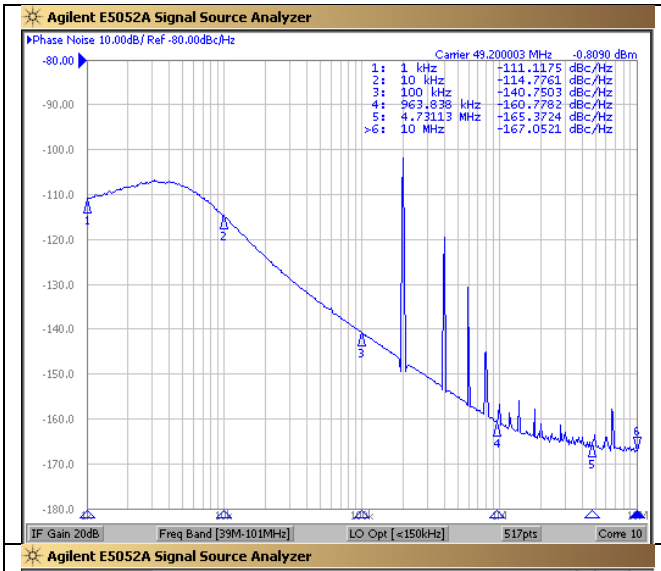
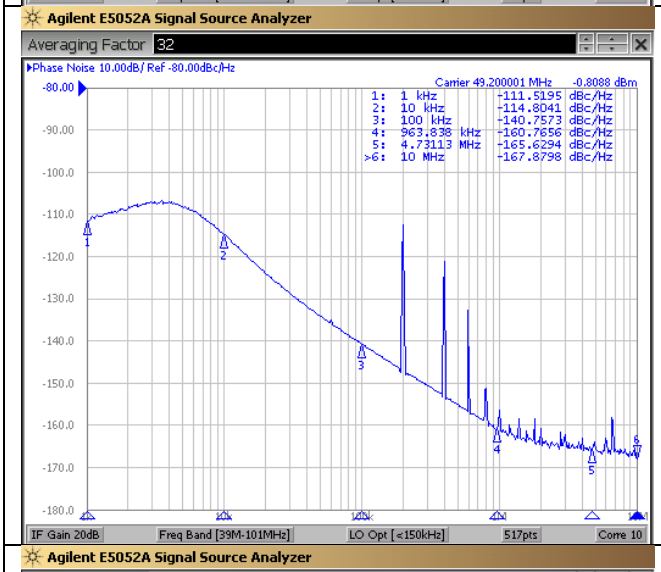
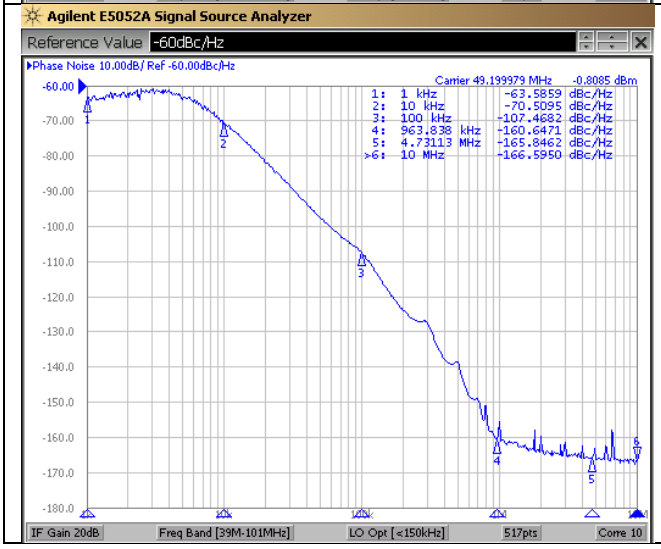
Dithering disabled

.

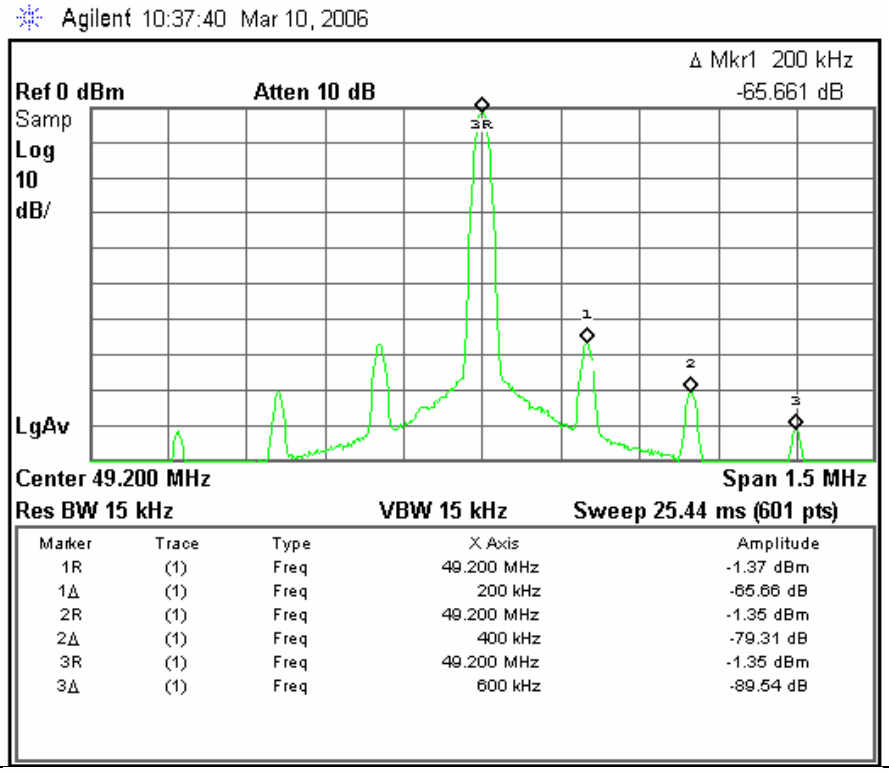
RF PLL Phase Noise with different Delta Sigma Modulator Order

	FM = 2 (2nd order delta sigma modulator) (FM =2 is the recommended setting) Phase Noise measured at 49.2 MHz CP gain = 0.76 mA (8X) (default setting) Fraction Compensation set to 1/5 Dithering disabled. In these three plots, you will note that PN does not vary.
	FM = 3 (3rd order delta sigma modulator) Phase Noise measured at 49.2 MHz CP gain = 0.76 mA (8X) (default setting) Fraction Compensation set to 1/5 Dithering disabled.
	FM=0 (4th order delta sigma modulator) Phase Noise measured at 49.2 MHz CP gain = 0.76 mA (8X) (default setting) Fraction Compensation set to 1/5 Dithering disabled.

RF PLL Phase Noise with different Dithering Settings

	DITH=0 (Disabled) (DITH=0 is the recommended setting) Phase Noise measured at 49.2 MHz CP gain set to 0.76 mA (8X) Fraction Compensation set to 1/5 FM=2 (2nd order delta sigma modulator). In these three plots, you will note that PN does not degrade very little with weak dithering, but does with strong dithering.
	DITH=1 (Weak Dithering) Phase Noise measured at 49.2 MHz CP gain set to 0.76 mA (8X) Fraction Compensation set to 1/5 FM=2 (2nd order delta sigma modulator).
	DITH=2 (Strong Dithering) Phase Noise measured at 49.2 MHz CP gain set to 0.76 mA (8X) Fraction Compensation set to 1/5 FM=2 (2nd order delta sigma modulator).

RF PLL Fractional Spurs with Different CP Currents



Fractional Spurs measured at 49.2 MHz

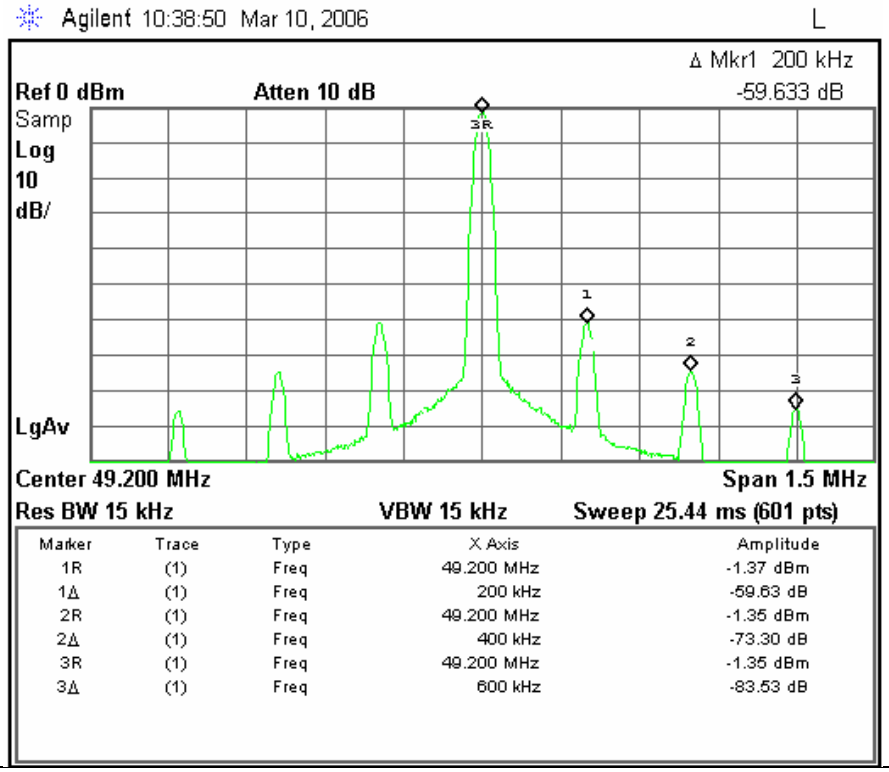
CP gain = 0.76 mA (8X) (default setting)

FM=2

Fraction Compensation set to 1/5

Dithering disabled

An observation is when the charge pump current is doubled; the spurs will increase by approximately 6 dB.



Fractional Spurs measured at 49.2 MHz

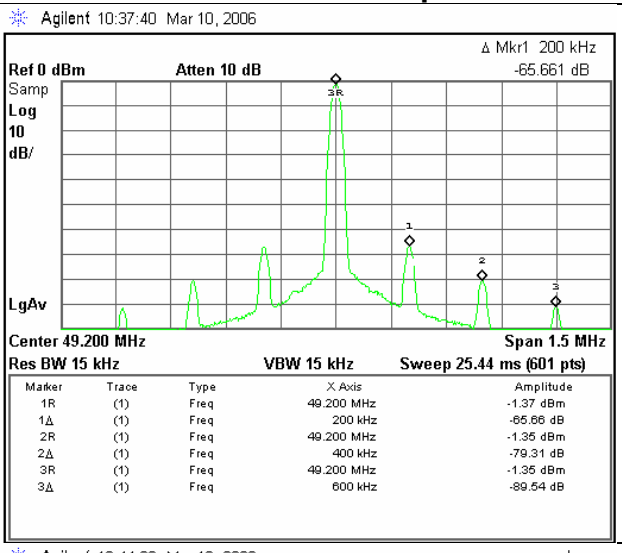
CP gain = 1.52 mA (16X)

FM=2

Fraction Compensation set to 1/5

Dithering disabled

RF PLL Fractional Spurs with different Delta Sigma Modulator Order



FM = 2 (2nd order delta sigma modulator)
(FM =2 is the recommended setting)

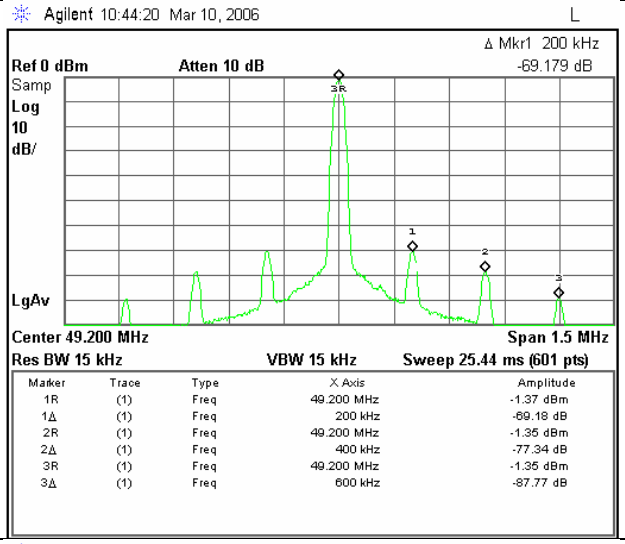
Fractional Spurs measured at 49.2 MHz

CP gain set to 0.76 mA (8X)

Fraction Compensation set to 1/5

Dithering disabled.

In these three plots, you will note that 200 kHz Fractional Spurs only varies slightly. The harmonics (400 kHz and 600 kHz) spurs increase as the delta sigma modulator order increases.



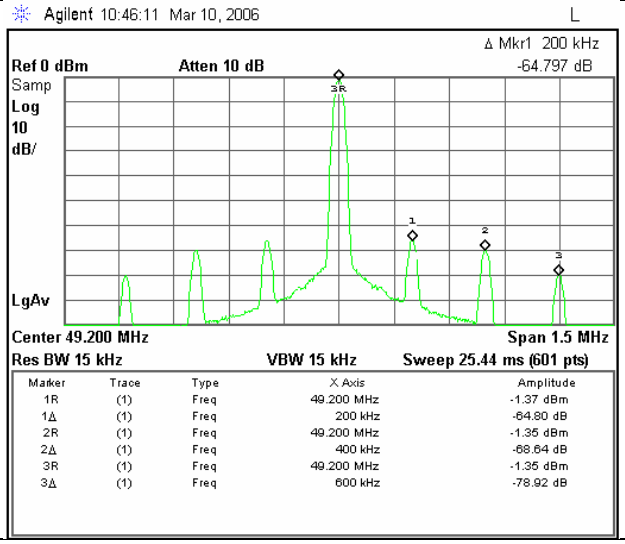
FM=3 (3rd order delta sigma modulator)

Fractional Spurs measured at 49.2 MHz

CP gain set to 0.76 mA (8X)

Fraction Compensation set to 1/5

Dithering disabled.



FM=0 (4th order delta sigma modulator)

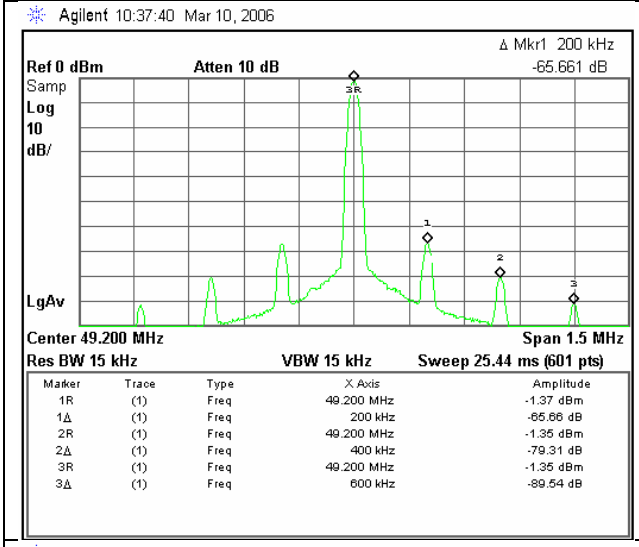
Fractional Spurs measured at 49.2 MHz

CP gain set to 0.76 mA (8X)

Fraction Compensation set to 1/5

Dithering disabled.

RF PLL Fractional Spurs with different Dithering Settings



DITH=0 (Disabled)
(DITH=0 is the recommended setting)

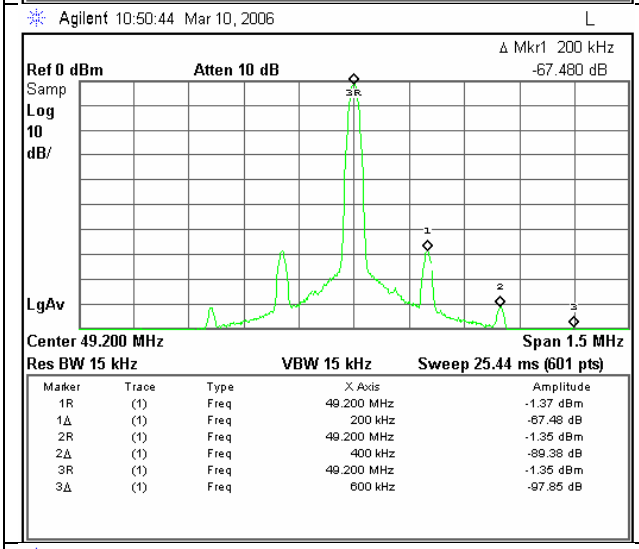
Fractional Spurs measured at 49.2 MHz

CP gain set to 0.76 mA (8X)

Fraction Compensation set to 1/5

FM=2 (2nd order delta sigma modulator).

In these three plots, you will note that Fractional Spurs decreases very little at 200 kHz as compared with the higher harmonics with weak dithering enabled. The spurs and waveform is different with strong dithering enabled.



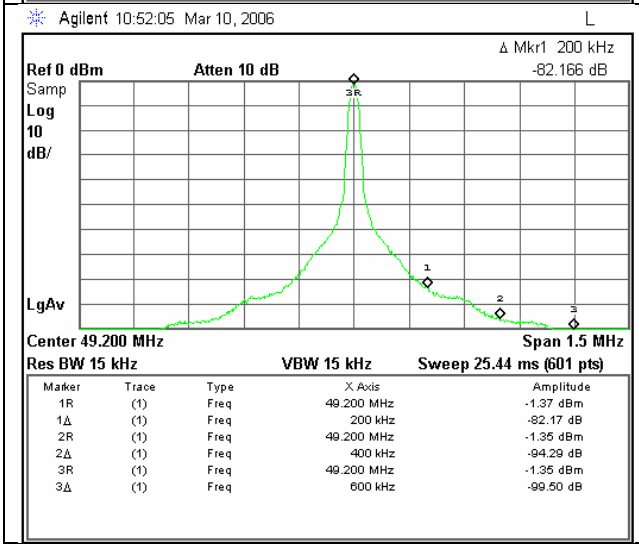
DITH=1 (Weak Dithering)

Fractional Spurs measured at 49.2 MHz

CP gain set to 0.76 mA (8X)

Fraction Compensation set to 1/5

FM=2 (2nd order delta sigma modulator).



DITH=2 (Strong Dithering)

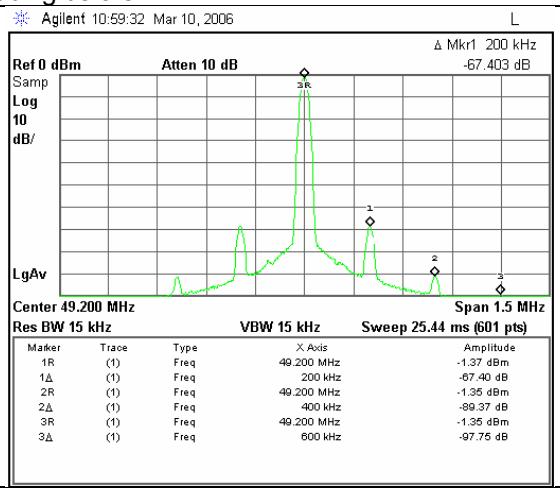
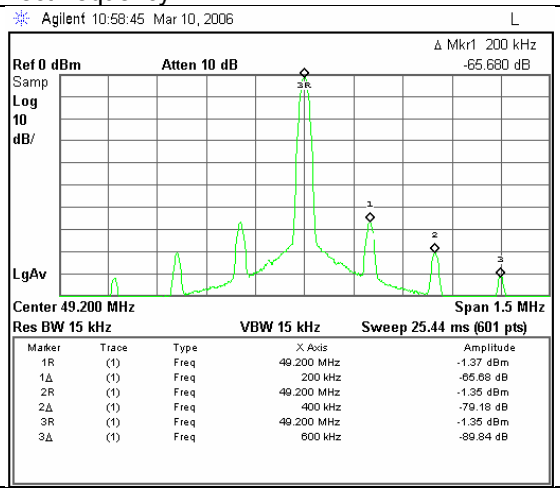
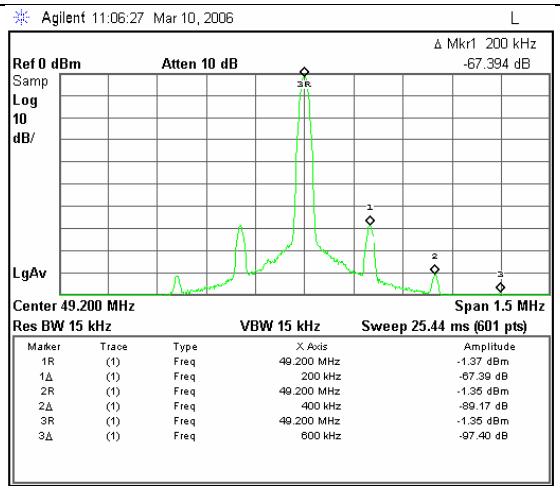
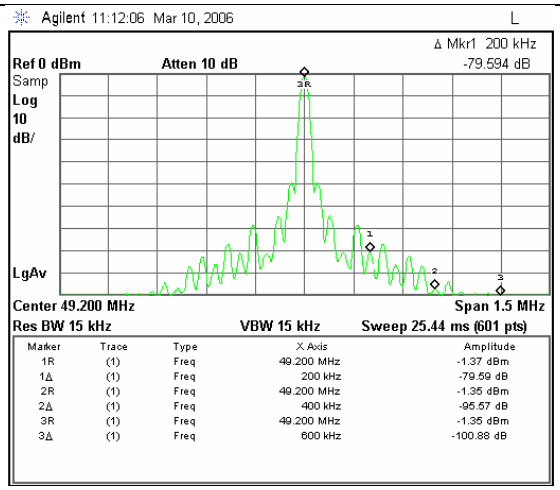
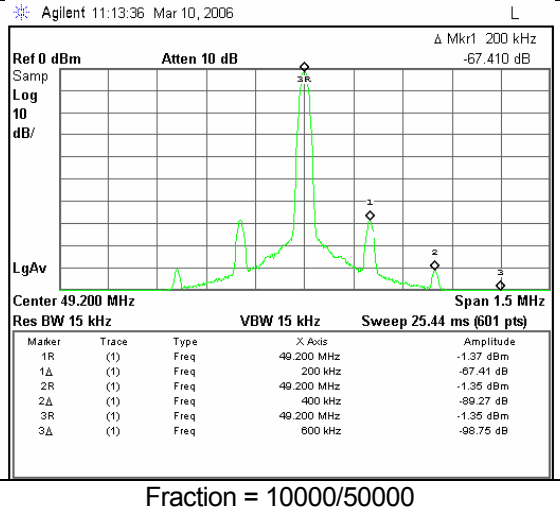
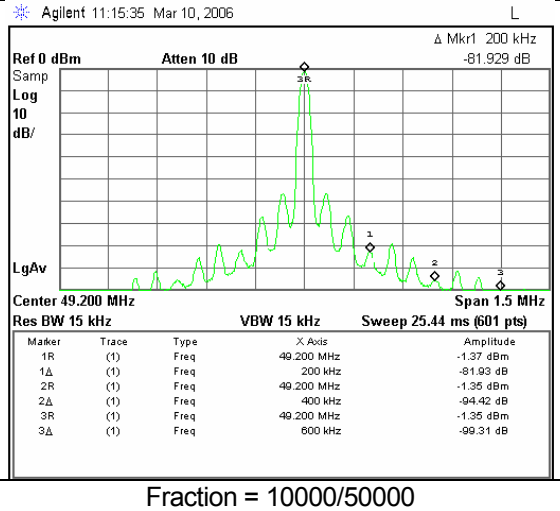
Fractional Spurs measured at 49.2 MHz

CP gain set to 0.76 mA (8X)

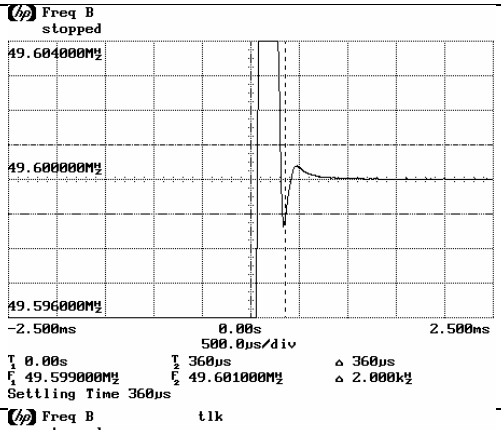
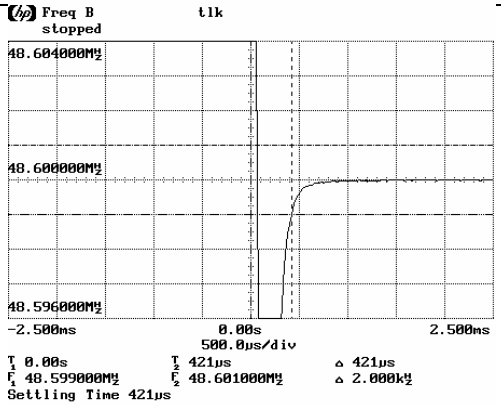
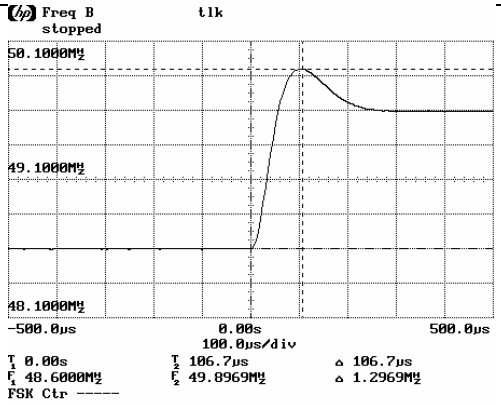
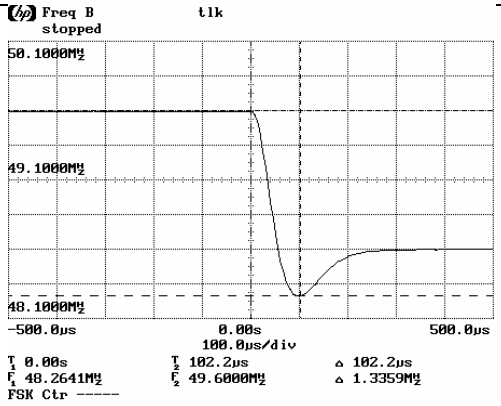
Fraction Compensation set to 1/5

FM=2 (2nd order delta sigma modulator).

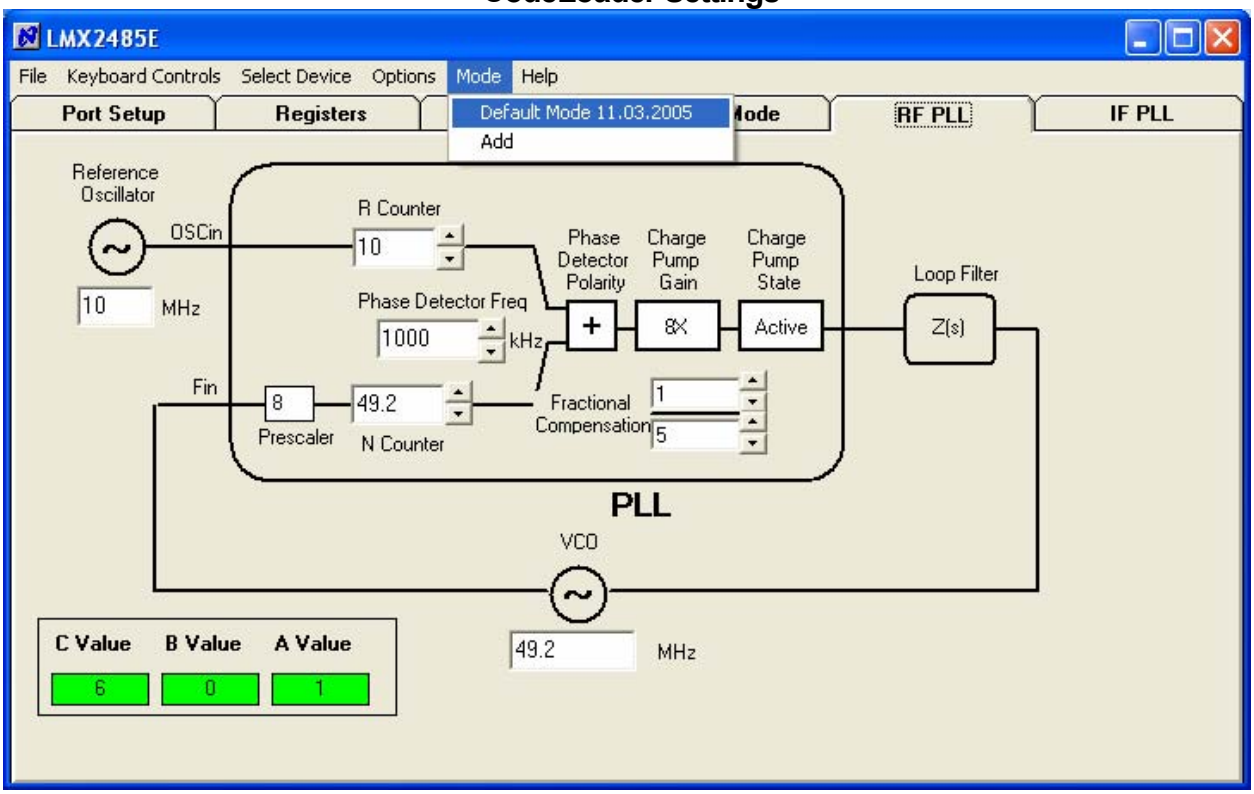
Impact of Large Fractional Denominator (FM=2, DITH=0)

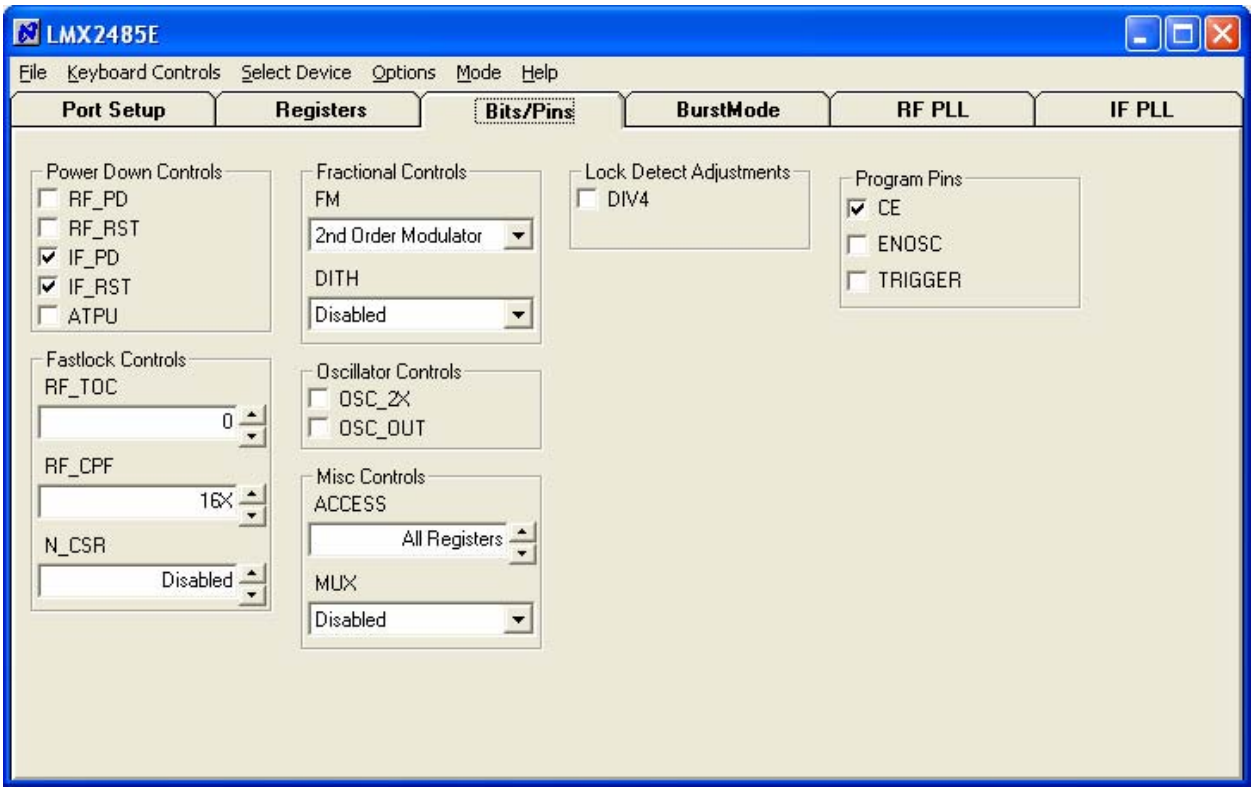
This column loads Reset Modulator before loading Fraction. Only column Reset Modulator is used before loading before FM =2.	This column does not use Reset Modulator. Fractional numerator was increase 5 steps and returned to correct frequency.
	
Fraction = 1/5	Fraction = 1/5
	
Fraction = 10/50	Fraction = 10/50
	
Fraction = 10000/50000	Fraction = 10000/50000

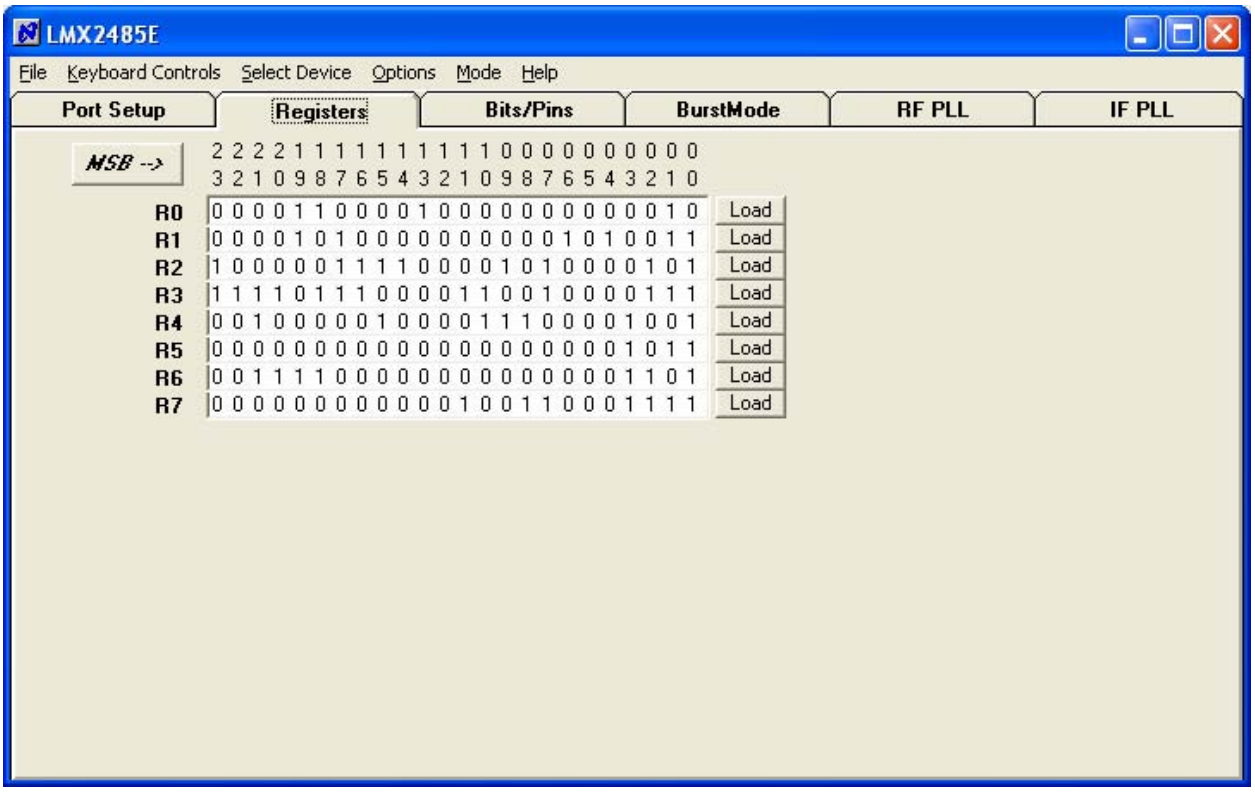
RF PLL Lock Time

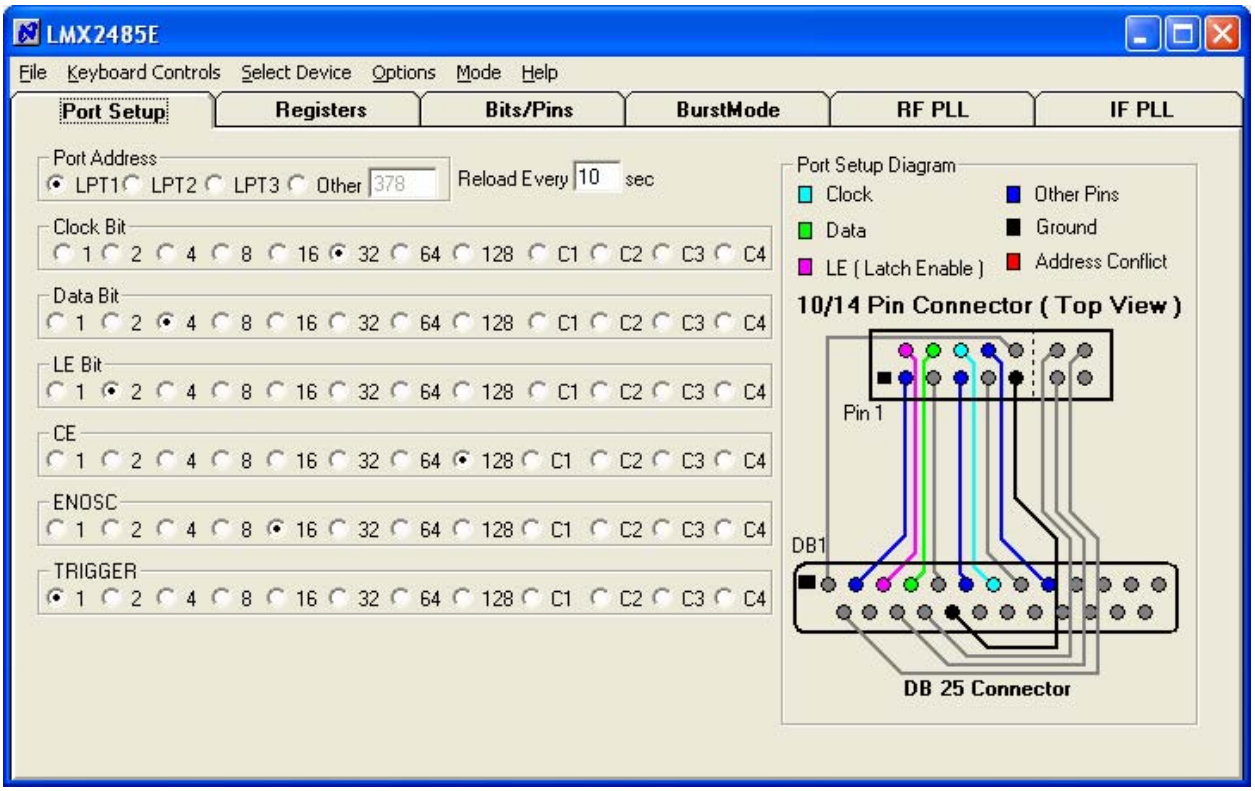
No Cycle Slip Reduction and RF_TOC=0		Positive lock time is 360 µs
		Negative lock time is 421 µs
		RF PLL positive switching waveform
		RF PLL negative switching waveform

CodeLoader Settings

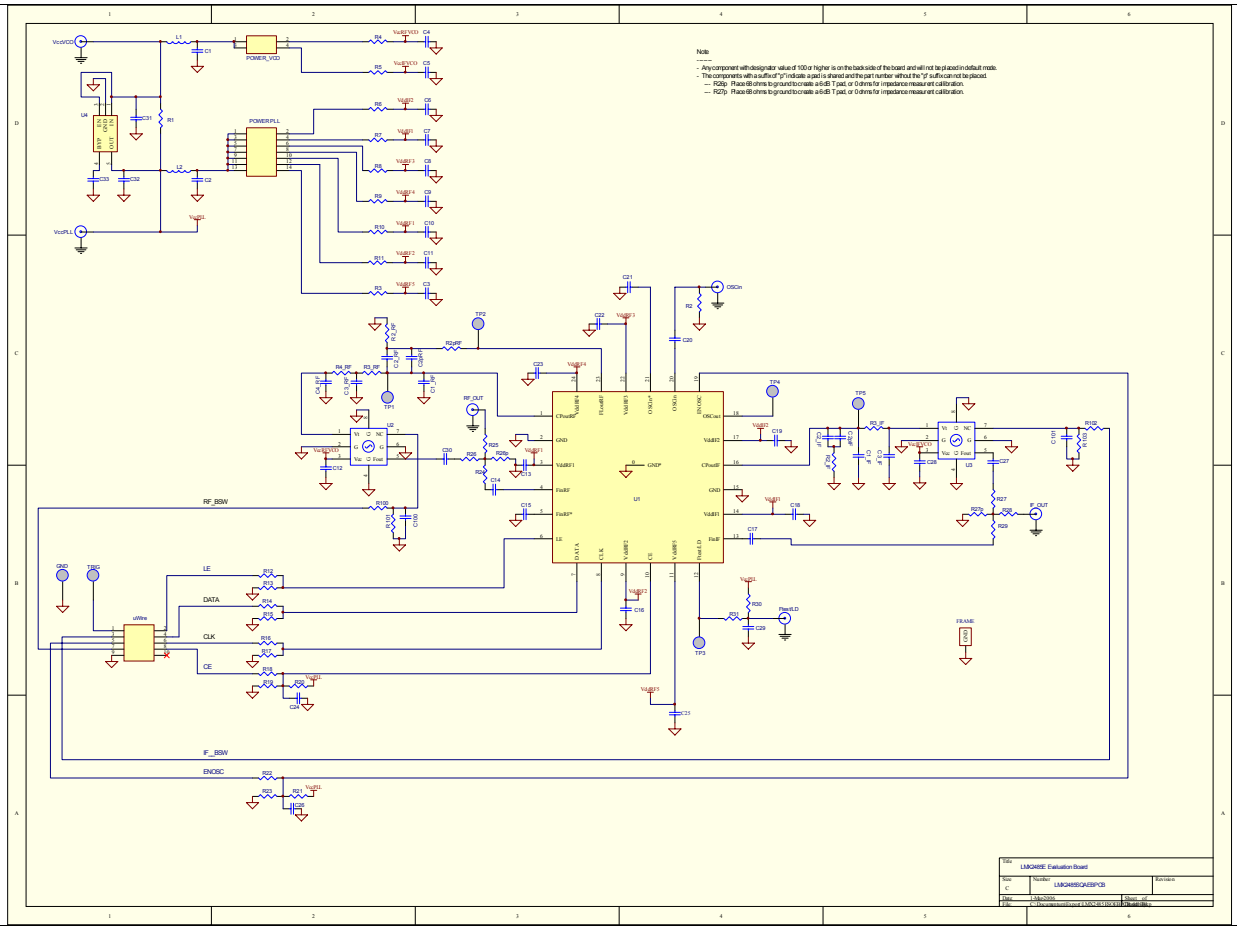




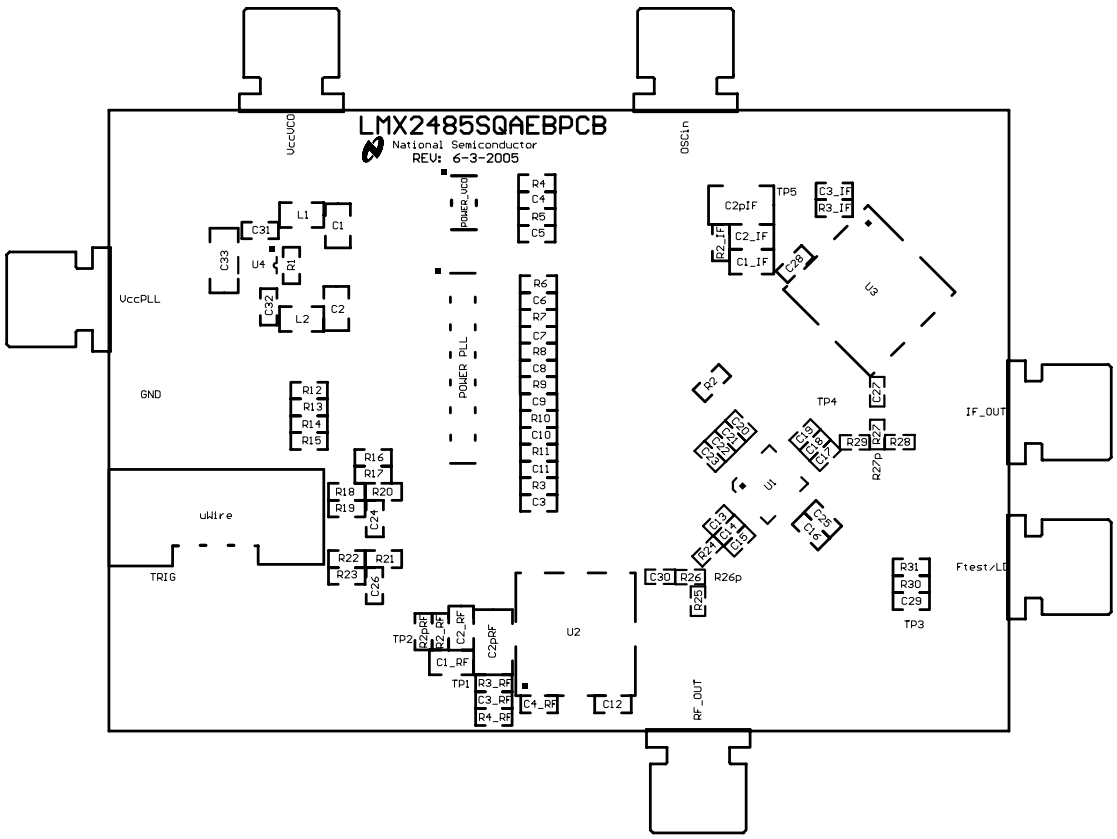




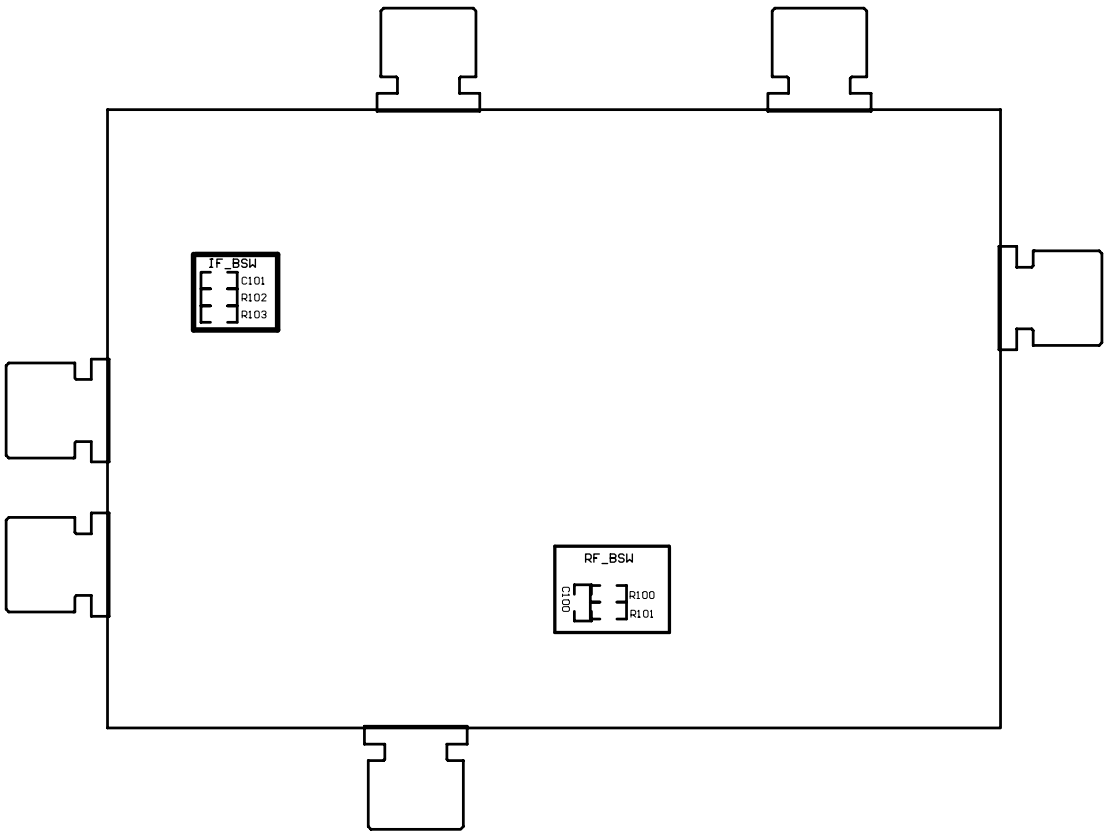
Schematic



Top Build Diagram



Bottom Build Diagram



Bill of Materials

Revision		LMX2485ESQ EVAL BOARD	03.09.2006							
Item	**Qty**	**Manufacturer**	**Part #**	**Value**	**Unit**	**Size**	**Voltage**	**Tolerance**	**Material**	**Designator**
0	n/a	-- C1_IF,C2pRF, C2_IF, C2pIF, C3_IF, C4_RF, C5, C17, C27, C28, C29 -- R1, R2_IF, R2pRF, R3_IF, R5, R20, R21, R26p, R27, R27p, R28, R29, R30, R31 -- R100, R101, R102, R103, C100, C101, VccPLL, Ftest/LD, IF_OUT, U3								
1	1	National Semiconductor	LMX2485SQAEBPCB	er = 4, First GND 10 mils down		4 layer. 62 mils total thickness			FR4	Board REV: 6-3-2005
2	4	SPC Technology	SPCS-8	Stand-Offs					Nylon	Place in 4 holes in edge of board
3	9	Com Con Connectors	CCIJ255G	2-Pin	Shunt				Plastic	Place across POWER_PLL (1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14) and POWER_VCO (1-2, 3-4)
4	1	Com Con Connectors	HTSM3203-4G2	4-Pin	Header				Plastic	POWER_VCO
5	1	Com Con Connectors	HTSM3203-14G2	14-Pin	Header				Plastic	POWER_PLL
6	1	FCI Electronics	52601-S10-8	10-Pin	Header				Plastic	uWire
7	3	Johnson Components	142-0701-851	Edge SMA					Metal	OSCin, RF_OUT, VccVCO
8	11	Kemet	C0603C102J3GAC	1000	pF	0603	25 V	5%	C0G	C12, C13, C14, C15, C16, C18, C19, C22, C23, C25, C30
9	1	Kemet	C0603C182CJ5RAC	1800	pF	0603	50 V	5%	X7R	C3_RF
10	1	Kemet	C1206C103J3GACTU	0.01	uF	1206	50 V	5%	C0G	C33
11	1	Kemet	C0805C682J3RAC	6800	pF	0805	25 V	5%	X7R	C1_RF
12	3	Kemet	C0603C104K3RAC	100	nF	0603	25 V	10%	X7R	C2_RF, C20, C21
13	12	Kemet	C0603C105K3PAC	1	uF	0603	25 V	10%	X5R	C3, C4, C6, C7, C8, C9, C10, C11, C24, C26, C31, C32
14	2	Kemet	C0805C106K8PAC	10	uF	0805	10 V	10%	X5R	C1, C2
15	8	Vishay	CRCW0603100JRT1	10	Ω	0603	10 V	5%	Cermaic	R3, R4, R6, R7, R8, R9, R10, R11
16	5	Vishay	CRCW0603180JRT1	18	Ω	0603	10 V	5%	Cermaic	R24, R25, R26, L1, L2
17	1	Vishay	CRCW0603510FRT1	51	Ω	0603	10 V	10%	Cermaic	R2
18	1	VISHAY	CRCW0603102JRT1	1.0	KΩ	0603	10 V	5%	Cermaic	R2_RF
19	1	VISHAY	CRCW0603222JRT1	2.2	KΩ	0603	10 V	5%	Cermaic	R3_RF
20	1	VISHAY	CRCW0603000ZRT1	0	Ω	0603	10 V	5%	Cermaic	R4_RF
21	5	Vishay	CRCW0603103JRT1	10	KΩ	0603	10 V	5%	Cermaic	R12, R14, R16, R18, R22
22	5	Vishay	CRCW0603123JRT1	12	KΩ	0603	10 V	5%	Cermaic	R13, R15, R17, R19, R23
23	1	National Semiconductor	LMX2485ESQ	PLL	n/a	24P	3.6	n/a	Silicon	U1
24	1	National Semiconductor	LP3985IM5-3.3	Regulator	n/a	SOT23-5	3.3	2%	Silicon	U4
25	1	VARIL	VCO190-52U	51 - 53	MHz	U	5 V		Can	U2

Additional Features of the LMX2485E Evaluation Board

HYBRID VCO FOOTPRINT

Although the evaluation board is created to support a particular VCO, the footprint is flexible and designed such that other VCOs are easy to put on the board. To mount a smaller VCO on the board, scratch off the solder mask with the flat edge of a screwdriver and then put solder on the pads such that it covers the exposed copper.

TEST POINTS

Test Point	Function
TP1	RF Charge Pump voltage
TP2	RF Fastlock output
TP3	Ftest/LD output
TP4	OSCout pin
TRIG	Microwire trigger

BANDSWITCH VCO SUPPORT

The board is also configured so that CodeLoader can control a bandswitch VCO for either the RF or IF PLL. In order to do this, one can use the trigger pin. Don't forget to stuff the components on the bottom layer for the bandswitch option.

COMPONENT OPTIONS

Some components have a 'p' suffix to denote it as an option. These usually have shared footprints and can not both be stuffed. Below is a list of these options.

Component	Option
C2_RF & C2pRF	These components both add in parallel. There are 2 footprints here to allow for different sizes of capacitors
R2_RF & R2pRF	During Fastlock, the chip switches R2pRF in parallel with R2_RF
R26 & R26p	For normal operation R26p should be open. However, for sensitivity measurements 68 Ω may be placed in R26p and R26 can be removed in order to form a 6 dB T-Pad.